

# *CROSSVOLT*<sup>TM</sup>

## Low Voltage Logic Series Databook

LCX Family  
LVX Translator Family  
LVX Bus Switch Family  
LVX Family  
LVQ Family  
LVT Family

Introducing the  
LCX family with 5V tolerant inputs and outputs  
and the  
LVX Dual Supply Translating Transceivers



# CROSSVOLT™ LOW VOLTAGE LOGIC SERIES DATABOOK

1994 Edition

Description and Family Characteristics

Ratings, Specifications and Waveforms

Quality and Reliability

Application and Design Considerations

LCX Family

LVX Translator Family

LVX Bus Switch Family

LVX Family

LVQ Family

LVT Family

Physical Dimensions

1

2

3

4

5

6

7

8

9

10

11

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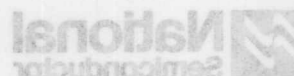
## Introduction

National Semiconductor has created the *CROSSVOLT*<sup>TM</sup> Logic Series of low voltage logic products not only to serve the logic needs of the low voltage market but also to ease the migration to lower supply voltages. At National we recognize that the transition from 5 volts to 3 volts has not been an easy or clean process. According to market research groups, the changeover to pure 3 volt systems will take years. That's why National Semiconductor's *CROSSVOLT* Logic Series features logic families (like our LCX High Speed CMOS Family) and translators (like our LVX Dual Supply CMOS Translating Transceivers) that can interface between 5V logic and 3V logic without the need for additional components. This greatly simplifies the design of mixed voltage supply systems and provides a seamless migration to pure 3V systems.

As processors, memory, and batteries require even lower voltages, National Semiconductor will continue to ease the migration to lower voltages by expanding the *CROSSVOLT* Logic Series portfolio to include new over-voltage tolerant logic families and translators.

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# Table of Contents

Alphanumeric Index .....	viii
Low Voltage Selection Guide .....	ix
<b>Section 1 Description and Family Characteristics</b>	
Description and Family Characteristics .....	1-3
<b>Section 2 Ratings, Specifications and Waveforms</b>	
Low Voltage Logic Ratings, Specifications and Waveforms .....	2-3
<b>Section 3 Quality and Reliability</b>	
Quality and Reliability .....	3-3
<b>Section 4 Application and Design Considerations</b>	
Low Voltage Logic Applications and Design Considerations .....	4-3
<b>Section 5 LCX Family</b>	
LCX Family Features .....	5-3
74LCX240 Low-Voltage Octal Buffer/Line Driver with 5V Tolerant Inputs and Outputs .....	5-4
74LCX244 Low-Voltage Buffer/Line Driver with 5V Tolerant Inputs and Outputs .....	5-7
74LCX245 Low-Voltage Bidirectional Transceiver with 5V Tolerant Inputs and Outputs .....	5-10
74LCX373 Low-Voltage Octal Transparent Latch with 5V Tolerant Inputs and Outputs .....	5-14
74LCX374 Low-Voltage Octal D Flip-Flop with 5V Tolerant Inputs and Outputs .....	5-18
74LCX646 Low-Voltage Octal Transceiver/Register with 5V Tolerant Inputs and Outputs .....	5-22
74LCX652 Low-Voltage Transceiver/Register with 5V Tolerant Inputs and Outputs .....	5-26
74LCX16240 Low-Voltage 16-Bit Inverting Buffer/Line Driver with 5V Tolerant Inputs/Outputs .....	5-31
74LCX16244 Low-Voltage 16-Bit Buffer/Line Driver with 5V Tolerant Inputs and Outputs .....	5-35
74LCX16245 Low-Voltage 16-Bit Bidirectional Transceiver with 5V Tolerant Inputs and Outputs .....	5-39
74LCX16373 Low-Voltage 16-Bit Transparent Latch with 5V Tolerant Inputs and Outputs .....	5-43
74LCX16374 Low-Voltage 16-Bit D Flip-Flop with 5V Tolerant Inputs and Outputs .....	5-47
74LCX16646 Low-Voltage 16-Bit Transceiver/Register with 5V Tolerant Inputs and Outputs .....	5-51
74LCX16652 Low-Voltage Transceiver/Register with 5V Tolerant Inputs and Outputs .....	5-56
<b>Section 6 LVX Translator Family</b>	
LVX Translator Family Features .....	6-3
74LVX3245 8-Bit Dual Supply Translating Transceiver with TRI-STATE Outputs .....	6-4
74LVX4245 8-Bit Dual Supply Translating Transceiver with TRI-STATE Outputs .....	6-9
74LVXC3245 8-Bit Dual Supply Configurable Voltage Interface Transceiver with TRI-STATE Outputs for 3V System .....	6-15
74LVXC4245 8-Bit Dual Supply Configurable Voltage Interface Transceiver with TRI-STATE Outputs .....	6-21
<b>Section 7 LVX Bus Switch Family</b>	
LVX Bus Switch Family Features .....	7-3
74LVX3L383 10-Bit Low Power Bus-Exchange Switch .....	7-4
74LVX3L384 10-Bit Low Power Bus Switch .....	7-7
<b>Section 8 LVX Family</b>	
LVX Family Features .....	8-3
74LVX00 Low Voltage Quad 2-Input NAND Gate .....	8-4
74LVX02 Low Voltage Quad 2-Input NOR Gate .....	8-7
74LVX04 Low Voltage Hex Inverter .....	8-10
74LVX08 Low Voltage Quad 2-Input AND Gate .....	8-13

# Table of Contents (Continued)

## Section 8 LVX Family (Continued)

74LVX14 Low Voltage Hex Inverter with Schmitt Trigger Input	8-16
74LVX32 Low Voltage Quad 2-Input OR Gate	8-19
74LVX74 Low Voltage Dual D-Type Positive Edge-Triggered Flip-Flop	8-22
74LVX86 Low Voltage Quad 2-Input Exclusive-OR Gate	8-26
74LVX125 Low Voltage Quad Buffer with TRI-STATE Outputs	8-29
74LVX138 Low Voltage 1-of-8 Decoder/Demultiplexer	8-32
74LVX157 Low Voltage Quad 2-Input Multiplexer	8-36
74LVX174 Low Voltage Hex D Flip-Flop with Master Reset	8-40
74LVX240 Low Voltage Octal Buffer/Line Driver with TRI-STATE Outputs	8-43
74LVX244 Low Voltage Octal Buffer/Line Driver with TRI-STATE Outputs	8-46
74LVX245 Low Voltage Octal Bidirectional Transceiver	8-49
74LVX273 Low Voltage Octal D Flip-Flop	8-52
74LVX373 Low Voltage Octal Transparent Latch with TRI-STATE Outputs	8-56
74LVX374 Low Voltage Octal D Flip-Flop with TRI-STATE Outputs	8-61
74LVX573 Low Voltage Octal Latch with TRI-STATE Outputs	8-65

## Section 9 LVQ Family

LVQ Family Features	9-3
74LVQ00 Low Voltage Quad 2-Input NAND Gate	9-4
74LVQ02 Low Voltage Quad 2-Input NOR Gate	9-7
74LVQ04 Low Voltage Hex Inverter	9-10
74LVQ08 Low Voltage Quad 2-Input AND Gate	9-13
74LVQ14 Low Voltage Hex Inverter Schmitt Trigger Input	9-16
74LVQ32 Low Voltage Quad 2-Input OR Gate	9-19
74LVQ74 Low Voltage Dual D-Type Positive Edge-Triggered Flip-Flop	9-22
74LVQ86 Low Voltage Quad 2-Input Exclusive-OR Gate	9-27
74LVQ125 Low Voltage Quad Buffer with TRI-STATE Outputs	9-30
74LVQ138 Low Voltage 1-of-8 Decoder/Demultiplexer	9-34
74LVQ151 Low Voltage 8-Input Multiplexer	9-39
74LVQ157 Low Voltage Quad 2-Input Multiplexer	9-44
74LVQ174 Low Voltage Hex D Flip-Flop with Master Reset	9-49
74LVQ240 Low Voltage Octal Buffer/Line Driver with TRI-STATE Outputs	9-54
74LVQ241 Low Voltage Octal Buffer/Line Driver with TRI-STATE Outputs	9-58
74LVQ244 Low Voltage Octal Buffer/Line Driver with TRI-STATE Outputs	9-62
74LVQ245 Low Voltage Octal Bidirectional Transceiver with TRI-STATE Outputs	9-65
74LVQ273 Low Voltage Octal D Flip-Flop	9-69
74LVQ373 Low Voltage Octal Transparent Latch with TRI-STATE Outputs	9-73
74LVQ374 Low Voltage Octal D Flip-Flop with TRI-STATE Outputs	9-78
74LVQ573 Low Voltage Octal Latch with TRI-STATE Outputs	9-83

## Section 10 LVT Family

LVT Family Features	10-3
74LVT125 3.3V ABT Quad Buffer with TRI-STATE Outputs	10-4
74LVT240 3.3V ABT Octal Buffer/Line Driver with TRI-STATE Outputs	10-5
74LVT244 3.3V ABT Octal Buffer/Line Driver with TRI-STATE Outputs	10-6
74LVT245 3.3V ABT Octal Bidirectional Transceiver with TRI-STATE Inputs/Outputs	10-10
74LVT373 3.3V ABT Octal Transparent Latch with TRI-STATE Outputs	10-14
74LVT374 3.3V ABT Octal D Flip-Flop with TRI-STATE Outputs	10-16
74LVT646 3.3V ABT Octal Transceiver/Register with TRI-STATE Outputs	10-18
74LVT652 3.3V ABT Octal Transceiver/Register with TRI-STATE Outputs	10-20
74LVT16240 3.3V ABT 16-Bit Inverting Buffer/Line Driver with TRI-STATE Outputs	10-23
74LVT16244 3.3V ABT 16-Bit Buffer/Line Driver with TRI-STATE Outputs	10-25

74LVT16245 3.3V ABT 16-Bit Transceiver with TRI-STATE Outputs	10-27
74LVT16373 3.3V ABT 16-Bit Transparent Latch with TRI-STATE Outputs	10-29
74LVT16374 3.3V ABT 16-Bit D Flip-Flop with TRI-STATE Outputs	10-31
74LVT16646 3.3V ABT 16-Bit Transceiver/Register with TRI-STATE Outputs	10-33
74LVT16652 3.3V ABT 16-Bit Transceiver/Register with TRI-STATE Outputs	10-36
<b>Section 11 Physical Dimensions</b>	
Available and Planned Package Offering	
Ordering Information and Physical Dimensions	
Physical Dimensions	
Bookshelf	Outputs
Distributors	Inputs and Outputs
74LVT16245 3.3V ABT 16-Bit Transceiver with TRI-STATE Outputs	10-27
74LVT16373 3.3V ABT 16-Bit Transparent Latch with TRI-STATE Outputs	10-29
74LVT16374 3.3V ABT 16-Bit D Flip-Flop with TRI-STATE Outputs	10-31
74LVT16646 3.3V ABT 16-Bit Transceiver/Register with TRI-STATE Outputs	10-33
74LVT16652 3.3V ABT 16-Bit Transceiver/Register with TRI-STATE Outputs	10-36
<b>Section 11 Physical Dimensions</b>	
Available and Planned Package Offering	
Ordering Information and Physical Dimensions	
Physical Dimensions	
Bookshelf	Outputs
Distributors	Inputs and Outputs
74LVT16245 3.3V ABT 16-Bit Transceiver with TRI-STATE Outputs	10-27
74LVT16373 3.3V ABT 16-Bit Transparent Latch with TRI-STATE Outputs	10-29
74LVT16374 3.3V ABT 16-Bit D Flip-Flop with TRI-STATE Outputs	10-31
74LVT16646 3.3V ABT 16-Bit Transceiver/Register with TRI-STATE Outputs	10-33
74LVT16652 3.3V ABT 16-Bit Transceiver/Register with TRI-STATE Outputs	10-36

# Alpha-Numeric Index

Table of Contents (Continued)

74LCX240 Low-Voltage Octal Buffer/Line Driver with 5V Tolerant Inputs and Outputs	5-4
74LCX244 Low-Voltage Buffer/Line Driver with 5V Tolerant Inputs and Outputs	5-7
74LCX245 Low-Voltage Bidirectional Transceiver with 5V Tolerant Inputs and Outputs	5-10
74LCX373 Low-Voltage Octal Transparent Latch with 5V Tolerant Inputs and Outputs	5-14
74LCX374 Low-Voltage Octal D Flip-Flop with 5V Tolerant Inputs and Outputs	5-18
74LCX646 Low-Voltage Octal Transceiver/Register with 5V Tolerant Inputs and Outputs	5-22
74LCX652 Low-Voltage Transceiver/Register with 5V Tolerant Inputs and Outputs	5-26
74LCX16240 Low-Voltage 16-Bit Inverting Buffer/Line Driver with 5V Tolerant Inputs/Outputs	5-31
74LCX16244 Low-Voltage 16-Bit Buffer/Line Driver with 5V Tolerant Inputs and Outputs	5-35
74LCX16245 Low-Voltage 16-Bit Bidirectional Transceiver with 5V Tolerant Inputs and Outputs	5-39
74LCX16373 Low-Voltage 16-Bit Transparent Latch with 5V Tolerant Inputs and Outputs	5-43
74LCX16374 Low-Voltage 16-Bit D Flip-Flop with 5V Tolerant Inputs and Outputs	5-47
74LCX16646 Low-Voltage 16-Bit Transceiver/Register with 5V Tolerant Inputs and Outputs	5-51
74LCX16652 Low-Voltage Transceiver/Register with 5V Tolerant Inputs and Outputs	5-56
74LVQ00 Low Voltage Quad 2-Input NAND Gate	9-4
74LVQ02 Low Voltage Quad 2-Input NOR Gate	9-7
74LVQ04 Low Voltage Hex Inverter	9-10
74LVQ08 Low Voltage Quad 2-Input AND Gate	9-13
74LVQ14 Low Voltage Hex Inverter Schmitt Trigger Input	9-16
74LVQ32 Low Voltage Quad 2-Input OR Gate	9-19
74LVQ74 Low Voltage Dual D-Type Positive Edge-Triggered Flip-Flop	9-22
74LVQ86 Low Voltage Quad 2-Input Exclusive-OR Gate	9-27
74LVQ125 Low Voltage Quad Buffer with TRI-STATE Outputs	9-30
74LVQ138 Low Voltage 1-of-8 Decoder/Demultiplexer	9-34
74LVQ151 Low Voltage 8-Input Multiplexer	9-39
74LVQ157 Low Voltage Quad 2-Input Multiplexer	9-44
74LVQ174 Low Voltage Hex D Flip-Flop with Master Reset	9-49
74LVQ240 Low Voltage Octal Buffer/Line Driver with TRI-STATE Outputs	9-54
74LVQ241 Low Voltage Octal Buffer/Line Driver with TRI-STATE Outputs	9-58
74LVQ244 Low Voltage Octal Buffer/Line Driver with TRI-STATE Outputs	9-62
74LVQ245 Low Voltage Octal Bidirectional Transceiver with TRI-STATE Outputs	9-65
74LVQ273 Low Voltage Octal D Flip-Flop	9-69
74LVQ373 Low Voltage Octal Transparent Latch with TRI-STATE Outputs	9-73
74LVQ374 Low Voltage Octal D Flip-Flop with TRI-STATE Outputs	9-78
74LVQ573 Low Voltage Octal Latch with TRI-STATE Outputs	9-83
74LVT125 3.3V ABT Quad Buffer with TRI-STATE Outputs	10-4
74LVT240 3.3V ABT Octal Buffer/Line Driver with TRI-STATE Outputs	10-5
74LVT244 3.3V ABT Octal Buffer/Line Driver with TRI-STATE Outputs	10-6
74LVT245 3.3V ABT Octal Bidirectional Transceiver with TRI-STATE Inputs/Outputs	10-10
74LVT373 3.3V ABT Octal Transparent Latch with TRI-STATE Outputs	10-14
74LVT374 3.3V ABT Octal D Flip-Flop with TRI-STATE Outputs	10-16
74LVT646 3.3V ABT Octal Transceiver/Register with TRI-STATE Outputs	10-18
74LVT652 3.3V ABT Octal Transceiver/Register with TRI-STATE Outputs	10-20
74LVT16240 3.3V ABT 16-Bit Inverting Buffer/Line Driver with TRI-STATE Outputs	10-23
74LVT16244 3.3V ABT 16-Bit Buffer/Line Driver with TRI-STATE Outputs	10-25
74LVT16245 3.3V ABT 16-Bit Transceiver with TRI-STATE Outputs	10-27
74LVT16373 3.3V ABT 16-Bit Transparent Latch with TRI-STATE Outputs	10-29
74LVT16374 3.3V ABT 16-Bit D Flip-Flop with TRI-STATE Outputs	10-31
74LVT16646 3.3V ABT 16-Bit Transceiver/Register with TRI-STATE Outputs	10-33
74LVT16652 3.3V ABT 16-Bit Transceiver/Register with TRI-STATE Outputs	10-36

# Alpha-Numeric Index (Continued)



Low Voltage Logic Selection Guide

74LVX00 Low Voltage Quad 2-Input NAND Gate .....	8-4
74LVX02 Low Voltage Quad 2-Input NOR Gate .....	8-7
74LVX04 Low Voltage Hex Inverter .....	8-10
74LVX08 Low Voltage Quad 2-Input AND Gate .....	8-13
74LVX3L383 10-Bit Low Power Bus-Exchange Switch .....	7-4
74LVX3L384 10-Bit Low Power Bus Switch .....	7-7
74LVX14 Low Voltage Hex Inverter with Schmitt Trigger Input .....	8-16
74LVX32 Low Voltage Quad 2-Input OR Gate .....	8-19
74LVX74 Low Voltage Dual D-Type Positive Edge-Triggered Flip-Flop .....	8-22
74LVX86 Low Voltage Quad 2-Input Exclusive-OR Gate .....	8-26
74LVX125 Low Voltage Quad Buffer with TRI-STATE Outputs .....	8-29
74LVX138 Low Voltage 1-of-8 Decoder/Demultiplexer .....	8-32
74LVX157 Low Voltage Quad 2-Input Multiplexer .....	8-36
74LVX174 Low Voltage Hex D Flip-Flop with Master Reset .....	8-40
74LVX240 Low Voltage Octal Buffer/Line Driver with TRI-STATE Outputs .....	8-43
74LVX244 Low Voltage Octal Buffer/Line Driver with TRI-STATE Outputs .....	8-46
74LVX245 Low Voltage Octal Bidirectional Transceiver .....	8-49
74LVX273 Low Voltage Octal D Flip-Flop .....	8-52
74LVX373 Low Voltage Octal Transparent Latch with TRI-STATE Outputs .....	8-56
74LVX374 Low Voltage Octal D Flip-Flop with TRI-STATE Outputs .....	8-61
74LVX573 Low Voltage Octal Latch with TRI-STATE Outputs .....	8-65
74LVX3245 8-Bit Dual Supply Translating Transceiver with TRI-STATE Outputs .....	6-4
74LVX4245 8-Bit Dual Supply Translating Transceiver with TRI-STATE Outputs .....	6-9
74LVXC3245 8-Bit Dual Supply Configurable Voltage Interface Transceiver with TRI-STATE Outputs for 3V System .....	6-15
74LVXC4245 8-Bit Dual Supply Configurable Voltage Interface Transceiver with TRI-STATE Outputs .....	6-21

No	Yes	18	x	x				18374	18-Bit D
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## Latches

Function/Description	Type	LVO	LVS	LCS	LVT	Data Inputs	Enable (Level)	TRI-STATE® Outputs	Broadcastable Pin Out
Octal Transparent Latch	373	x	x	x	x	8	1 (H)	Yes	No
Octal Transparent Latch	573	x	x			8	1 (L)	Yes	Yes
18-Bit Transparent Latch	18373		x	x	x	18	2 (H)	Yes	No

## Buffers/Line Drivers

Function/Description	Type	LVO	LVS	LCS	LVT	Enable (Level)	Inverting/Non-Inverting
Quad Buffer	125	x	x		x	4 (L)	N
Octal Buffer/Line Driver	240	x	x	x	x	2 (L)	I
Octal Buffer/Line Driver	241	x				1 (L) + 1 (H)	N
Octal Buffer/Line Driver	244	x	x	x	x	2 (L)	N
18-Bit Buffer/Line Driver	18240			x	x	4 (L)	I
18-Bit Buffer/Line Driver	18244			x	x	4 (L)	N



## Low Voltage Logic Selection Guide

### Gates

Function/Description	Type	LVQ	LVX	LCX	LVT
Quad 2-Input NAND	00	x	x		
Quad 2-Input AND	08	x	x		
Quad 2-Input OR	32	x	x		
Quad 2-Input NOR	02	x	x		
Quad 2-Input Exclusive-OR	86	x	x		
Hex Inverter	04	x	x		
Hex Schmitt Trigger Inverter	14	x	x		

### Flip-Flops

Function/Description	Type	LVQ	LVX	LCX	LVT	Data Inputs	TRI-STATE® Outputs	Master Reset
Dual D	74	x	x			2	No	No
Hex D	174	x	x			6	No	Yes
Octal D	273	x	x			8	No	Yes
Octal D	374	x	x	x	x	8	Yes	No
16-Bit D	16374			x	x	16	Yes	No

### Latches

Function/Description	Type	LVQ	LVX	LCX	LVT	Data Inputs	Enable (Level)	TRI-STATE® Outputs	Broadside Pin Out
Octal Transparent Latch	373	x	x	x	x	8	1 (H)	Yes	No
Octal Transparent Latch	573	x	x			8	1 (L)	Yes	Yes
16-Bit Transparent Latch	16373			x	x	16	2 (H)	Yes	No

### Buffers/Line Drivers

Function/Description	Type	LVQ	LVX	LCX	LVT	Enable (Level)	Inverting/Non-Inverting
Quad Buffer	125	x	x		x	4 (L)	N
Octal Buffer/Line Driver	240	x	x	x	x	2 (L)	I
Octal Buffer/Line Driver	241	x				1 (L) + 1 (H)	N
Octal Buffer/Line Driver	244	x	x	x	x	2 (L)	N
16-Bit Buffer/Line Driver	16240			x	x	4 (L)	I
16-Bit Buffer/Line Driver	16244			x	x	4 (L)	N

**Decoders/Demultiplexers**

Function/Description	Type	LVQ	LVX	LCX	LVT	Enable (Level)	Active Address Inputs	Outputs
1-of-8 Decoder/Demultiplexer	138	x	x			2 (L) + 1 (H)	3	8

**Multiplexers**

Function/Description	Type	LVQ	LVX	LCX	LVT	Enable (Level)	True Output	Complement Output
8-Input Multiplexer	151	x				1 (L)	Yes (1)	Yes (1)
Quad 2-Input Multiplexer	157	x	x			1 (L)	Yes (4)	No

**Transceivers/Registers**

Function/Description	Type	LVQ	LVX	LCX	LVT	Registers	Enable (Level)	TRI-STATE® Outputs
Octal Bidirectional Transceiver	245	x	x	x	x	No	1 (L)	Yes
Octal Bus Transceiver and Register	646			x	x	Yes	1 (L)	Yes
Octal Bus Transceiver and Register	652			x	x	Yes	1 (L) + 1 (H)	Yes
16-Bit Bidirectional Transceiver	16245			x	x	No	2 (L)	Yes
16-Bit Bus Transceiver and Register	16646			x	x	Yes	2 (L)	Yes
16-Bit Bus Transceiver and Register	16652			x	x	Yes	2 (L) + 2 (H)	Yes

**Translators**

Function/Description	Type	LVQ	LVX	LCX	LVT	TRI-STATE® Outputs	3V or 5V Configurable I/O	V <sub>CCA</sub>	V <sub>CCB</sub>
Octal Translating Transceivers	3245		x			Yes	No	2.7V–3.6V	4.5V–5.5V
Octal Translating Transceivers	4245		x			Yes	No	4.5V–5.5V	2.7V–3.6V
Octal Translating Transceivers	C3245		x			Yes	Yes	2.7V–3.6V	3.0V–5.5V
Octal Translating Transceivers	C4245		x			Yes	Yes	4.5V–5.5V	2.7V–5.5V

**Bus Switches**

Function/Description	Type	LVQ	LVX	LCX	LVT	TRI-STATE® Outputs	3V or 5V Configurable I/O	V <sub>CC</sub>
10-Bit Bus Switch or 5-Bit Bus Exchanger	3L383		x			Yes	Yes	4.0V–5.0V
10-Bit Bus Switch	3L384		x			Yes	Yes	4.0V–5.0V

Decoders/Demultiplexers									
Function/Description	Type	LVO	LVS	LCS	LVT	Enable (Level)	Active Address Inputs	Outputs	
1-of-8 Decoder/Demultiplexer	138	x	x			2 (L) + 1 (H)	3	8	
Multiplexers									
Function/Description	Type	LVO	LVS	LCS	LVT	Enable (Level)	True Output	Complement Output	
8-Input Multiplexer	151	x				1 (L)	Yes (1)	Yes (1)	
Quad 2-Input Multiplexer	157	x	x			1 (L)	Yes (4)	No	
Transceivers/Registers									
Function/Description	Type	LVO	LVS	LCS	LVT	Registers	Enable (Level)	TRI-STATE® Outputs	
Octal Bidirectional Transceiver	245	x	x	x	x	No	1 (L)	Yes	
Octal Bus Transceiver and Register	848			x	x	Yes	1 (L)	Yes	
Octal Bus Transceiver and Register	852			x	x	Yes	1 (L) + 1 (H)	Yes	
16-Bit Bidirectional Transceiver	18245			x	x	No	2 (L)	Yes	
16-Bit Bus Transceiver and Register	18648			x	x	Yes	2 (L)	Yes	
16-Bit Bus Transceiver and Register	18652			x	x	Yes	2 (L) + 2 (H)	Yes	
Translators									
Function/Description	Type	LVO	LVS	LCS	LVT	TRI-STATE® Outputs	3V or 5V Configurable I/O	VCCA	VCCB
Octal Translating Transceivers	3245		x			Yes	No	2.7V-3.6V	4.5V-5.5V
Octal Translating Transceivers	4245		x			Yes	No	4.5V-5.5V	2.7V-3.6V
Octal Translating Transceivers	C3245		x			Yes	Yes	2.7V-3.6V	3.0V-5.5V
Octal Translating Transceivers	C4245		x			Yes	Yes	4.5V-5.5V	2.7V-3.6V
Bus Switches									
Function/Description	Type	LVO	LVS	LCS	LVT	TRI-STATE® Outputs	3V or 5V Configurable I/O	VCC	
10-Bit Bus Switch or 5-Bit Bus Exchanger	31383		x			Yes	Yes	4.0V-5.0V	
10-Bit Bus Switch	31384		x			Yes	Yes	4.0V-5.0V	



## Section 1 Contents

1-3	..... Description and Family Characteristics
1-3	..... Introduction
1-3	..... Family Specification Comparison
1-5	..... Operating Voltage Features of National Semiconductor's Low Voltage Logic Families
1-6	..... Low Voltage Logic Family Feature Comparison
1-7	..... Process Technology
1-7	..... Switching Speed and Static Output Drive
1-8	..... Switching Induced Noise
1-8	..... Low Voltage Product Summary
1-9	..... LVC—Low Voltage Quiet CMOS Logic
1-10	..... LVX—Low Voltage (with 5V Tolerant Inputs)
1-11	..... LVX—Low Voltage Dual Supply CMOS Translating Transceivers
1-12	..... LVX—Low Voltage High Speed CMOS Logic (with 5V Tolerant Inputs and Outputs)
1-13	..... LVT—Low Voltage High Speed BiCMOS Logic
1-14	.....

## Section 1 Description and Family Characteristics



## Section 1 Contents

Description and Family Characteristics .....	1-3
Introduction .....	1-3
Family Specification Comparison .....	1-3
Operating Voltage Features of National Semiconductor's Low Voltage Logic Families .....	1-5
Low Voltage Logic Family Feature Comparison .....	1-6
Process Technology .....	1-7
Switching Speed and Static Output Drive .....	1-7
Switching Induced Noise .....	1-8
Low Voltage Product Summaries .....	1-8
LVQ—Low Voltage Quiet CMOS Logic .....	1-9
LVX—Low Voltage CMOS Logic (with 5V Tolerant Inputs) .....	1-10
LVX—Low Voltage Dual Supply CMOS Translating Transceivers .....	1-11
LVX—Low Voltage CMOS Bus Switches .....	1-12
LCX—Low Voltage High Speed CMOS Logic (with 5V Tolerant Inputs and Outputs) .....	1-13
LVT—Low Voltage High Speed BiCMOS Logic .....	1-14



## Description and Family Characteristics

### Introduction

In order to provide optimum logic solutions for a variety of low voltage applications, National Semiconductor offers several low voltage logic product families. Each of these families possess a unique set of features and operating characteristics optimized for a particular low voltage application. All National low voltage logic devices share the following features:

- low or "zero" static power dissipation (<100 nA typical for LVQ)
- reduced dynamic power consumption
- lower switching noise than comparable higher supply voltage counterparts
- compliance with EIA-JEDEC low voltage interface standard #8-1B

Output drive, translation capabilities, switching speed and interface flexibility are examples of the characteristics that differentiate these low voltage logic families.

### Recommended Operating Conditions

	LVQ	LVX			LCX (Preliminary)	LVT (Advance Information)
		LVX	Dual Supply Translating Transceivers	Bus Switches		
	'245	'245	4245	'3L383	'245	'245
Supply Voltage ( $V_{CC}$ )	2.0V to 3.6V	2.0V to 3.6V	2.7V to 3.6V and 4.5V to 5.5V	4.0V to 5.5V	2.0V to 3.6V	2.7V to 3.6V
Input Voltage ( $V_I$ )	0V to $V_{CC}$	0V to 5.5V	0V to 5.5V		0V to 5.5V	0V to 5.5V
Output Voltage ( $V_O$ )						
Active	0V to $V_{CC}$	0V to $V_{CC}$	0V to $V_{CC}$		0V to $V_{CC}$	0V to $V_{CC}$
TRI-STATE®	0V to $V_{CC}$	0V to $V_{CC}$	0V to $V_{CC}$		0V to 5.5V	0V to 5.5V
Operating Temperature ( $T_A$ )	-40°C to +85°C	-40°C to +85°C	-40°C to +85°C	-40°C to +85°C	-40°C to +85°C	-40°C to +85°C
Input Rise and Fall Time	125 mV/ns	0 ns/V to 100 ns/V	8 ns/V		10 ns/V	10 ns/V

### Family Specifications

To assist the designer in selecting one of National Semiconductor's Low Voltage Logic families the specifications for a '245 function are compared below for easy reference. Please reference individual data sheets for specific device information.

## DC Electrical Characteristics

		LVQ	LVX			LCX (Preliminary)	LVT (Advance Information)
			LVX	Dual Supply Translating Transceivers	Bus Switches		
		'245	'245	4245	'3L383	'245	'245
V <sub>IH</sub>	Min	2.0V	2.0V	2.0V	2.0V	2.0V	2.0V
V <sub>IL</sub>	Max	0.8V	0.8V	0.8V	0.8V	0.8V	0.8V
V <sub>OH</sub>	Min	2.48V @ I <sub>OH</sub> = -12 mA	2.48V @ I <sub>OH</sub> = -4 mA	3.76V @ I <sub>OH</sub> = -24 mA		2.2V @ I <sub>OH</sub> = -24 mA	2.0V @ I <sub>OH</sub> = -32 mA
V <sub>OL</sub>	Max	0.44V @ I <sub>OL</sub> = +12 mA	0.44V @ I <sub>OL</sub> = 4 mA	0.44V @ I <sub>OL</sub> = 24 mA		0.55V @ I <sub>OL</sub> = 24 mA	0.55V @ I <sub>OL</sub> = 64 mA
I <sub>IN</sub>	Max	±1.0 μA	±1.0 μA	±1.0 μA	±1 μA	±5.0 μA	±10 μA
I <sub>CC</sub>	Max	40 μA	40 μA	80 μA	3 μA	10 μA	12 mA
I <sub>OZ</sub>	Max	±3.0 μA	±2.5 μA	±5 μA	±1 μA	±5 μA	±1 μA
V <sub>OLP</sub>	Max	0.8V	0.8V	1.5V/0.8V		0.8	TBD
V <sub>OLV</sub>	Min	-0.8V	-0.8V	-1.2V/-0.8V		0.8	TBD
V <sub>IHD</sub>	Max	2V	2V	2V			TBD
V <sub>ILD</sub>	Max	0.8V	0.8V	0.8V			TBD

## AC Electrical Characteristics

		LVQ	LVX			LCX (Preliminary)	LVT (Advance Information)
			LVX	Dual Supply Translating Transceivers	Bus Switches		
Units = ns		'245	'245	4245	'3L383	'245	'245
T <sub>PHL</sub>	Max	10.5	11.5	8.5	0.25	7	4
T <sub>PLH</sub>	Max	10.5	11.5	8	0.25	7	4
T <sub>PZL</sub>	Max	13.5	16.5	9	6.5	8.5	5.5
T <sub>PZH</sub>	Max	13.5	16.5	9.5	6.5	8.5	5.5
T <sub>PHZ</sub>	Max	15	14.5	8.5	5.5	7.5	5.9
T <sub>PLZ</sub>	Max	15	14.5	7	5.5	7.5	4.8
T <sub>OSHL</sub>	Max	1.5	1.5	1.5		1	1
T <sub>OSLH</sub>	Max	1.5	1.5	1.5		1	1

## Operating Voltage Features of National Semiconductor's Low Voltage Logic Families

One of the most popular uses of low voltage logic is for translation between voltage levels. '244 and '245 functions are most often used for translation, but other functions are also used. The following table summarizes the translation capabilities for each family.

Parameter	Pure 3V	Mixed Voltage Tolerant	Translators			Mixed Voltage Tolerant	Mixed Voltage Tolerant
			Non-Configurable	Configurable	Conditional (Note 1)		
	LVQ	LVX	LVX3245/4245	LVXC3245/4245	LVX3L383/4	LCX	LVT
V <sub>CC</sub>	2.0V–3.6V	2.0V–3.6V			4.0V–5.5V	2.0V–3.6V	2.7V–3.6V
V <sub>CCA</sub>			4.5V–4.5V or 2.7V–3.6V	2.7V–3.6V or 4.5V–5.5V			
V <sub>CCB</sub>			4.5V–5.5V or 2.7V–3.6V	2.7V–5.5V or 3.0V–5.5V			
Inputs	3V	Accepts 3V and 5V	0V–V <sub>CC</sub>	0V–V <sub>CC</sub>	0V–V <sub>CC</sub>	Accepts 3V and 5V	Accepts 3V and 5V
I/O and Outputs	3V	3V Only	0V–V <sub>CC</sub>	0V–V <sub>CC</sub>	Interfaces with 3V/5V	Accepts 3V and 5V (Note 2)	Accepts 3V and 5V (Note 2)
A-Port			Interfaces with 3V or 5V (Fixed)	Interfaces with 3V or 5V (Fixed)			
B-Port			Interfaces with 3V or 5V (Fixed)	Interfaces with 3V or 5V (Configurable)			

**Note 1:** Translation feature implemented by adding a diode between V<sub>CC</sub> and the device.

**Note 2:** Only when outputs in TRI-STATE condition (when an I/O is an input it can accept a 5V stimulus).

All the families except LVQ provide some sort of translation capability. LVX and LCX will accept 5V signals on the inputs, and LCX will also tolerate 5V signals on the outputs when the outputs are in TRI-STATE. The LVX3L383/4 devices can be used as "zero delay" translators when a diode is used between V<sub>CC</sub> and the devices. For pure translation,

the LVX Dual Supply Translating Transceivers are unsurpassed. They can even be used to drive 5V CMOS inputs and the LVXC3245/4245 devices have B-port I/O which can be configured for 3V or 5V "on the fly". For further information on interfacing National Semiconductor's Low Voltage Logic to 5V Logic families see Section 4.

## Low Voltage Logic Family Feature Comparison

Feature	LVQ	LVX			LCX (Preliminary)	LVT (Advance Information)
		LVX	Dual Supply Translating Transceivers	Bus Switches		
Translation (5V $\leftrightarrow$ 3V) Input	no	yes	yes	yes	yes	yes
Bidirectional	no	no	yes	yes	yes	yes
Configurable	no	no	yes	no	no	no
VOLP < 0.8V	yes	yes	yes	yes	yes	yes
Zero Static Power	yes	yes	yes	yes	yes	no
Low EMI	yes	yes	yes	yes	yes	yes
Latchup > 300 mA	yes	yes	yes	yes	yes	yes
Alternative Source Available	yes	yes	yes	yes	yes	yes
Power Up Output Hi-Impedance	no	no	no	no	no	yes
Power Down Output Hi-Impedance	no	no	no	no	yes	yes
Corner Supply Pin	yes	yes	yes	yes	yes	yes
Product Range						
Gates/MSI	yes	yes	no	no	no	no
Octals	yes	yes	yes	no	yes	yes
10-Bit	no	no	no	yes	no	no
16-Bit	no	no	no	no	yes	yes
Current Package Offerings	SOIC, EIAJ, QSOP-Octals Only	SOIC, EIAJ, SSOP I	SOIC, QSOP	SOIC, QSOP, TSSOP	SOIC, EIAJ, TSSOP, SSOP-16-Bit Only	SOIC, EIAJ, TSSOP, SSOP-16-Bit Only

## Process Technology

A wide range of processing technologies are used to manufacture the various low voltage product families. Process selection is based upon the conversion of product electrical features to technological demands at the device level. Table I summarizes the process characteristics by product line.

TABLE I

Product Line	LVQ	LVX					Units
		LVX	Dual Supply Translating Transceivers	Bus Switches	LCX	LVT	
Process	1.5 CMOS	1.0 CMOS	0.8 CMOS	1.0 BICMOS	0.8 CMOS	1.0 BICMOS	
<b>Device Characteristics</b>							
TOX	nom	225	150	150	150	150	Å
Abs Max $V_{CC}$	max	7.0	7.0	7.0	7.0	7.0	V
LEFF NMOS	nom	1.05	0.65	0.6	0.65	0.6	μm
LEFF PMOS	nom	1.05	1.0	0.75	0.7	0.75	μm
$\beta_{NPN}$	nom	n/a	n/a	n/a	n/a	90	
<b>Process Characteristics</b>							
Starting Material		P-epi on P++	P-epi on P++	N-epi/N++	N-epi/N++	N-epi/N++	N-epi/N++
Minimum Feature		1.4	1.0	0.8	1.0	0.8	1.0
M1 Pitch	min	4.5	3.5	2.0	3.5	2.0	3.5
M2 Pitch	min	6.0	5.0	2.5	5.0	2.5	5.0

## Switching Speed and Static Output Drive

National Semiconductor offers the low voltage system designer choices when it comes to switching speed, output drive and mixed supply level flexibility. Table II summarizes the performance of the various low voltage logic families with regard to these system critical parameters.

TABLE II

Parameters	LVQ	LVX			LCX	LVT (Advance Information)	Units
		LVX	Dual Supply Translating Transceivers	Bus Switches			
$T_{PD}$ (3.0V, 85°C)	9.5	12.0	9.0	250 ps (Note 1)	6.5	4.0	ns
$I_{OL}$ (Note 2)	12	4	24	n/a	24	64	mA
$I_{OH}$ (Note 3)	-12	-4	-24	n/a	-24	-32	mA
Abs Max $V_{CC}$	7	7	7	7	7	7	V
Maximum $V_{IH}$ ( $V_{CC} = 3.0V$ )	$V_{CC} + 0.5$	5.5	$V_{CC} + 0.5$	5.5	5.5	5.5	V
Maximum $V_{OH}$ ( $V_{CC} = 3.0V$ )	$V_{CC} + 0.5$	$V_{CC} + 0.5$	$V_{CC} + 0.5$	5.5	5.5 (Note 4)	5.5 (Note 4)	V

Note 1: Calculated based upon 50 pF load and 5Ω nominal channel resistance

Note 2: Refer to individual datasheets for  $V_{OL}$  level.

Note 3: Refer to individual datasheets for  $V_{OH}$  level.

Note 4:  $V_{OH}$  is permitted to rise above  $V_{CC}$  only when  $OEB \geq V_{IH}$ .

## Switching Induced Noise

Reducing the power supply potential and compressing the output swing of a high drive output buffer reduces the switching induced noise that it propagates or generates. At the same time using advanced technology to provide aggressive propagation delay and large load driving capabilities serves to increase  $V_{OLP}$  and  $V_{OLV}$ . The net result is that great care must be taken in the design of high speed, low voltage line drivers if the noise benefits of the reduced supply and compressed swing are to be preserved. By incorporating a low-voltage-tuned version of National Semiconductor's proven Graduated Turn-On (GTO™) circuitry (Note 1), best-in-class propagation delay guarantees are achieved along with the industry's only guaranteed maximum specifications for ground bounce, undershoot and dynamic input thresholds.

Figure 1 depicts a functionally correct, but schematically simplified representation of the National Semiconductor GTO circuit used throughout the low voltage portfolios. In the case of an output high-to-low transition this circuit behaves according to the following flow.

**Note 1:** United States Patents #4,961,010, #5,036,222 and #5,081,374

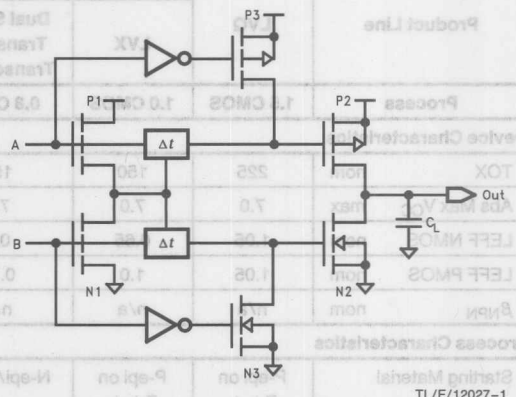
### INITIAL CONDITIONS

- $V_g[P1]$  and  $V_g[P2]$  are discharged to  $\sim 0V$
- $V_g[P1, P2] = V_{CC}$
- $V_{ds}[P1, P2] = 0V \rightarrow I_{ds}[P1] = I_{ds}[P2] = 0$  (assumes purely capacitive load)
- $V_g[N1]$  and  $V_g[N2] = 0V \rightarrow I_{ds}[N1] = I_{ds}[N2] = 0$
- $V_o = V_{CC}$

### NODES A AND B ARE EXTERNALLY CHARGED TO $V_{CC}$ FROM $0V$

- $V_g[P1, N1]$  rises to  $V_{CC}$
- The  $\Delta t$  circuits delay the delivery of the signals A and B to P2 and N2
- $V_g[P1] = 0V, I_{ds}[P1] = 0 \rightarrow P1$  is off
- $V_g[N1] = V_{CC}, V_{ds}[N1] = V_{CC}$ , N1 saturates and begins to discharge  $C_L$

- The  $\Delta t$  circuits now pass the signals at A and B
- $V_g[P2] = 0V, I_{ds}[P2] = 0 \rightarrow P2$  is off
- $V_g[N2] = V_{CC}, V_{ds}[N2] = V_{CC}$ , N2 saturates and discharges  $C_L$
- $I_{ds}[N2] \gg I_{ds}[N1]$  and  $I_{ds}[P2] \gg I_{ds}[P1]$



**FIGURE 1. Simplified Schematic of GTO Noise Control**

The connectivity within the  $\Delta t$  blocks is such that all signals arriving at nodes A and B are delayed en route to P2 and N2. This would serve to degrade the disable time performance of the buffer. N3 and P3 restore the disable time performance by bypassing the delay elements during LZ or HZ output transitions only. The turn-off signals to N2 and P2 are thereby delivered without delay.

## Low Voltage Product Summaries

To assist the system designer in understanding the specific operating characteristics of each of the various products a brief description of the circuit topology for each is presented.

Parameters	LVS	LVX	LVX	LVX	LVX	LVX
Maximum $V_{IH}$ ( $V_{CC} = 3.0V$ )	$V_{CC} + 0.8$	$V_{CC} + 0.8$	$V_{CC} + 0.8$	$V_{CC} + 0.8$	$V_{CC} + 0.8$	$V_{CC} + 0.8$
Maximum $V_{OH}$ ( $V_{CC} = 3.0V$ )	$V_{CC} + 0.8$	$V_{CC} + 0.8$	$V_{CC} + 0.8$	$V_{CC} + 0.8$	$V_{CC} + 0.8$	$V_{CC} + 0.8$
Maximum $V_{OL}$ ( $V_{CC} = 3.0V$ )	$V_{CC} + 0.8$	$V_{CC} + 0.8$	$V_{CC} + 0.8$	$V_{CC} + 0.8$	$V_{CC} + 0.8$	$V_{CC} + 0.8$
Maximum $V_{OLP}$ ( $V_{CC} = 3.0V$ )	$V_{CC} + 0.8$	$V_{CC} + 0.8$	$V_{CC} + 0.8$	$V_{CC} + 0.8$	$V_{CC} + 0.8$	$V_{CC} + 0.8$
Maximum $V_{OLV}$ ( $V_{CC} = 3.0V$ )	$V_{CC} + 0.8$	$V_{CC} + 0.8$	$V_{CC} + 0.8$	$V_{CC} + 0.8$	$V_{CC} + 0.8$	$V_{CC} + 0.8$
Maximum $V_{OLP}$ ( $V_{CC} = 3.0V$ )	$V_{CC} + 0.8$	$V_{CC} + 0.8$	$V_{CC} + 0.8$	$V_{CC} + 0.8$	$V_{CC} + 0.8$	$V_{CC} + 0.8$
Maximum $V_{OLV}$ ( $V_{CC} = 3.0V$ )	$V_{CC} + 0.8$	$V_{CC} + 0.8$	$V_{CC} + 0.8$	$V_{CC} + 0.8$	$V_{CC} + 0.8$	$V_{CC} + 0.8$
Maximum $V_{OLP}$ ( $V_{CC} = 3.0V$ )	$V_{CC} + 0.8$	$V_{CC} + 0.8$	$V_{CC} + 0.8$	$V_{CC} + 0.8$	$V_{CC} + 0.8$	$V_{CC} + 0.8$
Maximum $V_{OLV}$ ( $V_{CC} = 3.0V$ )	$V_{CC} + 0.8$	$V_{CC} + 0.8$	$V_{CC} + 0.8$	$V_{CC} + 0.8$	$V_{CC} + 0.8$	$V_{CC} + 0.8$

## LVQ—Low Voltage Quiet CMOS Logic

The LVQ product line is targeted for 3.3V-only applications where interfacing to 5V or other interface levels is not a requirement. Figure 2 depicts the circuitry common to the LVQ family. Complementary diode input protection is used but **without** the usual current limiting input resistor. This dramatically reduces the forward resistance associated with these junctions and significantly improves their input overshoot and undershoot clamping capabilities. Diode D1 protects the input node from positive voltage ESD events by conducting the charge to the  $V_{CC}$  node and away from the ESD sensitive structures internal to the device. D1 becomes forward biased when charge builds up on the input node such that the potential difference across D1 is larger than  $V_F$  for D1. This type of input protection circuit precludes the application of input signals containing components that rise above  $V_{CC}$  by more than the  $V_F$  of D1.

The complementary MOS output drivers used throughout the LVQ family include drain isolation junctions D5 and D6 that are reverse biased during normal operation. This implies that signals applied to any LVQ output node must not rise above  $V_{CC} + V_F[D5]$  or below  $GND - V_F[D6]$ . Operation outside this range will forward bias D5 or D6 and thus creating an undesirable forward conducting path to  $V_{CC}$  or ground. This current may result in violation of the Absolute Maximum Ratings for these devices which in turn may adversely and permanently affect device performance and reliability.

LVQ devices include output drivers that feature National Semiconductor's GTO noise control circuitry. The output transistors are designed with suitable dynamic current sourcing and sinking capabilities to assure incident wave switching when driving non-terminated transmission lines having a characteristic impedance of 750Ω or greater.

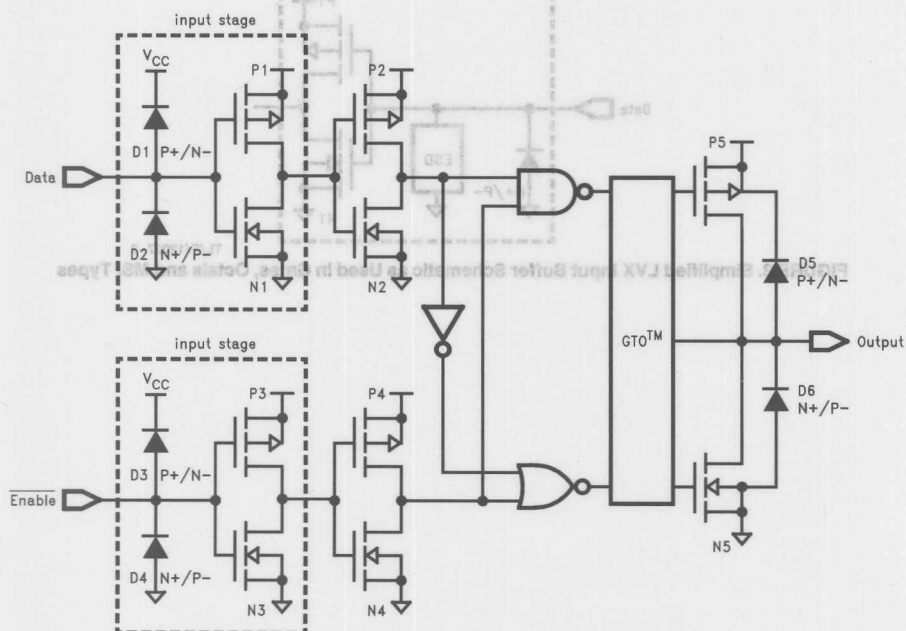


FIGURE 2. Simplified LVQ Schematic Diagram

TL/F/12027-2

## LVX—Low Voltage CMOS Logic (with 5V Tolerant Inputs)

The LVX family is made up of three product groupings, each possessing a unique set of interfacing capabilities and characteristics optimized for specific applications.

- Gates, octals and MSI types
- Dual Supply Translating Transceivers
- Bus Switches

The LVX gates, octals and MSI types all feature an alternate input ESD protection scheme that permit their inputs to receive signals whose logic-high levels exceed the supply voltage. Figure 3 shows a simplified LVX input buffer schematic that includes the alternate ESD structure.

Since there no longer exists a forward junction between the data input pin and  $V_{CC}$  the conduction path between the

data pin and  $V_{CC}$  is disrupted. The positive voltage limitation on the input pins increases from  $V_{CC} + V_F$  to the minimum breakdown path tied to the input. For the LVX family of gates, octals and MSI products this value (BVDSS) is in excess of 7V. As in the case of LVQ products, LVX utilizes complementary MOS devices in its output stage and therefore cannot tolerate signals applied to its outputs outside the range defined by  $GND - V_F$  and  $V_{CC} + V_F$ .

The output drive available from LVX is scaled to provide the lowest possible dynamic power dissipation and leakage. By virtue of their pin capacitance specifications, low noise and high speed, LVX products are ideally applied in 3.3V battery powered systems where system performance requires 5V FACT propagation delays.

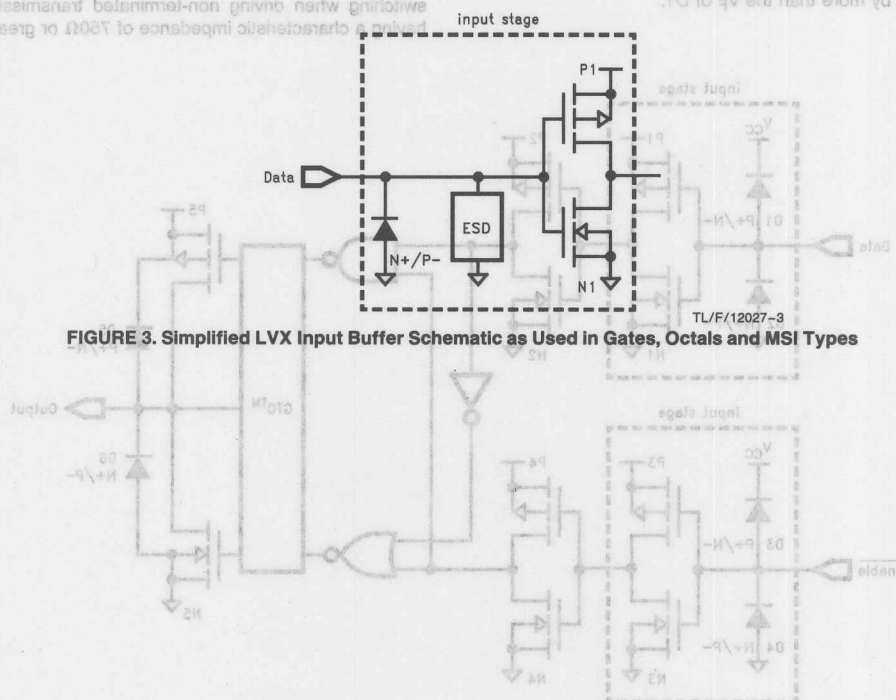


FIGURE 3. Simplified LVX Input Buffer Schematic as Used in Gates, Octals and MSI Types

## LVX—Low Voltage Dual Supply CMOS Translating Transceivers

The LVX family of true translating transceivers use an entirely different approach to the mixed supply interfacing issue. Not just overvoltage tolerant, these devices are true translators—meaning that they receive 3V signals and output 5V signals, and receive 5V signals and output 3V signals. This is accomplished by internally dividing the devices such that the circuitry associated with the A-side is electrically isolated from the B-side. This dual supply architecture permits the LVX translator family to interface 3V signals and 5V signals with **zero static power dissipation**.

In the case of the 74LVX4245 device the A-side is dedicated to 5V operation and  $V_{CCA}$  is specified for the range 4.5V–5.5V. The B-side is dedicated 3.3V and  $V_{CCB}$  is specified for the range 2.7V–3.6V. The LVXC3245 and LVXC4245 offer further enhanced interfacing in that the B-side is designed to operate over an extended range of I/O and supply levels. For these types  $V_{CCB}$  is permitted to be

set to any value between 2.7V and 5.5V. The I/O levels on the B-side will track or scale automatically according to the level set on  $V_{CCB}$ . This B-side operation is completely independent of  $V_{CCA}$ . The A-port and control input buffers are referenced to  $V_{CCA}$  and do not vary with  $V_{CCB}$ . Refer to Figure 4. The configurable dual supply translating transceivers (LVXC) are designed to tolerate floating inputs on the B-port when  $V_{CCA}$  and the control signals are set to valid operating levels. The combination of on-the-fly interface flexibility together with "empty socket" tolerance is intended to benefit designers of PC card systems where expansion cards with different supply potentials must be accommodated.

Along with the advanced interfacing capabilities offered by the LVX dual supply translators, these products offer switching speeds equivalent to 5V FCT/FAST but with Quiet Series noise performance and 3.3V supply.

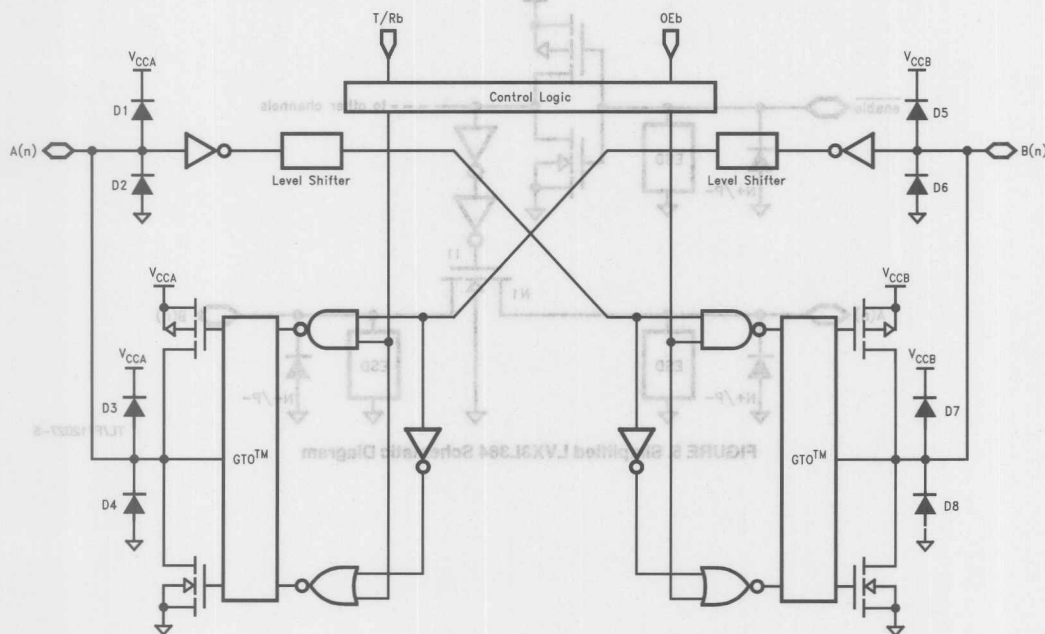


FIGURE 4. Simplified LVX Translator Schematic Diagram

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## LVX—Low Voltage CMOS Bus Switches

The LVX3L383 and LVX3L384 low impedance switches complete the LVX family. By virtue of their low "on" resistance these ten channel NMOS pass gates can be used to provide a high speed, bi-directional interface between mixed supply busses. Figure 5 depicts a single channel representation of the LVX3L384.

The enhancement type NMOS pass gate N1 utilized in all LVX3L383 and LVX3L384 low impedance switches provides bi-directional signal level translation capability. The source (Note 1) of the pass gate will always be clamped to  $V_g - V_{tn}$  irrespective of the drain potential.  $V_g$  is set by  $V_{CC}$  via inverter I1. Consider the following case:

- $V_{CC}$  is set to 4.1V
- $V_{tn} = 0.8V$

- $V_a = 5.0V$
- $V_{enable} = 0V$
- $V_b$  is initially discharged

Given these conditions pass gate N1 saturates ( $V_{ds} > V_{gs} - V_t$ ) and begins charging its source B(N) positively. As B(n) rises the difference between B(n) and  $V_{CC}$  ( $V_{gs}[N1]$ ) decreases. When B(n) rises to within  $V_{tn}$  of  $V_{CC}$ , N1 is cut-off and conduction ceases independent of the potential at A(n). The final terminal conditions then are:

$$V[A(n)] = 5.0V$$

$$V[B(n)] = V_{CC} - V_{tn} = 3.3V$$

and the translation is completed.

**Note 1:** For an NMOS transistor the source is defined as the diffusion with lowest potential.

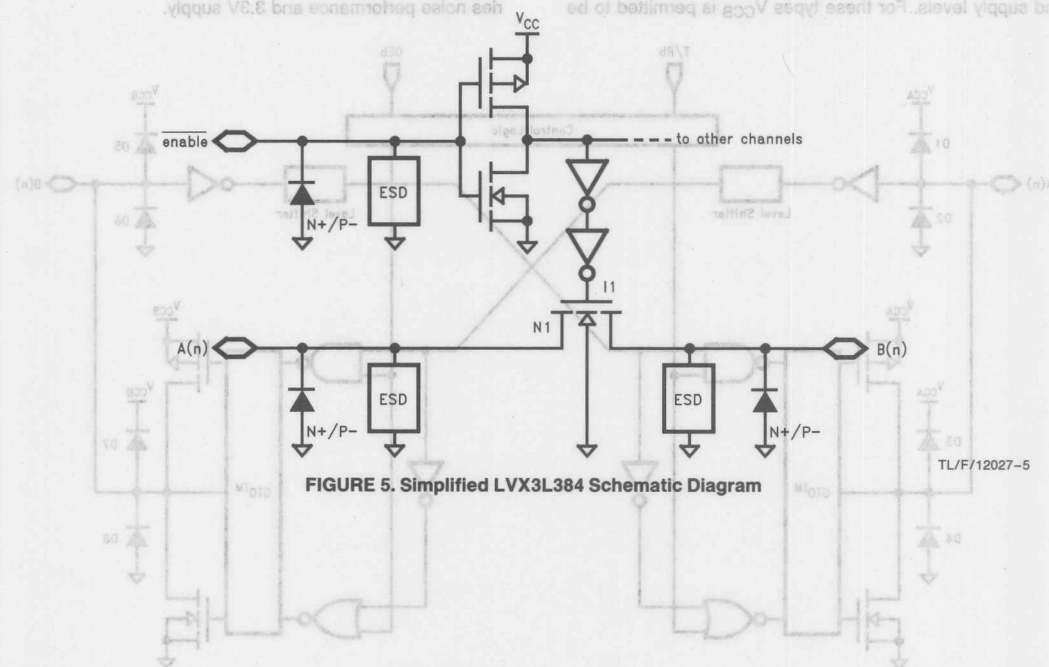


FIGURE 5. Simplified LVX3L384 Schematic Diagram

## LCX—Low Voltage High Speed CMOS Logic (with 5V Tolerant Inputs and Outputs)

The LCX product line represents National Semiconductor's most advanced low voltage CMOS product line. These devices offer mixed 3V–5V capability and are recommended for applications where 3.3V and 5.0V subsystems interface with one another and where low power consumption is a necessity. By virtue of a proprietary input/output structure (Note 1), the LCX family of products will tolerate input and output (Note 2) node exposure to signals or DC levels that exceed the  $V_{CC}$  level. Refer to Figure 6 for schematic description of a typical LCX circuit.

Note that the output PMOS device P5 has its bulk potential supplied by the output of the comparator X1 rather than by  $V_{CC}$  as in conventional CMOS. The circuitry contained within the comparator is designed such that the output is always the greater of  $V_{CC}$  or  $V_O$ . This technique circumvents the  $P^+ / N^-$  bulk-source forward junction that usually appears between the PMOS drain at the output and the bulk connection of the output PMOS which is usually tied to  $V_{CC}$ . Eliminating this junction is fundamental to the powered-down high Z and overvoltage tolerance features that distinguish LCX from other low voltage CMOS products.

**Note 1:** U.S. and international patent protection applied for.

**Note 2:** Output overvoltage is permitted unconditionally for tri-stated outputs. For active outputs, see datasheet.

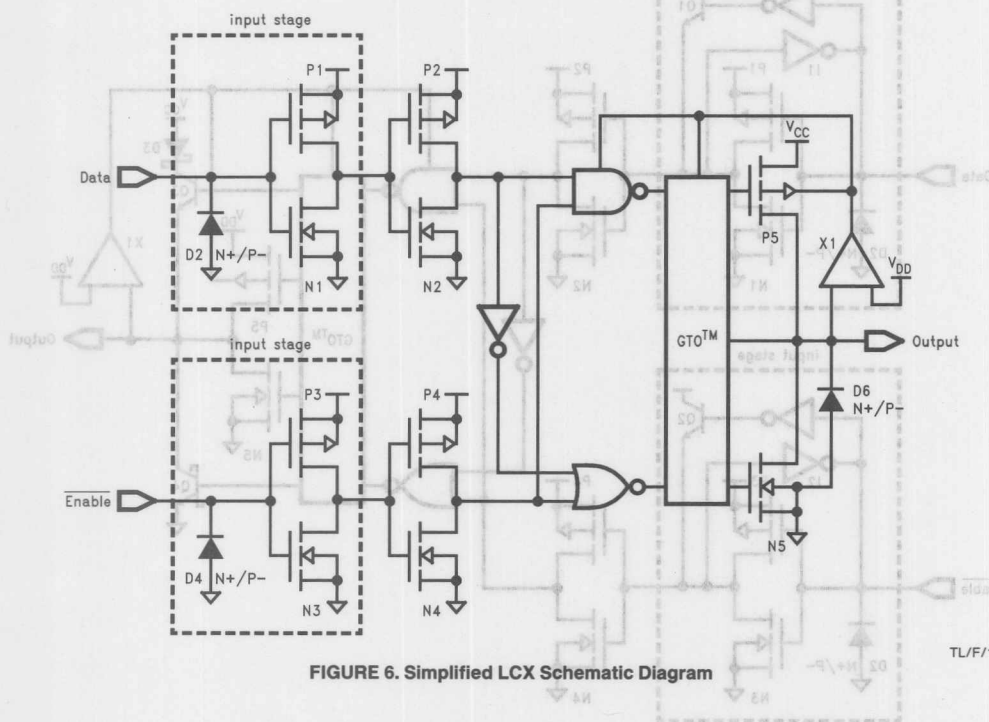


FIGURE 6. Simplified LCX Schematic Diagram

TL/F/12027-6

## LVT—Low Voltage High Speed BiCMOS Logic

LVT is National Semiconductor's highest performance low voltage family of products. Manufactured using sub-micron BiCMOS technology, LVT includes all the mixed-supply interface features of LCX in addition to BJT-enhanced propagation delays. These 5V tolerant low voltage devices are recommended for applications where 3.3V and 5.0V subsystems interface with one another and where high speed and high drive are required. By virtue of hysteresis applied by I1 and I2 directly at the input node (refer to Figure 7), LVT devices will tolerate floating input conditions that would otherwise lead to increased leakage or compromises in system data integrity.

The output buffer design is based upon the LCX circuit and includes overvoltage tolerance at the output as does LCX. AC and DC performance in the LVT version of the output is augmented by the addition of the parallel NPN devices Q3 and Q4. The Q4 base drive required to sink the rated  $I_{OL}$  results in a nominal  $I_{CCL}$  of less than 10 mA. The reverse-biased Schottky device D3 prevents output overvoltages that exceed  $V_{CEO}$  from corrupting the low voltage supply. LVT benefits from this protection when  $V_{CC}$  is applied as well as when the device is powered-down.

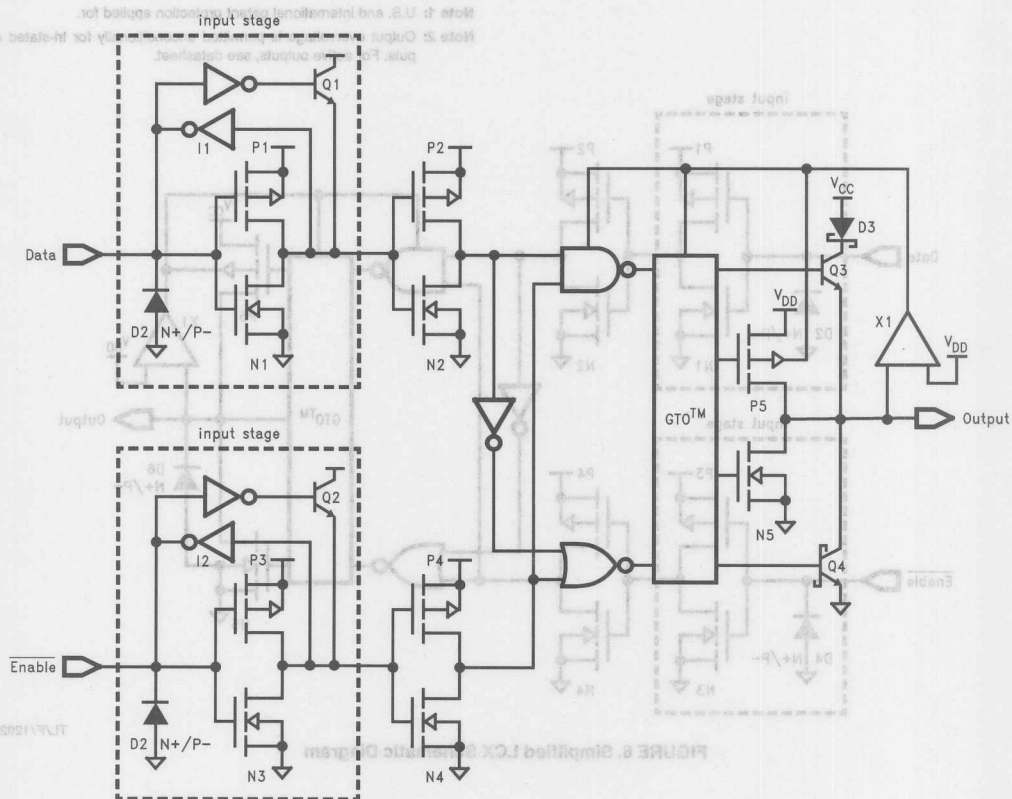


FIGURE 7. Simplified LVT Schematic Diagram

TL/F/12027-7

At National Semiconductor it is our mission to excel in serving chosen markets by delivering semiconductor intensive products and services of the highest quality and value, thereby providing a competitive advantage to our customers worldwide. Should you have any additional questions about our Low Voltage Products, please contact your local sales office or our Customer Response Center at 1-800-272-9959 within the U.S., 1-800-258-6768 in Canada.



## Section 2 Contents

2-3	Low Voltage Logic Ratings, Specifications and Waveforms
2-3	Definition of Terms
2-4	Characterization Philosophy
2-4	Power Dissipation—Test Philosophy
2-5	AC Loading and Waveforms
2-6	Test Conditions
2-7	Propagation Delay, $t_{\text{PROP}}$ , Set and Hold Times
2-7	Enable and Disable Times
2-8	Electrostatic Discharge
2-8	Low Voltage Logic Noise Characteristics
2-9	External Definitions and Examples
2-14	Skew Definitions and Examples

## Section 2 Ratings, Specifications and Waveforms



## Section 2 Contents

Low Voltage Logic Ratings, Specifications and Waveforms .....	2-3
Definition of Terms .....	2-3
Characterization Philosophy .....	2-4
Power Dissipation—Test Philosophy .....	2-4
AC Loading and Waveforms .....	2-5
Test Conditions .....	2-6
Propagation Delays, $f_{\max}$ , Set and Hold Times .....	2-7
Enable and Disable Times .....	2-7
Electrostatic Discharge .....	2-8
Low Voltage Logic Noise Characteristics .....	2-8
Extended Specifications .....	2-9
Skew Definitions and Examples .....	2-14

## Low Voltage Logic Ratings, Specifications, and Waveforms

### Definition of Terms

#### DC Characteristics

**Currents:** Positive current is defined as conventional current flow into a device. Negative current is defined as current flow out of a device. All current limits are specified as absolute values.

**Voltages:** All voltages are referenced to the ground pin. All voltage limits are specified as absolute values.

**$I_{CC}$**  The current flowing into the  $V_{CC}$  supply terminal when the device is at a quiescent state.

**$I_{CCH}$**  The current flowing into the  $V_{CC}$  supply terminal when the outputs are in the HIGH state.

**$I_{CCL}$**  The current flowing into the  $V_{CC}$  supply terminal when the outputs are in the LOW state.

**$\Delta I_{CC}$**  Additional  $I_{CC}$  due to TTL HIGH levels forced on CMOS inputs.

**$I_{CCZ}$**  The current flowing into the  $V_{CC}$  supply terminal when the outputs are disabled (high impedance).

**$I_I, I_{IN}$**  Input Current. The current flowing into or out of an input when a specified LOW or HIGH voltage is applied to that input.

**$I_{OH}$**  Output HIGH Current. The current flowing out of an output which is in the HIGH state.

**$I_{OL}$**  Output LOW Current. The current flowing into an output which is in the LOW state.

**$I_{OS}$**  Output Short Circuit Current. The current flowing out of an output in the HIGH state when that output is shorted to ground (or other specified potential).

**$I_{OZ}$**  Output OFF current. The current flowing into or out of a disabled TRI-STATE® output when a specified LOW or HIGH voltage is applied to that output.

**$I_I(\text{HOLD})$**  Input hold Current. Input current that holds the input at the previous state when the driving device goes to a high impedance state.

**$I_I(\text{OD})$**  Input over-drive current. Input current that is specified to switch a logic level which is held at previous state.

**$I_{OFF}$**  Input/Output power-off leakage current. The maximum leakage current into or out of the input/output transistors when forcing the input/output from 0V to 5.5V with  $V_{CC} = 0V$ .

**$V_{CC}$**  Supply Voltage. The range of power supply voltages over which the device is guaranteed to operate.

**$V_{JK}$**  Input Clamp Diode Voltage. The voltage on an input (=) when a specified current is pulled from that input.

**$V_{IH}$**  Input HIGH Voltage. The minimum input voltage that is recognized as a DC HIGH-level.

**$V_{IHD}$**  Dynamic Input HIGH Voltage. The minimum input voltage that is recognized as a HIGH-level during a Multiple Output Switching (MOS) operation.

**$V_{IL}$**  Input LOW Voltage. The maximum input voltage that is recognized as a DC LOW-level.

**$V_{ILD}$**  Dynamic Input LOW Voltage. The maximum input voltage that is recognized as a LOW-level during Multiple Output Switching (MOS) operation.

**$V_{OH}$**  Output HIGH Voltage. The voltage at an output conditioned HIGH with a specified output load and  $V_{CC}$  supply voltage.

**$V_{OL}$**  Output LOW Voltage. The voltage at an output conditioned LOW with a specified output load and  $V_{CC}$  supply voltage.

**$V_{OLP}$**  Maximum (peak) voltage induced on a static LOW output during switching of other outputs.

**$V_{OLV}$**  Minimum (valley) voltage induced on a static LOW output during switching of other outputs.

#### AC Characteristics

**$f_t$  Maximum Transistor Operating Frequency**—The frequency at which the gain of the transistor has dropped by three decibels.

**$f_{max}$  Toggle Frequency/Operating Frequency**—The maximum rate at which clock pulses may be applied to a sequential circuit. Above this frequency the device may cease to function.

**$t_{PLH}$  Propagation Delay Time**—The time between the specified reference points, on the input and output voltage waveforms, with the output changing from the defined LOW level to the defined HIGH level.

**$t_{PHL}$  Propagation Delay Time**—The time between the specified reference points, on the input and output voltage waveforms, with the output changing from the defined HIGH level to the defined LOW level.

**$t_W$  Pulse Width**—The time between specified amplitude points of the leading and trailing edges of a pulse.

**$t_H$  Hold Time**—The interval immediately following the active transition of the timing pulse (usually the clock pulse) or following the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its continued recognition. A negative hold time indicates that the correct logic level may be released prior to the active transition of the timing pulse and still be recognized.

**$t_s$  Setup Time**—The interval immediately preceding the active transition of the timing pulse (usually the clock pulse) or preceding the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its recognition. A negative setup time indicates that the correct logic level may be initiated sometime after the active transition of the timing pulse and still be recognized.

**$t_{PHZ}$  Output Disable Time (of a TRI-STATE Output) from HIGH Level**—The time between specified levels on the input and a voltage 0.3V below the steady state output HIGH level with the TRI-STATE output changing from the defined HIGH level to a high impedance (OFF) state.

**$t_{PLZ}$  Output Disable Time (of a TRI-STATE Output) from LOW Level**—The time between specified levels on the input and a voltage 0.3V above the steady state output LOW level with the TRI-STATE output changing from the defined LOW level to a high impedance (OFF) state.

**$t_{pZH}$  Output Enable Time (of a TRI-STATE Output) to a HIGH Level**—The time between the specified levels of the input and output voltage waveforms with the TRI-STATE output changing from a high impedance (OFF) state to a HIGH level.

**$t_{pZL}$  Output Enable Time (of a TRI-STATE Output) to a LOW Level**—The time between the specified levels of the input and output voltage waveforms with the TRI-STATE output changing from a high impedance (OFF) state to a LOW level.

**$t_{rec}$  Recovery Time**—The time between the specified level on the trailing edge of an asynchronous input control pulse and the same level on a synchronous input (clock) pulse such that the device will respond to the synchronous input.

**Multiple (Simultaneous) Output Switching Propagation Delays**—These tests are used to ensure compliance to the extended databook specifications and include active propagation delays, disable and enable times at 50 pF output load.

**Multiple Output Switching Skew**—Performance data from the Multiple Output Switching propagation delay testing is analyzed to obtain information regarding output skew of an IC.

## AC Dynamic (Noise) Characteristics

**$V_{OLP}$ ,  $V_{OLV}$ —Ground Bounce (Quiet Output Switching)**—Measured parameters with 50 pF loading relate the amount that a static conditioned output will change in voltage under multiple outputs switching condition with outputs operating in phase. They are heavily influenced by the magnitude that  $V_{CC}$  and Ground move internal to the IC.

**$V_{ILD}$ ,  $V_{IHD}$ —Dynamic Threshold**—Dynamic threshold measures the shift of an IC's input threshold due to noise generated while under multiple outputs switching condition with outputs operating in phase. This test is package and test environment sensitive.

**Input Edge Rate**—This test is performed to determine what minimum edge rate can be applied to an input and have the corresponding output transition with no abnormalities such as glitches or oscillations.

## Power

**Power-Up  $I_{CC}$  Traces**—Shows how the supply current reacts to various input conditions during power up.

**$I_{CC}$  vs  $V_{IN}$  Traces**—Traces of  $I_{CC}$  vs  $V_{IN}$  show how the supply current changes with input voltage.

**$I_{CCD}$  (Dynamic  $I_{CC}$ )**—Determines the amount of current an IC will consume at frequency.

## Capacitance

**Input/Output Capacitance ( $C_{IN}/C_{OUT}$ )**

**Power Dissipation Capacitance ( $C_{PD}$ )**

## Reliability Tests

**Latch-Up**—Testing determines if an IC is susceptible to latch-up from over-current or over-voltage stresses per MIL-STD-883 JEDEC method 17.

**Electrostatic Discharge, Human Body**—Per MIL-STD-883C and Machine model.

## Characterization Philosophy

During the National new product introduction process for logic IC's, a new low voltage IC design will undergo a rigorous characterization to baseline its performance. This data is required to correlate with simulation models, determine product specifications, compare performance to other product, provide a feedback mechanism to the fabrication process, and for customer information. National's Logic IC characterizations are designed to get as much information as possible about the product and potential customer application performance.

National's logic IC characterization methodology uses past knowledge of design performance, simulation, and process parametrics to determine what electrical parameters to characterize. Characterization samples are selected so that they have key process parametrics (e.g., Drive, Beta,  $V_{TN}$ ,  $V_{TP}$ ,  $V_{OFF}$ , etc.) which have been shown to significantly affect device electrical parameters. Data is acquired and processed using statistical analysis software. Manufacturing test limits are then set using the knowledge of variations due to fabrication, package, tester,  $V_{CC}$ , temperature, and condition. This allows product to be shipped on demand without problems or delays.

## Power Dissipation—Test Philosophy

In an effort to reduce confusion about measuring power dissipation capacitance,  $C_{PD}$ , a JEDEC standard test procedure (7A Appendix E) has been adopted which specifies the test setup for each type of device. This allows a device to be exercised in a consistent manner for the purpose of specification comparison.

The following is a list of different types of logic functions, along with the input setup conditions under which the  $C_{PD}$  was measured for each type of device. By understanding how the device was exercised during  $C_{PD}$  measurements,

## Power Dissipation—Test Philosophy (Continued)

the designer can understand whether the  $C_{PD}$  specified for that particular device reflects the total power dissipation capacitance for either the entire device or for just a certain stage of that device. For example, from the following list, it is apparent that the  $C_{PD}$  value specified for a counter reflects the internal capacitance for the entire device, since the entire device is being exercised during measurement. On the other hand, the  $C_{PD}$  value specified for an octal line driver reflects the internal capacitance for only one of eight stages, since only one input was being switched during test. Therefore the octal's overall power dissipation should be calculated for each of the eight stages, individually.

- Gates/Buffers/Line Drivers: Switch one input. Bias the remaining inputs such that one output switches.
- Latches: Switch the Enable and D inputs such that the latch toggles.
- Flip-Flops: Switch the clock pin while changing D (or bias J and K) such that the output(s) change each clock cycle. For parts with a common clock, exercise only one flip-flop.

- Decoders: Switch one address pin which changes two outputs.
- Multiplexers: Switch one address pin with the corresponding data inputs at opposite logic levels so that the output switches.
- Counters: Switch the clock pin with other inputs biased such that the device counts.
- Shift Registers: Switch the clock pin with other inputs biased such that the device shifts.
- Transceivers: Switch one data input. For bidirectional devices enable only one direction.
- Parity Generator: Switch one input.
- Priority Encoders: Switch the lowest priority input.

## AC Loading and Waveforms

### LOADING CIRCUIT

Figure 1 shows the AC test circuit used in characterizing and specifying propagation delays for all of the low voltage logic devices as shown, unless otherwise specified in the data sheet of a specific device.

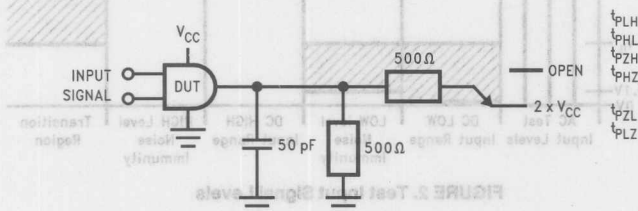


FIGURE 1a. AC Test Circuit for LVQ, LVX Translator Families

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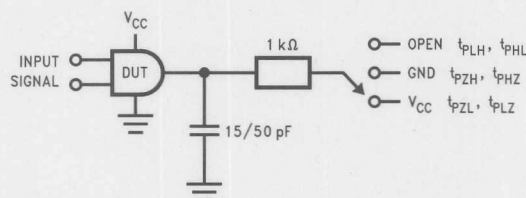


FIGURE 1b. AC Test Circuit for LVX Family

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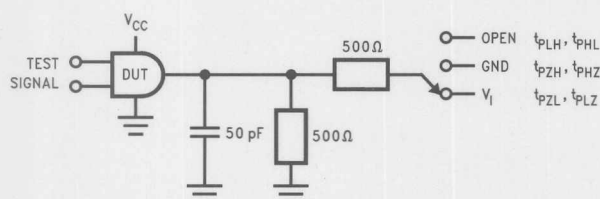


FIGURE 1c. AC Test Circuit for LCX, LVT, LVX Bus Switch Families

TL/F/12010-25

Family	$V_I$
LCX	6V
LVT	6V
LVX Bus SW	7V

## Test Conditions

Figure 2 describes the input signal voltage levels to be used when testing low voltage logic circuits. The AC test conditions follow industry convention requiring  $V_{IN}$  to range from 0V to  $V_{CC}$ . The DC parameters are normally tested with  $V_{IN}$  at guaranteed input levels, that is  $V_{IH}$  to  $V_{IL}$  (see data tables for details). Care must be taken to adequately decouple these high performance parts and to protect the test signals from electrical noise. In an electrically noisy environment, (e.g., a tester and handler not specifically designed for high speed work), DC input levels may need to be adjusted to increase the noise margin to allow for the extra noise in the tester which would not be seen in a system.

Noise immunity testing is performed by raising  $V_{IN}$  to the nominal supply voltage of 3.3V then dropping it to a level corresponding to  $V_{IH}$  characteristics, and then raising it again to the 3.3V level. Noise tests can also be performed on the  $V_{IL}$  characteristics by raising  $V_{IN}$  from 0V to  $V_{IL}$ , then returning to 0V. Both  $V_{IH}$  and  $V_{IL}$  noise immunity tests should not induce a switch condition on the appropriate outputs.

Good high frequency wiring practices should be used in constructing test jigs. Leads on the load capacitor should be as short as possible to minimize ripples on the output waveform transitions and to minimize undershoot. Generous ground metal (preferably a ground plane) should be used for the same reasons. A  $V_{CC}$  bypass capacitor should be provided at the test socket, also with minimum lead lengths.

### AC Loading and Waveforms

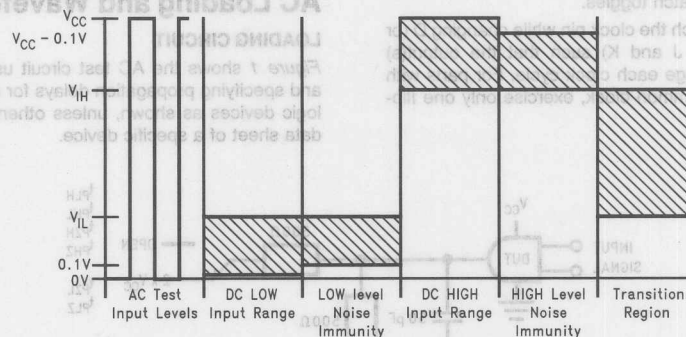


FIGURE 2. Test Input Signal Levels

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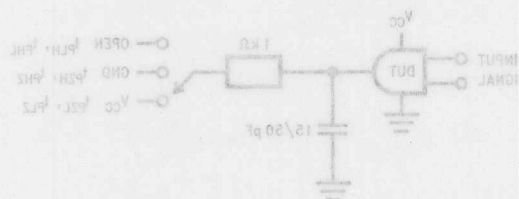
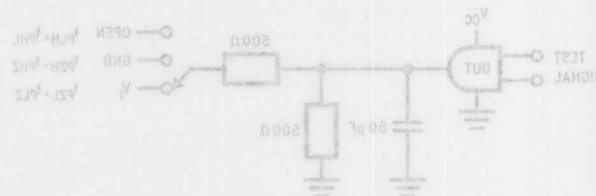


FIGURE 1b. AC Test Circuit for LVC, LVT, and LVT+ Families

Family	$V_I$
LVC	8V
LVT	8V
LVT Bus SW	7V

TL/F/12010-2a

FIGURE 1c. AC Test Circuit for LVC, LVT, LVT Bus Switch Families



## Propagation Delays, $f_{max}$ , Set and Hold Times

A 1.0 MHz square wave is recommended for most propagation delay tests. The repetition rate must necessarily be increased for testing  $f_{max}$ . A 50% duty cycle should always be used when testing  $f_{max}$ . Two pulse generators are usually required for testing such parameters as setup time, hold time, recovery time, etc. See Figures 3 and 4.

## Enable and Disable Times

Figures 5 and 6 show that the disable times are measured at the point where the output voltage has risen or fallen by 0.3V from  $V_{OL}$  or  $V_{OH}$ , respectively. This change enhances the repeatability of measurements, and gives the system

designer more realistic delay times to use in calculating minimum cycle times. Since the high impedance state rising or falling waveform is RC-controlled, the first 0.3V of change is more linear and is less susceptible to external influences. More importantly, perhaps from the system designer's point of view, a change in voltage of 0.3V is adequate to ensure that a device output has turned OFF. Measuring to a larger change in voltage merely exaggerates the apparent Disable times and thus penalizes system performance since the designer must use the Enable and Disable times to devise worst case timing signals to ensure that the output of one device is disabled before that of another device is enabled. Note that the measurement points have been changed from the 10% and 90% points. This better reflects actual test points and does not change specification limits.

## Waveforms

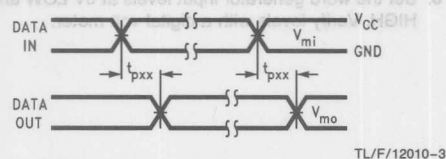


FIGURE 3. Waveform for Inverting and Non-Inverting Functions

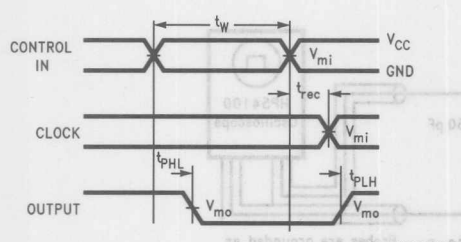


FIGURE 4. Propagation Delay, Pulse Width and  $t_{rec}$  Waveforms

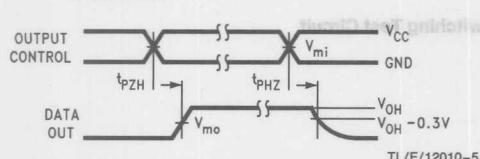


FIGURE 5. TRI-STATE Output High Enable and Disable Times for Low Voltage Logic

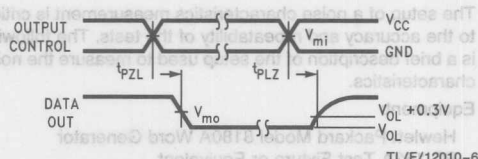


FIGURE 6. TRI-STATE Output Low Enable and Disable Times for Low Voltage Logic

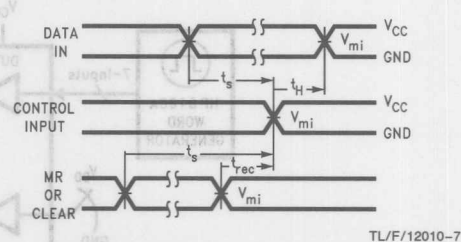


FIGURE 7. Setup Time, Hold Time and Recovery Time for Low Voltage Logic

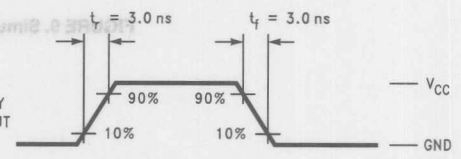


FIGURE 8.  $t_{rise}$  and  $t_{fall}$

	$V_{mi}$	$V_{mo}$
LVQ	50% $V_{CC}$	50% $V_{CC}$
LVX	50% $V_{CC}$	50% $V_{CC}$
LVXX	50% $V_{CC}^*$	50% $V_{CC}$
LCX	1.5V	1.5V
LVT	1.5V	1.5V

\*1.5V for TTL Compatible

## Electrostatic Discharge

Precautions should be taken to prevent damage to devices by electrostatic discharge. Static charge tends to accumulate on insulated surfaces such as synthetic fabrics or carpeting, plastic sheets, trays, foam, tubes or bags, and on ungrounded electrical tools or appliances. The problem is much worse in a dry atmosphere. In general, it is recommended that individuals take the precaution of touching a known ground before handling devices. To effectively avoid electrostatic damage to low voltage logic devices, it is recommended that individuals wear a grounded wrist strap when handling devices. More often, handling equipment, which is not properly grounded, causes damage to parts. Ensure that all parts of the tester, which are near the device, are conductive and connected to ground.

## Noise Characteristics

The setup of a noise characteristics measurement is critical to the accuracy and repeatability of the tests. The following is a brief description of the setup used to measure the noise characteristics.

### Equipment:

- Hewlett Packard Model 8180A Word Generator
- PC-163A Test Fixture or Equivalent
- HP54100 Oscilloscope or Equivalent

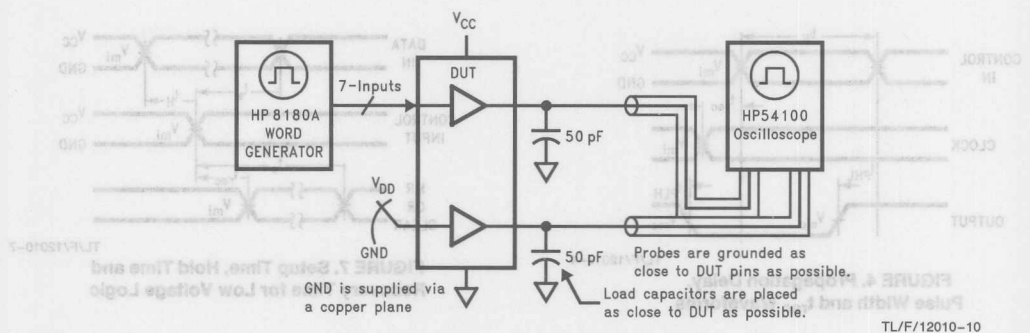


FIGURE 9. Simultaneous Switching Test Circuit

### Procedure:

1. Verify Test Fixture Loading: Standard Load 50 pF.
2. Deskew the word generator so that no two channels have greater than 150 ps skew between them. This requires that the oscilloscope be deskewed first. Swap out the channels that have more than 150 ps of skew until all channels being used are within 150 ps. It is important to deskew the word generator channels before testing. This will ensure that the outputs switch simultaneously.
3. Terminate all inputs and outputs to ensure proper loading of the outputs and that the input levels are at the correct voltage.
4. Set  $V_{CC}$  to 3.3V.
5. Set the word generator to toggle all but one output at a frequency of 1 MHz. Greater frequencies will increase DUT heating and affect the results of the measurement.
6. Set the word generator input levels at 0V LOW and 3.3V HIGH. Verify levels with a digital volt meter.

## Noise Characteristics (Continued)

The concern for the system designer evolves from the possibility that the quiet output voltage shift could impact the logic threshold. Values on some product families peak about the peak of the time the voltage shift occurs in the opposite state is short, in the neighborhood of 10-100 ps, and may not disturb sequential circuitry if it is level sensing. If the affected circuit is a timing edge, such as a clock input, the sequence may take the inadvertent de-assertion and interpret it as a logic 1, providing the QOS specification to assist in noise margin planning.

ACTIVE  
OUTPUTS  
  
QUIET  
OUTPUT  
UNDER TEST

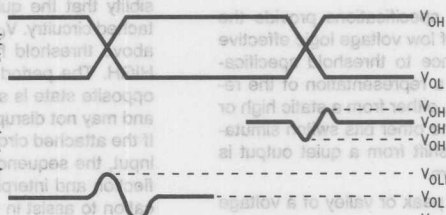


FIGURE 10. Quiet Output Noise Voltage Waveforms

Note 1:  $V_{OHV}$  and  $V_{OLP}$  are measured with respect to ground reference.

Note 2: Input pulses have the following characteristics:  $f = 1 \text{ MHz}$ ,  $t_r = 3 \text{ ns}$ ,  $t_f = 3 \text{ ns}$ , skew  $< 150 \text{ ps}$ .

$V_{OLP}/V_{OLV}$  and  $V_{OHP}/V_{OHV}$ :

- Determine the quiet output pin that demonstrates the greatest noise levels. The worst case pin will usually be the furthest from the ground pin. Monitor the output voltages using a 10 k $\Omega$  scope probe plugged into a standard SMB type connector on the test fixture.
- Measure  $V_{OLP}$  and  $V_{OLV}$  on the quiet output LOW during the HL transition. Measure  $V_{OHP}$  and  $V_{OHV}$  on the quiet output HIGH during the LH transition.
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.

$V_{ILD}$  and  $V_{IHD}$ :

- Monitor one of the switching outputs using a 10 k $\Omega$  scope probe plugged into a standard SMB type connector on the test fixture.
- First increase the input LOW voltage level,  $V_{IL}$ , until the output begins to oscillate. Oscillation is defined as noise on the output LOW level that exceeds  $V_{IL}$  limits, or on output HIGH levels that exceed  $V_{IH}$  limits. The input LOW voltage level at which oscillation occurs is defined as  $V_{ILD}$ .
- Next decrease the input HIGH voltage level on the word generator,  $V_{IH}$  until the output begins to oscillate. Oscillation is defined as noise on the output low level that exceeds  $V_{IL}$  limits, or on output HIGH levels that exceed  $V_{IH}$  limits. The input HIGH voltage level at which oscillation occurs is defined as  $V_{IHD}$ .
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.

## Extended Specifications

National has taken new steps in aiding the system designer with a better method to predict device performance in his application. National now offers system oriented performance specifications so a designer can feel confident in the way a device will perform over a wider variety of switching conditions. Performance specifications in the form of Extended Specifications are provided with each product data-sheet.

## Extended Specifications (Continued)

### QUIET OUTPUT SWITCHING

Quiet output switching (QOS) is a new specification that system designer up until now has not had. It is a specification that control to noise and performance to threshold specifications. The QOS specification is a representation of the low level on a single bit, while the output is in a quiet state. The voltage level on a single bit, while the output is in a quiet state, is specified through four parameters:  $V_{OLP}$ ,  $V_{OLV}$ ,  $V_{OHP}$ , and  $V_{OHV}$ .  $V_{OLP}$  and  $V_{OLV}$  describe the low level on a quiet output.  $V_{OHP}$  and  $V_{OHV}$  describe the high level on a quiet output.

In the past, most extended databook specifications depended on a representative product family function to provide the guaranteed performance data for the rest of the family. The drawback from this method of test and specmanship leaves rather large process, tester and function guardbands in the final maximum or minimum specifications. The test data for National's low voltage logic product family, taken during product development on each function, provides the low voltage logic family with device specific and guaranteed extended specifications that can be passed directly to the system designers. National offers the extended specifications with the belief that customers can reduce their incoming test requirements and in essence reduce the cost and time for product design-in.

Additional specifications provided by National include: Quiet Output Switching (QOS)  $V_{OLP}$ ,  $V_{OLV}$ , and Dynamic Threshold (DVTH),  $V_{ILD}$ , and  $V_{IHD}$ .

Each of the guaranteed extended specifications involve multiple output switching events. During a multiple output switching event, stray inductance and capacitance inhibit product performance. National has developed standardized hardware that aligns with the industry for low voltage logic product evaluations. Some of the features of the test fixturing include ground planes and low inductive connections, critical in evaluating the product and not the fixture.

The extended specification tests have very similar if not identical test setups. The results of the measurements from each test depend on the application focus. The quantitative analysis from the tests provides insight into product performance. The parameters and typical results from each test type can be easily explained in the sections that follow.

TABLE I. Test Conditions for QOS, DVTH

Parameter	Value
Input Edge Rate	2.5 ns
Input Skew	$< 300 \text{ pS}$
Input Amplitude	0V to 3.0V
Input Frequency	1 MHz
Output Load	50 pF

## Extended Specifications (Continued)

### QUIET OUTPUT SWITCHING

Quiet output switching, (QOS), specifications provide the system designer quantification of low voltage logic effective control of noise and performance to threshold specifications. The QOS specification is a representation of the resultant shift of an output voltage, either from a static high or low level on a single bit, while the other bits switch simultaneously in phase. The voltage shift from a quiet output is specified through four parameters.

- $V_{OLP}$  and  $V_{OLV}$  describe the peak or valley of a voltage shift from a quiet output low level.
- $V_{OHP}$  and  $V_{OHV}$  describe the peak or valley of a voltage shift from a quiet output high level.

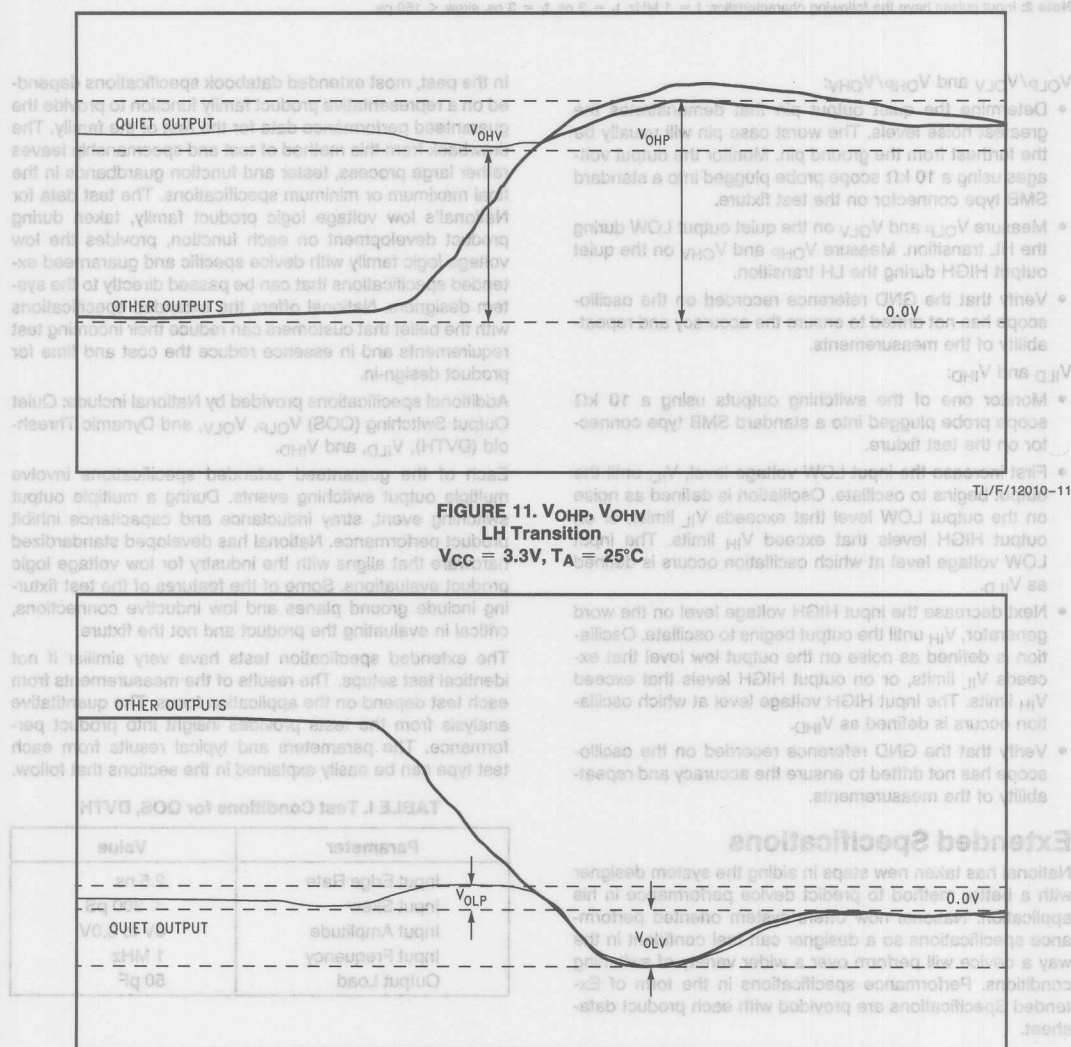


FIGURE 11.  $V_{OHP}$ ,  $V_{OHV}$  LH Transition  
 $V_{CC} = 3.3V$ ,  $T_A = 25^\circ C$

FIGURE 12.  $V_{OLP}$ ,  $V_{OLV}$  HL Transition  
 $V_{CC} = 3.3V$ ,  $T_A = 25^\circ C$

The concern for the system designer evolves from the possibility that the quiet output voltage shift could impact attached circuitry.  $V_{OLP}$  values on some product families peak above threshold high and become recognized as a logic HIGH. The period of time the voltage shift spends in the opposite state is short, in the neighborhood of 10–100 pS, and may not disrupt sequential circuitry if it is level sensing. If the attached circuitry needs a rising edge, such as a clock input, the sequential circuitry may take the inadvertent deflection and interpret it. National provides the QOS specification to assist in noise margin planning.

- Detail the test conditions that determine the worst case pin voltage levels. The worst case pin voltage levels are determined by the test conditions. The test conditions are specified in the test data.
- Measure  $V_{OLP}$  and  $V_{OLV}$  on the quiet output LOW during the LH transition. Measure  $V_{OHP}$  and  $V_{OHV}$  on the quiet output HIGH during the LH transition.
- Verify that the GND reference recorded on the oscilloscope is not shifted relative to the measurements.
- Monitor one of the switching outputs using a 10 k $\Omega$  scope probe plugged into a standard SMB type connector on the test fixture.
- First, measure the input LOW voltage level at which oscillation occurs. Oscillation is defined as noise on the output LOW level that exceeds  $V_{IL}$  limit. The input LOW voltage level at which oscillation occurs is as  $V_{IL}$ .
- Next, decrease the input HIGH voltage level on the word generator.  $V_{IH}$  until the output begins to oscillate. Oscillation is defined as noise on the output high level that exceeds  $V_{IH}$  limit. The input HIGH voltage level at which oscillation occurs is defined as  $V_{IH}$ .
- Verify that the GND reference recorded on the oscilloscope has not shifted to ensure the accuracy and repeatability of the measurements.

TL/F/12010-12

# Extended Specifications (Continued)

## DYNAMIC THRESHOLD

Dynamic threshold data, (DVTH), like QOS data, provides the system designer with noise performance criteria. DVTH specifications quantify the magnitude of output voltage deflection that a logic high or low might experience under a multiple output switching condition. The voltage deflection is a result of an apparent shift of an input's threshold due to noise generated from MOS switching on the internal die ground and  $V_{CC}$  busses. The phenomenon occurs during any logic state transition: LH, HL, ZL, etc. As a practice, National determines the worse case transition for each product and generates the specification based on that transition.

Dynamic threshold specifications are denoted by the nomenclature,  $V_{ILD}$  and  $V_{IHD}$ , where the "D" represents "Dynamic". The definitions for each are as follows,

- $V_{ILD}$  - The maximum LOW input level such that normal switching/functional characteristics are observed on the output
- $V_{IHD}$  - The minimum HIGH input level such that normal switching/functional characteristics are observed on the output

Dynamic threshold failures are bundled into five main failure modes. The most predominant failure is an output deflection in violation of an input threshold level. Others include propagation delay step out in excess of an MOS propagation delay specification, state changes and oscillations. A detailed definition of each failure can be described as follows,

1. On a low output, the LOW level will not rise above an input threshold low level of 0.8V after the transition of the output. *Figures 13 and 14.* Numbered output curve deflections are a result of 10 mV incremental changes on the low input signal level.

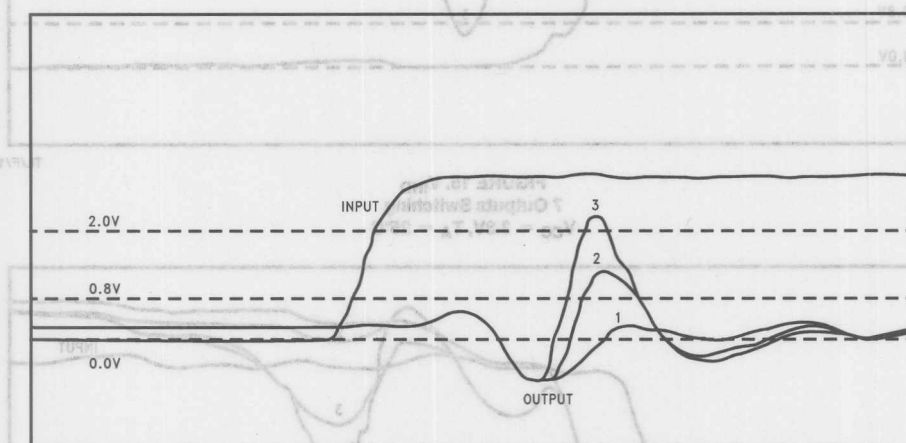


FIGURE 13.  $V_{ILD}$  7 Outputs Switching  
 $V_{CC} = 3.3V, T_A = 25^{\circ}C$

TL/F/12010-13

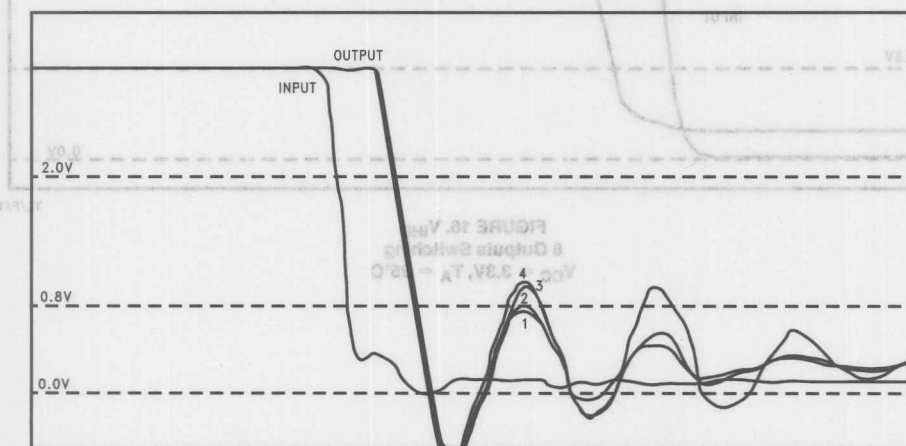
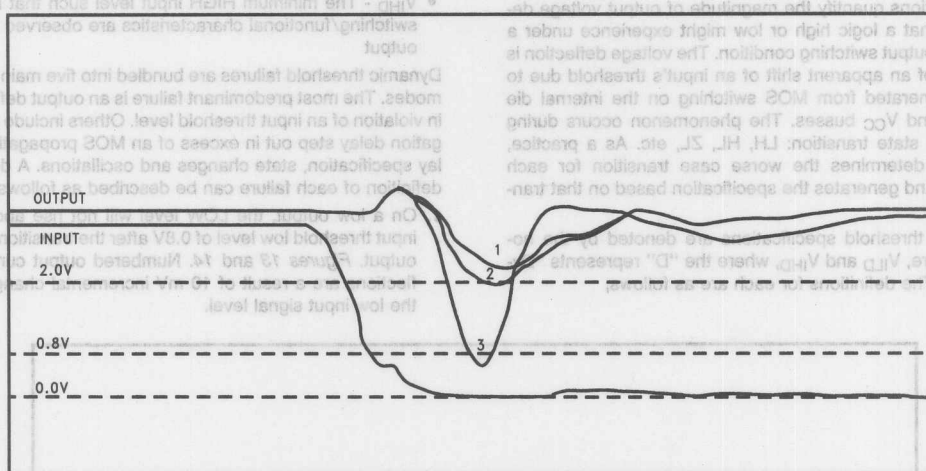


FIGURE 14.  $V_{ILD}$  8 Outputs Switching  
 $V_{CC} = 3.3V, T_A = 25^{\circ}C$

TL/F/12010-14

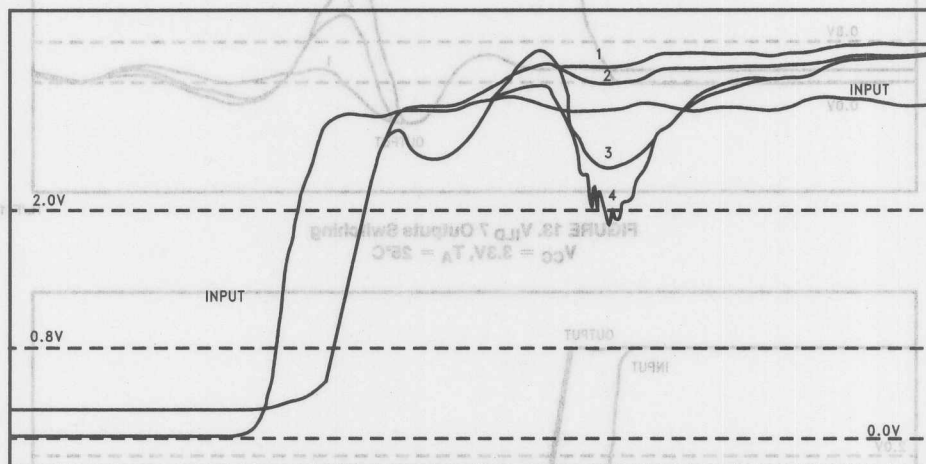
## Extended Specifications (Continued)

2. On a high output, the HIGH level will not drop below an input threshold high level of 2.0V after the transition of the output. Figures 15 and 16. Numbered output curve deflections are a result of 10 mV incremental changes on the high input signal level.



**FIGURE 15.  $V_{IH}$   
7 Outputs Switching  
 $V_{CC} = 3.3V$ ,  $T_A = 25^\circ C$**

TL/F/12010-15



**FIGURE 16.  $V_{IH}$   
8 Outputs Switching  
 $V_{CC} = 3.3V$ ,  $T_A = 25^\circ C$**

TL/F/12010-16

## Extended Specifications (Continued)

3. If the natural ringing, other than the initial bounce, of the output violates an input threshold level, the starting voltage level is noted and monitored until a 100 mV amplitude change towards threshold. If no amplitude change occurs, then the next peak or valley on the output is monitored for input threshold violation. *Figure 17.*

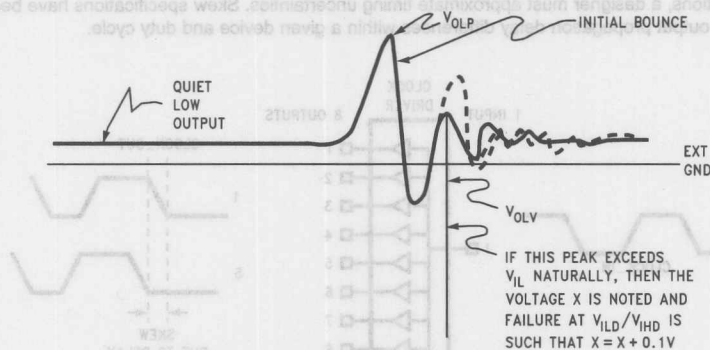


FIGURE 17

TL/F/12010-17

SOURCES OF CLOCK SKEW  
Total system clock skew includes intrinsic and extrinsic skew. Intrinsic skew is defined as the difference in delays between the outputs of devices. Extrinsic skew is defined as the difference in trace delays and loading conditions.

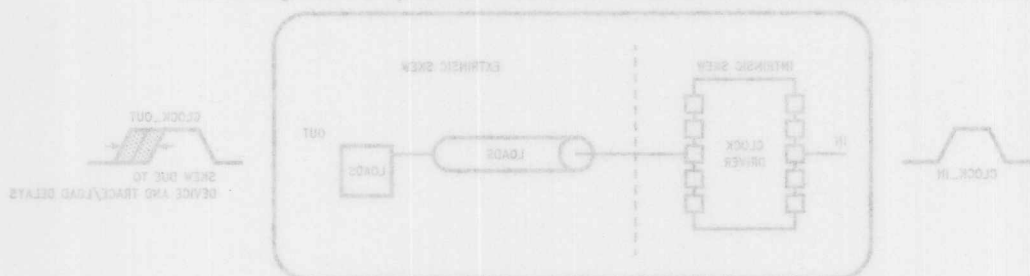


FIGURE 18. Sources of Clock Skew

Example: 50 MHz Clock signal distribution on a PC Board.

50 MHz signal produces 20 ns clock cycles	
Total system skew budget = 10% of clock cycle = 2 ns	→
Intrinsic skew = 1 ns	→
Device skew (intrinsic skew) must be less than 1 ns	→
1 ns	→
2 ns	→

\* Clock Design Rule of thumb

## Skew Definitions and Examples

Minimizing output skew is a key design criteria in today's high-speed clocking schemes, and National has incorporated skew specifications into low Voltage devices. This section provides general definitions and examples of skew.

### CLOCK SKEW

Skew is the variation of propagation delay differences between output clock signal(s). See *Figure 18*.

#### Example:

If signal appears at output #1 in 3 ns and in 4 ns at output #5, the skew is 1 ns.

Without skew specifications, a designer must approximate timing uncertainties. Skew specifications have been created to help clock designers define output propagation delay differences within a given device and duty cycle.

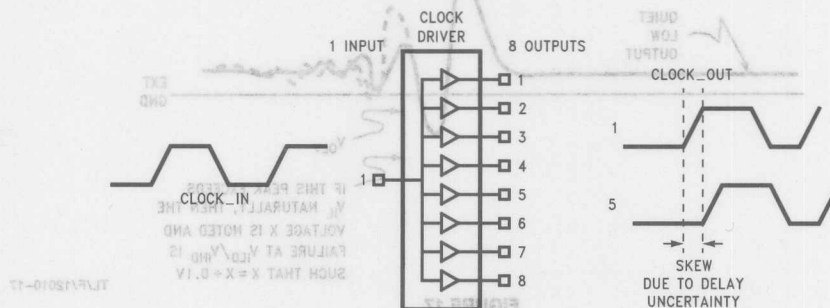


FIGURE 18. Clock Output Skew

TL/F/12010-18

### SOURCES OF CLOCK SKEW

Total system clock skew includes intrinsic and extrinsic skew. Intrinsic skew is defined as the differences in delays between the outputs of device(s). Extrinsic skew is defined as the differences in trace delays and loading conditions.

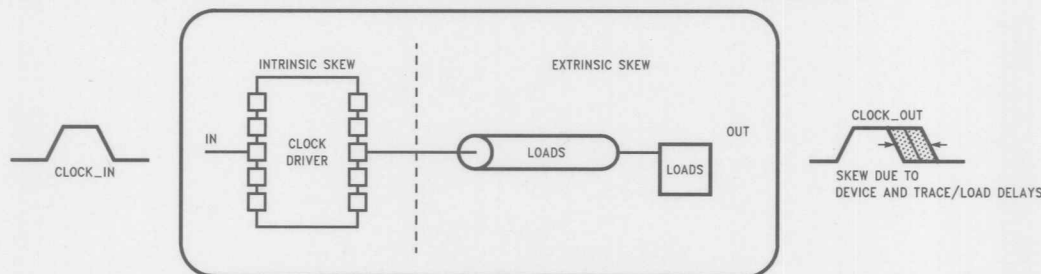


FIGURE 19. Sources of Clock Skew

TL/F/12010-19

**Example:** 50 MHz Clock signal distribution on a PC Board.

50 MHz signals produces 20 ns clock cycles

Total system skew budget = 10% of clock cycle\* = 2 ns → 2 ns

If extrinsic skew = 1 ns → 1 ns

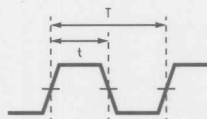
Device skew (intrinsic skew) must be less than 1 ns! ← 1 ns

\*Clock Design Rule of thumb.

## Skew Definitions and Examples (Continued)

### CLOCK DUTY CYCLE

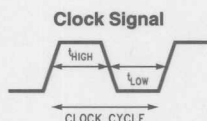
- Clock Duty Cycle is a measure of the amount of time a signal is *HIGH* or *LOW* in a given clock cycle.



TL/F/12010-20

$$\text{Duty Cycle} = t/T \cdot 100\%$$

FIGURE 20. Duty Cycle Calculation



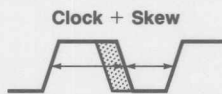
TL/F/12010-21

FIGURE 21. Clock Cycle

#### Example:

$t_{\text{HIGH}}$  and  $t_{\text{LOW}}$  are each 50% of the clock cycle therefore the clock signal has a Duty Cycle of 50/50%.

- Clock skew effects the Duty Cycle of a signal.



TL/F/12010-22

FIGURE 22. Clock Skew

#### Example: 50 MHz clock distribution on a PC board.

Skew must be guaranteed less than 1 ns at 50 MHz to achieve 55/45% Duty Cycle requirements of core silicon!

TABLE II

System Frequency	Skew	$t_{\text{HIGH}}$	$t_{\text{LOW}}$	Duty Cycle	
50 MHz	0 ns	10 ns	10 ns	50/50%	← Ideal Duty Cycle (50/50%) occurs for zero skew.
50 MHz	2 ns	12 ns	8 ns	60/40%	
50 MHz	1 ns	11 ns	9 ns	55/45%	
33 MHz	2 ns	17 ns	15 ns	55/45%	← Note that at lower frequencies, the skew budget is not as tight and skew does not effect the Duty Cycle as severely as seen at higher frequencies.

## Definition of Parameters

### $t_{\text{OSLH}}$ , $t_{\text{OSHL}}$ (Common Edge Skew)

$t_{\text{OSLH}}$  and  $t_{\text{OSHL}}$  are parameters which describe the delay from one driver to another on the same chip. This specification is the worst-case number of the delta between the fastest to the slowest path on the same chip. An example of where this parameter is critical is the case of the cache controller and the CPU, where both units use the same transition of the clock. In order for the CPU and the controller to be synchronized,  $t_{\text{OSLH/HL}}$  needs to be minimized.

#### Definition

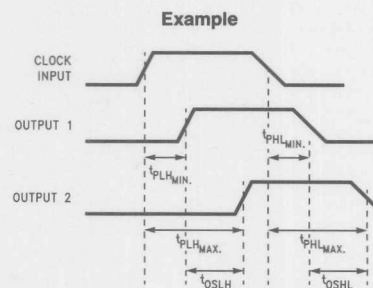
$t_{\text{OSLH}}$ ,  $t_{\text{OSHL}}$  (Output Skew for High-to-Low Transitions):

$$t_{\text{OSHL}} = |t_{\text{PHLMAX}} - t_{\text{PHLMIN}}|$$

Output Skew for Low-to-High Transitions:

$$t_{\text{OSLH}} = |t_{\text{PLHMAX}} - t_{\text{PLHMIN}}|$$

Propagation delays are measured across the outputs of any given device.



TL/F/12010-23

FIGURE 23.  $t_{\text{OSLH}}$ ,  $t_{\text{OSHL}}$

## Skew Definitions and Examples (Continued)

### CLOCK DUTY CYCLE

- Clock Duty Cycle is a measure of the amount of time a signal is HIGH or LOW in a given clock cycle.



TLV112010-20

$$\text{Duty Cycle} = t_H \cdot 100\%$$

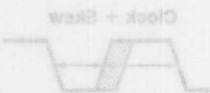
FIGURE 20. Duty Cycle Calculation



TLV112010-21

FIGURE 21. Clock Cycle

- Clock skew effects the Duty Cycle of a signal.



TLV112010-22

FIGURE 22. Clock Skew

Example: 50 MHz clock distribution on a PC board. Skew must be guaranteed less than 1 ns at 50 MHz to achieve 50% Duty Cycle requirements of core silicon.

Example: 50 MHz clock distribution on a PC board. Skew must be guaranteed less than 1 ns at 50 MHz to achieve 50% Duty Cycle requirements of core silicon.

TABLE II

System Frequency	Skew	High	Low	Duty Cycle
30 MHz	0 ns	10 ns	10 ns	50% (50% duty cycle occurs for zero skew.)
50 MHz	2 ns	15 ns	8 ns	50% (50% duty cycle occurs for zero skew.)
50 MHz	1 ns	11 ns	8 ns	50% (50% duty cycle occurs for zero skew.)
33 MHz	2 ns	17 ns	15 ns	50% (50% duty cycle occurs for zero skew.)

Note that at lower frequencies, the skew budget is not as tight and skew does not effect the Duty Cycle as severely as seen at higher frequencies.

## Definition of Parameters

### tsuH (Common Edge Skew)

tsuH and tsuL are parameters which describe the delay from one driver to another on the same chip. This specification is the worst-case number of the delay between the fastest to the slowest path on the same chip. An example of where this parameter is critical is the case of the cache controller and the CPU, where both units use the same transition of the clock. In order for the CPU and the controller to be synchronized, tsuH needs to be minimized.

### Definition

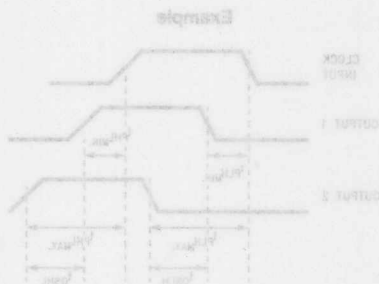
tsuH (Output Skew for High-to-Low Transitions):

$$tsuH = t_{PLHMAX} - t_{PLHMIN}$$

Output Skew for Low-to-High Transitions:

$$tsuL = t_{PLHMAX} - t_{PLHMIN}$$

Propagation delays are measured across the output of any given device.



TLV112010-23

FIGURE 23. tsuH, tsuL



## Section 3 Contents

3-3	Quality and Reliability .....
3-3	Introduction .....
3-3	Qualification Requirements for Logic Integrated Circuits .....
3-4	Quality Information and Communication (QUIC) System .....
3-4	Water Level Reliability (WLR) .....
3-5	Electrostatic Discharge (ESD) Sensitivity .....
3-5	Repeatability of Human Body Model (HBM) ESD Results .....
3-6	Power Sensitivities for Minimum Geometry Products .....
3-6	Latchup Testing .....

## Section 3 Quality and Reliability



### Section 3 Contents

Quality and Reliability .....	3-3
Introduction.....	3-3
Qualification Requirements for Logic Integrated Circuits .....	3-3
Quality Information and Communication (QUIC) System .....	3-4
Wafer Level Reliability (WLR) .....	3-4
Electrostatic Discharge (ESD) Sensitivity .....	3-5
Repeatability of Human Body Model (HBM) ESD Results .....	3-5
Power Sensitivities for Minimum Geometry Products .....	3-6
Latchup Testing .....	3-6

## Quality and Reliability

### Introduction

Product qualification is a disciplined, team activity which focuses on demonstrating, through the acquisition and analysis of engineering data, that a device design, fab process, or package design meets or exceeds minimum standards of performance. In most cases, this involves running samples of product through a series of tests which expose the samples to operating stresses far in excess of those which would be encountered in even the most severe "real life" operating environment. These tests are called either accelerated stress tests or accelerated life tests. A properly designed qualification test sequence exposes, within a matter of days or weeks, those design, materials, or workmanship defects which would lead to device failure in the customer's application after months or even years of operation.

In order to be considered a "world class" supplier of semiconductor devices, NSC designs and manufactures products which are capable of meeting the reliability expectations of its most demanding customers. While customer requirements and expectations vary on the subject of reliability requirements for devices, virtually all large users have general procurement specifications which establish failure rate goals or objectives for the suppliers of the components used in their products.

Failure rate goals for infant mortality and long-term-failure-rate-in-service have been established for all NSC product lines. These goals are published internally at the beginning of each fiscal half-year (usually June and December). The actual performance of the product against these goals is measured monthly using life test data gathered from various sources including the Fast Reaction and Long Term Audit Program. Performance is reviewed every six (6) months by Reliability and Product Group management and adjusted as necessary to reflect customer expectations, competitive data, and/or historical performance trends.

Given that product reliability is an overriding corporate objective, and that any deficiency in design, materials, procedures, or workmanship, has a potential for adversely affecting the reliability of the product, Manufacturing and Engineering organizations within NSC, its subsidiaries, and its sub-contractors, involved in introducing a new device, process, or package, share a joint responsibility for demonstrating that the product does conform to NSC standards and to the standards and expectations of NSC's customers.

As a matter of policy, it is NSC's goal to design and manufacture product that is 100% defect-free and capable of surviving the qualification tests with zero failures. This policy is not interpreted as a directive to abandon a qualification pro-

## Quality Information and Communication (QUIC) System

**BACKGROUND**  
National's Quality Assurance Systems Development Group (QASD) maintains a variety of data tracking systems such as: Electronic Reliability Data Management (ERDM), Analysis (FA), Burn-In Board Inventory, and a number of others.

QUIC users will find a user friendly, menu-driven, real-time system that gives them a simultaneous-user environment with timely data inputs from sites around the world. QUIC is program when failures occur or to delay new product releases until perfection has been achieved. Rather, the policy is intended to focus engineering resources on the identification and elimination of the design, process, or workmanship deficiencies that are the root causes of the failures and then to engineer a solution to correct those deficiencies.

Specific family qualification data is available and may be obtained by calling our customer response center at 1-800-272-9959 within the US, 1-800-258-6768 in Canada.

### Qualification Requirements for Logic Integrated Circuits

Test	Test Method	Test/Stress Conditions	Sample Size Each Lot
Operating Life	SOP-5-049-RA Method 107	1000 Hours @T <sub>A</sub> = 125°C	77
High Temperature Storage	SOP-5-049-RA Method 103	1000 Hours @150°C	45
Temperature Cycle	SOP-5-049-RA Method 105	1000 Cycles -65°C to +150°C	77
Temperature Cycle with Preconditioning	SOP-5-049-RA Method 105	1000 Cycles -65°C to +150°C	77
Temperature-Humidity-Bias	SOP-5-049-RA Method 104	1000 Hours 85°C @ 85%RH	77
Temperature-Humidity-Bias with Preconditioning	Method 112 Method 104	Precondition plus 100 hours 85°C to 85%RH	77
Autoclave	Method 101	500 hours 121°C @ 15 psig	45
Thermal Shock	Method 106	100 Cycles -65°C to +150°C	22
Salt Atmosphere	Method 209	25 Hours 35°C	22
Resistance to Solvents	Method 207	4 Solvents	3 Each Solvent
Lead Integrity	Method 205	Condition as Appropriate to Package	22 Leads
Solderability	Method 203	8 Hour Steam 5 secs @260°C	22
Solder Heat	Method 204	12 secs 260°C	22

## Quality Information and Communication (QUIC) System

### BACKGROUND

National's Quality Assurance Systems Development group (QASD) maintains a variety of data tracking systems such as: Electronic Reliability Data Management (ERDM), Failure Analysis (F/A), Burn-in Board Inventory, and a number of others.

QUIC users will find a user friendly, menu-driven, real-time system that gives them a simultaneous-user environment with timely data inputs from sites around the world. QUIC is programmed to recognize each individual user of the system at the point of logging on to the mainframe, and provides an appropriate list of menu options consistent with the user's level of access requirements.

National grants access to QUIC by customers that provides a sufficient level of security over the entire system, thus precluding the possibility of accidental access (or even damage) to various files.

### HOW A CUSTOMER LINKS TO QUIC

1. Check to make sure you have the hardware components listed below. (An attached printer is desirable but not imperative.)  
IBM/PC compatible computer with at least 128k memory.  
Hayes compatible 1200 baud modem (or 2400, 4800 or 9600).  
Touch tone phone.
2. Request access to QUIC by contacting your National sales representative or Customer Service Center at 1-800-272-9959, who will coordinate all activities necessary to provide access for your company and arrange training (usually handled over the telephone).
3. Identify the person who will be your company's main contact and user of the QUIC system. This person will assume responsibility for the USERID assigned to your company and will receive training on how to access and use the QUIC system.
4. National will provide a USERID, password and account number with appropriate menus and a communications software package called EXECULINK, which allows the customer's PC to talk with NSC's host computer and also turns the PC into a virtual host terminal, with full-screen editing capability and full use of program function (PF) keys. EXECULINK also provides for file transferring between host and PC and spooling of print files to a PC-attached printer.

### ONGOING IMPROVEMENTS

As we receive feedback from the users of QUIC, we (QASD) will continue to enhance the "User Friendliness" of the system and add new features which, we hope, will help promote a true sense of teamwork between us and our customers.

## Wafer Level Reliability (WLR)

### BACKGROUND

The conventional methods of reliability screening, that of short-term burn-in to eliminate infant mortalities and long-term life tests at high temperature, will soon become impractical for many devices. The reasons for this are tighter infant mortality ppm requirements, higher costs, and shortened lifetimes.

As device complexity increases, the testing sample size required to ensure infant mortality ppm levels in the 0-10 ppm range will quickly deplete reliability test capacity. While burn-in eliminates inferior devices, it can also substantially shorten the lifetimes of "good" devices to an unacceptable level, creating an expensive and somewhat risky procedure. New technology advances which minimize geometry, have moved our device lifetime distributions closer to our customer's expected system life. As device geometries shrink, resulting in higher current densities, electric fields, and chip temperatures, tighter fab process control and instant feedback become critical.

### THE GOAL OF WAFER-LEVEL-RELIABILITY TESTING-PROCESS RELIABILITY

Wafer-level-reliability testing represents a proactive, correlation and control approach to ensuring device reliability. WLR is not meant to replace classical reliability testing. Instead it is used to supplement existing methods.

WLR testing is used to:

1. Identify shifts in On-Line Process Controls (fab monitors) which affect product reliability.
2. Reduce process qualification cycle time.
3. Improve process qualification success rate.
4. Assess reliability trends of production processes.
5. Quantify the reliability impact of process modifications.

WLR provides faster feedback for fab process control. The collection of WLR test data during and at the end of wafer fab processing provide a reliability baseline for each of our fab processes. Shifts in WLR test results, whether intentional (a process change or qualification) or unintentional (a process control problem), signal an increase or decrease in product reliability risk. WLR monitoring of production processes using Statistical Quality Control (SQC) techniques provides engineering with the information required to find and fix process control problems faster, and to determine the effectiveness of on-line process controls from a reliability standpoint. In this way, WLR testing is used to link on-line process controls to the traditional accelerated life testing methods.

### NATIONAL'S WLR PROGRAM

National developed a corporate-wide WLR program which continues to implement powerful, new test techniques. WLR testing has been used effectively to help understand how process variability affects product reliability. It is also used to help build-in reliability at the design stage for new process technologies such as those used by the Low Voltage logic families.

WLR tests and test structures have been designed to increase the likelihood and predict a rate of a reliability failure mechanism occurrence. In addition, National has developed a partnership with a leading parametric test system supplier. Working together, a WLR test system was designed and developed to meet the unique requirements of Wafer-Level-Reliability testing. These systems are capable of testing to the voltage, current, and temperature extremes required for inducing the desired failure mechanisms in a short period of time. Some examples of the reliability failure mechanisms that are monitored using WLR techniques include:

## Wafer Level Reliability (WLR) (Continued)

### Interlayer Dielectric Integrity

Unique high voltage testing (to 1500V) is used to test for dielectric particles, metal hillocks or contamination, and poor dielectric stop coverage. Designed experiments have been successful in correlating the high voltage WLR test results to fab process monitors (such as deposition temperature and etch selectivity), and to accelerated life test results (Op-life, Temp Cycle, and Thermal Shock).

### Metal Step Coverage

High current testing of large area metal serpentine structures is performed to detect restrictions in the conducting stripe. Designed experiments have been successful in correlating the high current WLR test results to fab process monitors such as metal thickness, critical dimensions, and via size.

### Mobile Ions

A 200°C hot chuck is used with custom-built high temperature probe cards to accurately measure transistor threshold voltage shifts for a variety of oxide layers. Other methods for detecting mobile ion contamination include the use of self-heated polysilicon gate test structures and Triangular Voltage Sweep (TVS) test techniques.

### Metal Stress Voids

High current resistance measurements are taken before and after wafers are processed through a series of heating and cooling cycles. This heat treatment is designed to mimic the high temperature processing incurred during device assembly (such as a seal-dip furnace), and it has been shown to accelerate metal void formation when the stress of the overlying film is high enough. Significant increases in the final resistance indicate the formation of metal stress voids.

### Gate Oxide Integrity:

JEDEC J<sub>RAMP</sub>, V<sub>RAMP</sub> and Q<sub>BD</sub> test techniques are used to monitor gate oxide quality. The WLR tester is also used to perform very sensitive leakage current measurements, using a specially designed picoammeter module, which allows us to detect subtle differences in gate oxide quality.

### Passivation Integrity

A novel wafer-level-autoclave test technique has been developed which allows us to quantify the level of protection the passivation film provides when the wafer is subjected to a high temperature, high humidity environment.

### Hot Electron Degradation

Two wafer level tests are performed to indicate device susceptibility to hot electron damage. First, the maximum substrate current is measured to indicate the level of impact ionization occurring at the drain edge. Second, gate current measurements are taken to gauge the magnitude of electron injection during device operation. Long-term DC stressing of transistors at peak substrate current conditions is also monitored.

### Electromigration

A Standard Wafer Electromigration Accelerated Test (SWEAT) technique is used to measure the sensitivity of a metal line to electromigration failures. SWEAT is used as a relative test of the reliability of a line.

### Contact Electromigration

Risk of failures due to contact spiking and solid phase epitaxial growth (SPEG) are monitored by forcing current through specially designed test structures, and monitoring increases in resistance and substrate leakage.

## Electrostatic Discharge Sensitivity (ESD)

Low Voltage logic products are manufactured using either submicron CMOS or BiCMOS technology. To protect these circuits from the harmful effects of Human Body Model (HBM) ESD events, proprietary protection circuitry along with traditional ESD diodes are used.

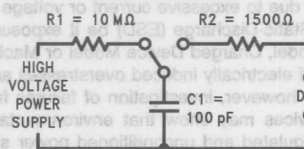
By design, this circuitry improves immunity to both HBM and Electrical Overstress (EOS). Protection from pin-to-ground (GND), pin-to-V<sub>CC</sub> is achieved through traditional diodes. Additional protection is provided via proprietary solutions that provide a low resistance path between V<sub>CC</sub> and GND during various ESD zap combinations.

The device design and layout ensures dependable turn-on characteristics as well as robustness.

ESD protection was achieved with no appreciable effect on speed or increase in capacitance.

Low voltage logic ESD sensitivity is guaranteed greater than 2000V, using the MIL-STD-883C, test method 3015 for Human Body Model (HBM) ESD.

HBM Test Circuit



TL/F/11564-2

Normal handling precautions should be observed as in the case of any semiconductor.

## Repeatability of HBM ESD Results

Research has shown that stray capacitance in the ESD testers can cause device degradation or early ESD failure. For this discussion, stray capacitance is defined as capacitance that is distributed from the device socket through the board connections and lines to the HBM R-C network: 1500Ω ± 1%, and charging capacitor: 100 pF ± 10%. This degradation is seen mainly in N-channel protection and is caused by the charge delivered by the stray capacitance, charge that is not accounted for in MIL STD-883C/3015.7.

Lowering stray capacitance in the tester is advocated by the EOS/ESD Association under their EOS/ESD-S5.1-1991 spec. This specification helps to improve tester-to-tester repeatability independent of part type, by designating ESD zap waveform guidelines, similar in fashion to those of MIL STD-883C/3015.7. The waveform guidelines ensure that zap capacitance of the tester will be limited to 30 pF or less.

The EOS/ESD Association has recommended EOS/ESD-S5.1-1991 be used in conjunction with MIL STD-883C/3015.7 to provide a better testing environment as well as the most representative HBM ESD zap waveform. Using this methodology will provide greater repeatability without compromising the intent of HBM ESD testing.

## Repeatability of HBM ESD Results

(Continued)

More information on stray capacitance and the EOS/ESD S5.1-1991 can be found in the 1993 EOS/ESD Symposium Proceedings' article "Analysis of HBM ESD testers and specifications using a 4th order lumped element model", pp. 129-137.

## Power Sensitivities for Minimum Geometry Products

The demand for high performance process technology capable of faster speeds, minimal noise and lower operating voltages drives the microelectronics industry towards decreasing layout geometries. Advanced process technology minimizes gate widths, gate oxide thickness and junction depths to improve gate switching speeds. In contrast, the decreased geometries reduce the ability of the devices built on advanced processes to resist electrical overstresses. As geometries decrease, emphasis shifts towards the reduction of environmentally induced electrical overstresses to ensure system and component reliability.

Market trends continue to drive the need for smaller geometries with reduced power supply voltages. Current 5.0V technologies are migrating towards 3.0V technologies while 3.0V technologies have shown a greater sensitivity to electrical overstresses. Sensitivities to electrical overstresses have been observed in as large as 1.0  $\mu\text{m}$  geometries.

Device damage from electrical overstresses vary and the categories include, but are not limited to: Electrical-Over-Stress (EOS) due to excessive current or voltage exposure and Electro-Static-Discharge (ESD) be it exposure by Human Body Model, Charged Device Model or Machine Model. Sources of electrically induced overstresses are difficult to determine; however, investigation of failures from small geometry devices may show that environmental hazards such as unregulated and unconditioned power supplies in the field exceed "Absolute Maximum Ratings" causing unrecoverable device damage.

In an effort to resolve device sensitivities to electrical overstresses, designers and engineers can reference device databooks. Databook specifications include "Absolute Maximum Ratings" and adherence to this specification is essential in ensuring component and system level reliability.

1. A. Amerasekera, A. Chatterjee, "An Investigation of BiCMOS ESD Protection Circuit Elements and Applications in Submicron Technologies", EOS/ESD Symposium, p58.6.1.

## Latchup Testing

Latchup in CMOS and BiCMOS circuits can vary in severity from being a temporary condition of excessive  $I_{CC}$  current and functional failure, to total destruction requiring a new unit. The latchup condition is usually caused by applying a stimulus that is able to cause a regenerative condition in a PNP-NPN structure. For a more detailed description of definitions and causes of latchup, see National Semiconductor Application Note 600 (located in the "FACT Advanced CMOS Logic Data book" Lit. # 40019).

National has characterized its Low Voltage logic for robustness using an IMCS 4600 Automated Latchup Test System, complying to the JEDEC Standard No. 17. The automated test equipment approach to latchup provides a repeatable test setup and application of test conditions, reduces the amount of time for evaluation, and provides a more comprehensive set of vectors and stimuli over a shorter period of time.

The JEDEC Standard No. 17 is a standard measurement procedure for the characterization of CMOS integrated circuit latchup susceptibility/immunity, measured under static conditions. The method allows for overcurrent/overvoltage stressing of inputs and outputs to detect latchup.

In short, the JEDEC Standard No. 17 follows a sequence of:

1. Apply power
2. Setup I/O conditions to place device in desired state
3. Apply trigger source for desired duration
4. Measure supply current
5. Remove power supply if  $I_{CC} \geq$  test limit
6. Inspect for electrical damage

For Low Voltage logic products, all logic states are checked for a susceptibility to latchup with all outputs high, all outputs low, and all outputs in TRI-STATE®. If the device is a bi-directional device, then the logic states are tested in each direction. All inputs and outputs are tested for each logic state and direction.

For products with clamp diodes at inputs and outputs, a Positive and a Negative Current Trigger are required as stimuli for latchup. National characterizes latchup testing on all low voltage logic products at 125°C and at maximum supply voltage.

Due to the high trigger stresses, devices used for latchup testing should be discarded and not used for design, production, or other tests. Latchup testing is potentially destructive and may limit the life of a device.



## Section 4 Contents

4-3	Low Voltage Logic Applications and Design Considerations .....
4-3	Interfacing 3V/5V Logic .....
4-3	Introduction .....
4-3	Interfacing Dual Voltage Systems .....
4-4	Guidelines for Using Logic in Dual Supply (3V/5V) Systems .....
4-5	Interfacing to Pure 3V LVC Logic .....
4-6	Interfacing to 5V Tolerant LVT and LVC Logic .....
4-7	Using LVX383 and LVX384 "Zero Delay" 10-Bit CMOS Bus Switches for 5V to 3V Signal Conversion .....
4-8	Using LVT Dual Supply Translating Logic .....
4-8	Summary .....
4-9	Line Driving and Termination .....
4-11	CMOS Noise Effects .....
4-12	Crosstalk .....
4-12	Decoupling Requirements .....
4-16	Capacitor Types .....
4-17	

## Section 4 Application and Design Considerations



## Section 4 Contents

Low Voltage Logic Applications and Design Considerations .....	4-3
Interfacing 3V/5V Logic .....	4-3
Introduction .....	4-3
Interfacing Dual Voltage Systems .....	4-3
Guidelines for Using Logic in Dual Supply (3V/5V) Systems .....	4-4
Interfacing to Pure 3V LVQ Logic .....	4-5
Interfacing to 5V Tolerant LVX and LCX Logic .....	4-6
Using LVX3L383 and LVX3L384 "Zero Delay" 10-Bit CMOS Bus Switches for 5V to 3V	
Signal Conversion .....	4-7
Using LVX Dual Supply Translating Logic .....	4-8
Summary .....	4-9
Line Driving and Termination .....	4-9
CMOS Bus Loading .....	4-11
Noise Effects .....	4-12
Crosstalk .....	4-12
Decoupling Requirements .....	4-16
Capacitor Types .....	4-17



# Low Voltage Logic Applications and Design Considerations

## Interfacing 3V/5V Logic

### Introduction

Today's portable and battery-operated system designer is faced with the problem of keeping ahead when addressing system performance, long battery life and reliability. National Semiconductor's advanced CMOS Logic helps designers achieve these goals. Low Voltage CMOS Logic, like LVQ, LVX and LCX, are designed to alleviate many of the drawbacks that are common on present technology logic circuits. LV logic combines the low static power consumption and the high noise margins of CMOS with a high fan-out, low input loading and at least 75Ω transmission line drive capability. Performance features such as advanced Schottky speeds at CMOS power levels, excellent noise suppression, ESD protection, and latch-up immunity are characteristics that designers of state-of-the-art systems require.

To fully utilize the advantages provided by LV logic, the system designer should have an understanding of the flexibility as well as the trade-offs of CMOS design. The following section discusses common interfacing concerns relative to the performance and requirements of LV logic.

### Table of Contents

#### 1.0 INTERFACING DUAL VOLTAGE SYSTEMS

#### 2.0 INTERFACING TO PURE 3V LVQ LOGIC

#### 3.0 INTERFACING TO 5V TOLERANT LVX AND LCX LOGIC

#### 4.0 USING LVX3L383 AND LVX3L384 "ZERO DELAY" 10-BIT CMOS BUS SWITCHES FOR 5V TO 3V SIGNAL CONVERSION

#### 5.0 USING LVX DUAL SUPPLY TRANSLATING LOGIC

#### 6.0 SUMMARY

### 1.0 Interfacing Dual Voltage Systems

In order to reliably interface one integrated circuit to another, recommended input and output specifications for voltage and current must be satisfied. Output specifications of the driving IC must meet the input requirements ( $V_{IL}$  and  $V_{IH}$ ) of the receiver IC in order for the circuit design to function properly. This "noise margin" protects the design against malfunction during system and environmentally generated noise.

For better than two decades, almost all digital signal processing has been designed around a 5V standard power supply. During this period of time countless IC vendors have introduced new product families with higher drive, faster speeds, and lower power. As a result several Input/Output standards exist in the 5V world and interfacing between them can get confusing. Because of the inherent restrictions, pure-TTL technologies cannot operate with a 3.3V power supply. Therefore, the core technology for all 3V ICs will be MOS. In a straight 3V MOS system, all connections can be done directly, both on the outputs and on the inputs.

However, it will be quite some time before ALL components in a portable/desktop PC can operate at 3.3V. This is especially true for peripheral devices such as displays, printers, and faxes. Therefore, at some point in the system, 3V ICs must interface with 5V ICs. If mishandled, this interface will waste power and compromise reliability. On the following pages, solutions to possible dual voltage interfaces are outlined.

**TABLE I: Interfacing Guidelines for Using Logic in Dual Supply (3V/5V) Systems.**

See example for an explanation of how to use this table.

		5V			3V			
		TTL 74F245	CMOS 74AC245	3V/5V Translator 74LVX4245	Pure 3V 74LVQ245	5V Tolerant 74LVX245	5V Tolerant 74LCX245	3V/5V Translator 74LVX3245
		V <sub>IH</sub> = 2 V <sub>IL</sub> = 0.8	V <sub>IH</sub> = 3.85 V <sub>IL</sub> = 1.35	V <sub>IH</sub> = 2 V <sub>IL</sub> = 0.8	V <sub>IH</sub> = 2.4 V <sub>IL</sub> = 0.8	V <sub>IH</sub> = 2 V <sub>IL</sub> = 0.8	V <sub>IH</sub> = 2 V <sub>IL</sub> = 0.8	V <sub>IH</sub> = 2 V <sub>IL</sub> = 0.8
5V	TTL 74F245	Yes Direct 0.7 0.25	No None -1.15 0.8	Yes Direct 0.7 0.25	OK (Note 2) 0.3 0.25	OK (Note 2) 0.7 0.25	Yes Direct 0.7 0.25	Yes Direct 0.7 0.25
	CMOS 74AC245	Yes Direct 2.3 0.7	Yes Direct 0.45 1.25	Yes Direct 2.3 0.7	No None 1.9 0.7	Yes Direct 2.3 0.7	Yes Direct 2.3 0.7	Yes Direct 2.3 0.7
	3V/5V Translator 74LVX4245	Yes Direct 0.9 0.7	No None -0.95 1.25	Yes Direct 0.9 0.7	Yes Direct 0.5 0.7	Yes Direct 0.9 0.7	Yes Direct 0.9 0.7	Yes Direct 0.9 0.7
3V	Pure 3V 74LVQ245	OK Pull-Down 0.8 0.7	No None -1.05 1.25	Yes Direct 0.8 0.7	Yes Direct 0.4 0.7	Yes Direct 0.8 0.7	Yes Direct 0.8 0.7	Yes Direct 0.8 0.7
	5V Tolerant 74LVX245	OK TRI-STATE Outputs 0.8 0.7	No None -1.05 1.25	Yes Direct 0.8 0.7	Yes Direct 0.4 0.7	Yes Direct 0.8 0.7	Yes Direct 0.8 0.7	Yes Direct 0.8 0.7
	5V Tolerant 74LCX245	OK TRI-STATE Outputs 0.8 0.7	No None -1.05 1.25	Yes Direct 0.8 0.7	Yes Direct 0.4 0.7	Yes Direct 0.8 0.7	Yes Direct 0.8 0.7	Yes Direct 0.8 0.7
	3V/5V Translator 74LVX3245	Yes Direct 2.4 0.7	Yes Direct 0.55 1.25	Yes Direct 2.4 0.7	Yes Direct 0.7 0.7	Yes Direct 2.4 0.7	Yes Direct 2.4 0.7	Yes Direct 2.4 0.7

**Note 1:** Refer to individual device datasheets for  $V_{OH}$  and  $V_{OL}$  levels.  $V_{OH}$  and  $V_{OL}$  are dependant on  $I_{OH}$  and  $I_{OL}$  values.

Typical values of  $V_{OH}/V_{OL}$  used to calculate noise margins.

**Note 2:** Regulate both 3V and 5V power supplies together to maintain a safe 5V  $V_{OH}$  to 3V  $V_{CC}$  delta.

**Example:** Suppose a 5V CMOS (i.e. 74AC245) input is driven by a 3V/5V Translator (i.e. 74LVX3245) 3V outputs.

		Receiver (Input)	
		5V	3V
5V	Driver (Output)	CMOS 74AC245	According to Table I a 5V CMOS device, like the 74AC245, <b>can be interfaced</b> with a 3V/5V Translator, like the 74LVX4245, by <b>directly connecting</b> the input and output. This works because the <b><math>V_{OH}</math> of the 74LVX4245 is greater than the <math>V_{IH}</math> specification</b> of the 74AC245 input and the <b><math>V_{OL}</math> of the 74LVX4245 is less than the <math>V_{IL}</math> specification</b> of the 74AC245 input. Therefore a low or a high which ever is the case is maintained between the output to the input.
		$V_{IL} = 1.35$ $V_{IH} = 3.85$	
3V	3V/5V Translator 74LVX3245	Yes Direct 0.55 1.25	OK to interface? Recommended method Noise Margin Low (V) = $V_{IL} - V_{OL}$ Noise Margin High (V) = $V_{OH} - V_{IH}$

## 2.0 Interfacing to Pure 3V LVQ Logic

### 2.1 INTERFACING 5.0V TTL OR "REDUCED SWING" CMOS TO PURE 3V LVQ LOGIC

Bipolar TTL ICs or the newly introduced "reduced swing" (NMOS pull-up) CMOS ICs are the easiest of the 5V technologies to interface with because of their 3V output signal. 3V ICs such as LVQ have input specifications similar to the 5V TTL or TTL-compatible CMOS ICs. In this case, interfacing at this point may be direct. To safeguard this configuration against voltage and temperature fluctuations the designer should regulate BOTH the 3.3V and 5V power supplies together. Another option is to purposely run the 5V power supply on the low side to decrease the 5V-3V  $V_{OH}$ -to- $V_{CC}$  delta. This optimum configuration reduces any DC power loss from termination at the interface to zero. However, if the same system is allowed to operate with power supply tolerances that could vary  $\pm 10\%$  independently (examples: 5.0V  $\pm 10\%$  and 3.3V  $\pm 10\%$ ), then the input specifications for LVQ products would be violated. In order to remain within the absolute maximum specifications for LVQ products, the  $V_{OH}$  of the TTL I/O must be held to within 0.5V of the LVQ  $V_{CC}$ . The best way to reduce  $V_{OH}$  while retaining signal fidelity and specified propagation delays is to add a parallel resistor termination (to GND) to every signal line at the dual voltage interface.

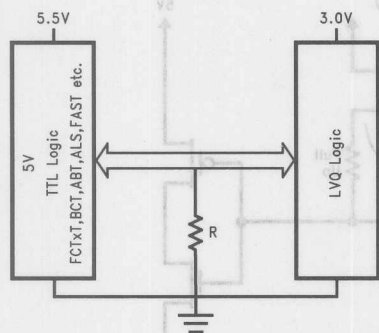


FIGURE 1a. Dual Voltage with Parallel Resistor Termination

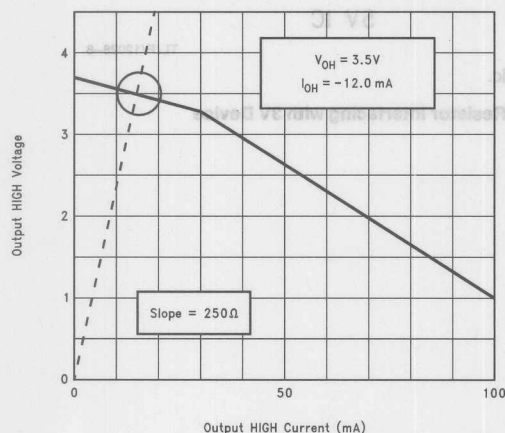


FIGURE 1b. 74F244 Output Drive

The "R" value in Figure 1a, Figure 1b is derived using manufacturer supplied  $I_{OH}/V_{OH}$  curves in conjunction with the formula:  $R = 3.5V/I_{OH} @ V_{OH} = 3.5V$ . In this example, the bipolar  $I_{OH}/V_{OH}$  curve is from the FAST Applications Handbook. Although only the 74F244 case is shown, the method also applies to a "reduced swing" CMOS, BiCMOS, and other bipolar devices.

### 2.2 INTERFACING 5.0V CMOS TO PURE 3V LVQ LOGIC

When ordinary LVQ inputs are driven beyond  $V_{CC}$ , large currents will flow into the silicon substrate raising the internal  $V_{CC}$  of the device to 4.0V or above. Therefore, it is generally not recommended to interface CMOS at 5.0V to these devices at 3.3V. However, such a configuration may become unavoidable in some mixed/dual voltage designs. In order to reduce the  $V_{OH}$  level of a CMOS device, a voltage divider must be set up on the output to provide the correct  $V_{OH}$  level to the device. One possible configuration is shown in the Figure 2.

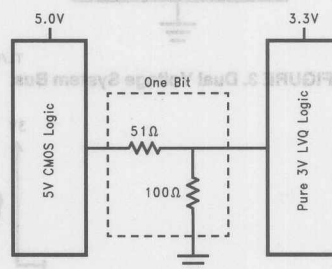


FIGURE 2. Dual Voltage with Resistor Divider Network

Although DC power is consumed by the voltage divider, using higher values of resistance for the voltage divider will create an additional propagation delay across the interface. This is due to the RC time constant setup by device inputs and the Thevenin equivalent resistance of the voltage divider. The resistance values shown exhibit a good compromise between DC power loss and signal fidelity.

### 2.3 INTERFACING PURE 3V LVQ LOGIC TO 5.0V INPUTS

Interfacing a 3V LVQ IC's output to a 5V TTL-compatible input can be done directly. LVQ 3V output specifications and 5V TTL-compatible specifications are compatible. Interfacing a 3V LVQ output to a 5V CMOS ( $V_{IH} = 3.15V @ V_{CC} = 5.0V$ ) input should NEVER be done, because the 5V CMOS part will require a low impedance pull-up to  $V_{CC}$  to satisfy its input requirements. Whenever a Pure 3V LVQ output is pulled up beyond its  $V_{CC}$ , an intrinsic diode in the output structure will begin to forward bias causing excessive currents to flow from the interface through the 3V output and into the 3.3V power supply. This could raise the output level of the 3.3V supply to a level exceeding the maximum rated voltages for some low voltage devices.

Many types of 5V Bipolar inputs can present a similar problem at the dual voltage interface. It is common for a Bipolar device to have 10 kΩ-20 kΩ internal pull-up resistors on every input pin connected directly to the 5V  $V_{CC}$  plane. In this case, external pull-down resistors are recommended to create a voltage divider network that would set the logic HIGH voltage to a safe level for the 3V output as described earlier. Figure 3 illustrates such an interface. This type of

## 2.0 Interfacing to Pure 3V LVQ

### Logic (Continued)

pull-down is also ideal for any bus with Bipolar or "Reduced Swing" I/O that can be TRI-STATE with high-impedance driver outputs. In the past, busses of this type were pulled up to  $V_{CC}$  with  $4\text{ k}\Omega$  resistors. The same results, pulling the bus away from threshold sensitive areas, are achieved with the pull-down resistor recommended. The value of this resistor is chosen based on the desired voltage divider network.

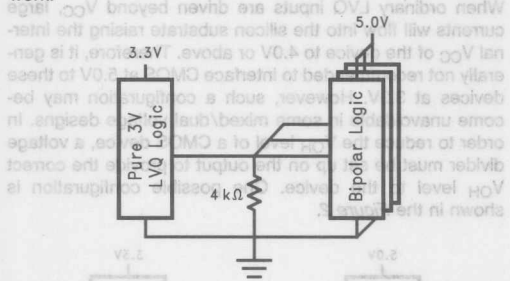
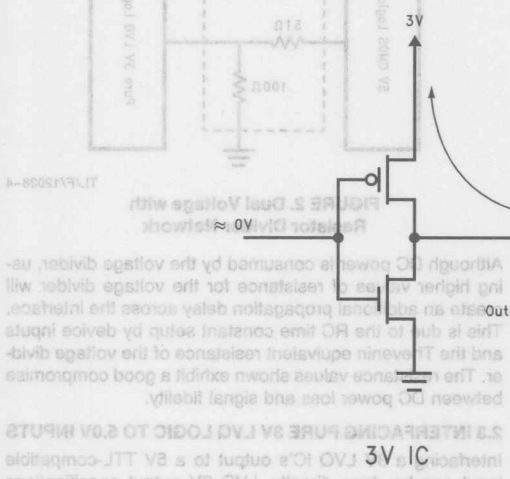


FIGURE 3. Dual Voltage System Bus



**Caution:** Avoid driving 5V IC's that have input pull-ups with 3V logic.

FIGURE 4. 5V IC with Internal Input Pullup Resistor Interfacing with 3V Device

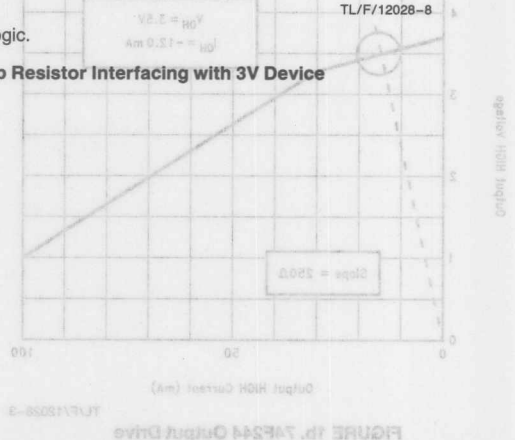
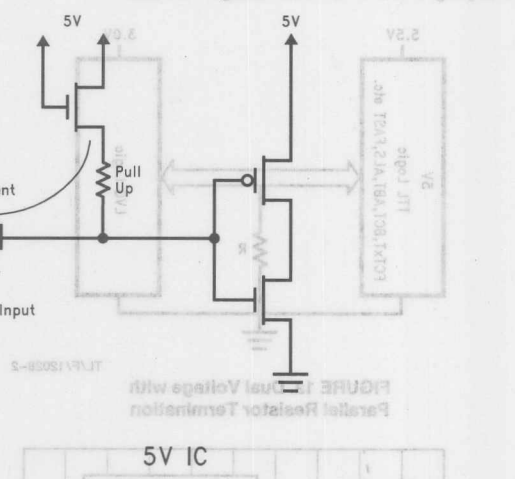
Many types of 5V Bipolar inputs can present a similar problem at the dual voltage interface. It is common for a Bipolar device to have  $10\text{ k}\Omega$ – $20\text{ k}\Omega$  internal pull-up resistors on every input pin connected directly to the  $5\text{ V}_{CC}$  plane. In this case, external pull-down resistors are recommended to create a voltage divider network that would set the logic HIGH voltage to a safe level for the 3V output as described earlier. Figure 3 illustrates such an interface. This type of

## 3.0 Interfacing to 5V Tolerant LVX and LCX Logic

### 3.1 INTERFACING 5V TOLERANT OUTPUTS TO 5V BUSES AND 5V DEVICES WITH INPUT PULL-UPS

5V tolerant inputs may safely be connected to 5V busses, however, care must be taken when interfacing 5V tolerant outputs to 5V busses to make certain these outputs are always in TRI-STATE when a 5V signal exists on the bus. It is important to note that this 5V signal may not only arise from bus contention, but also a bus which is pulled up to  $V_{CC} = 5\text{ V}$  by a pull-up resistor. A similar but less obvious situation which should be avoided occurs when these outputs are connected to 5V devices with input pull-up resistors. Devices, such as certain PLD's and chipsets which have internal input pullups will cause leakage currents to flow through the pull-up and into the substrate of the 3V device. Close attention should be paid to 5V device data-sheets and 5V bus architectures to be sure no pull-ups exist.

LVO products, the V<sub>OH</sub> of the TTL NO must be held to within 0.5V of the LVO V<sub>CC</sub>. The best way to reduce V<sub>OH</sub> while retaining signal fidelity and speed of propagation delay is to add a parallel resistor termination (to GND) to every signal line at the dual voltage interface.



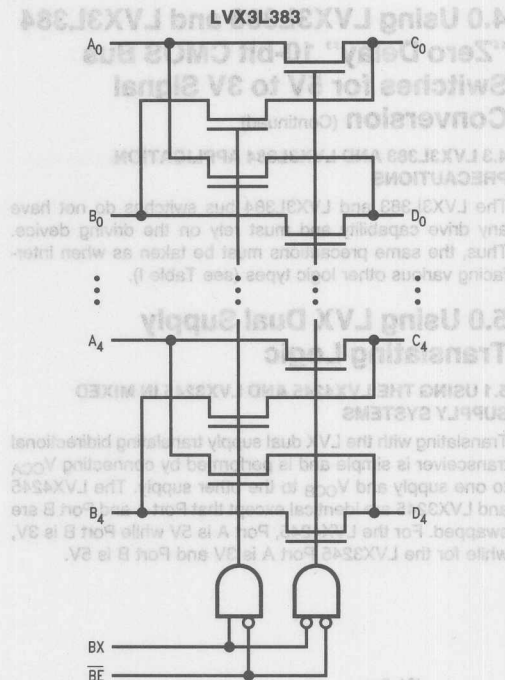
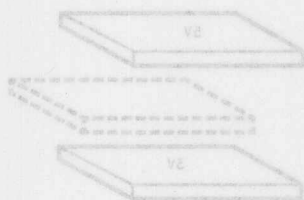
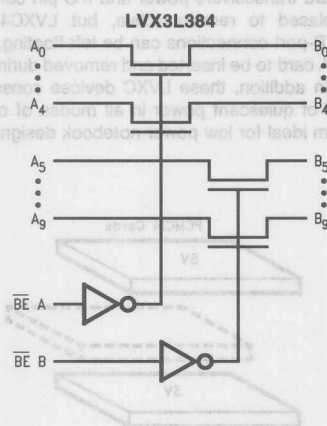
## 3.0 Interfacing to 5V Tolerant LVX and LCX Logic (Continued)

### 3.2 INTERFACING 5V TOLERANT LOGIC TO 5V CMOS INPUTS

Never interface a 3V "TTL compatible" output directly to a 5V CMOS ( $V_{IH} = 3.15V @ V_{CC} = 5.0V$ ) input. The 3V IC cannot satisfy the  $V_{IH}$  requirement of the 5V CMOS input. If the 3V device is able to switch the 5V CMOS device, it will do so unreliably. A 5V translator with a higher  $V_{OH}$  such as the 74LVX3245 ( $V_{OH} = 4.4V @ I_{OUT} = -100 \mu A$ ) should be used instead.

## 4.0 Using LVX3L383 and LVX3L384 "Zero Delay" 10-bit CMOS Bus Switches for 5V to 3V Signal Conversion

### 4.1 10-BIT BUS BLOCK DIAGRAMS



The 10-bit CMOS bus switches consist of NMOS pass transistors which act as a  $5\Omega$  switch between the two ports. Input signals are conveyed from one port to the other relatively unchanged except that they are clipped to a maximum voltage of about  $V_{OUT MAX} = V_{CC} - 1V$  since the transistor begins to turn off as its source/drain nears its gate voltage. By adding a diode between the  $V_{CC}$  pin and a 5V supply,  $V_{OUT MAX}$  is approximately  $V_{CC} - 1.7V = 3.3V$ . Thus, when 5V signals are applied to either port, they are clipped to about 3.3V. Substrate leakage issues are not a problem as they are with some 5V tolerant logic because the pass transistors are NMOS, not PMOS, devices. Thus, the source/drain to substrate intrinsic diode is reverse biased, not forward biased.

### 4.2 ADDITIONAL BENEFITS OF USING LVX3L383 AND LVX3L384 5V TO 3V TRANSLATORS

The LVX3L383 and LVX3L384 provide 5V-3V translation while consuming almost no current ( $0.3 \mu A$ ) and having virtually no propagation delay ( $\leq 250$  ps). In addition, the bus enable signals (which are tied to the transistors' gates) can be used to turn off the translation function to reduce switching power when in power conservation mode. The bus enable signals can also be used to increase the speed of some busses by disconnecting devices when they are not required to talk to the bus. This reduces the loading on the bus which can increase bus speeds.

## 4.0 Using LVX3L383 and LVX3L384 "Zero Delay" 10-bit CMOS Bus Switches for 5V to 3V Signal Conversion (Continued)

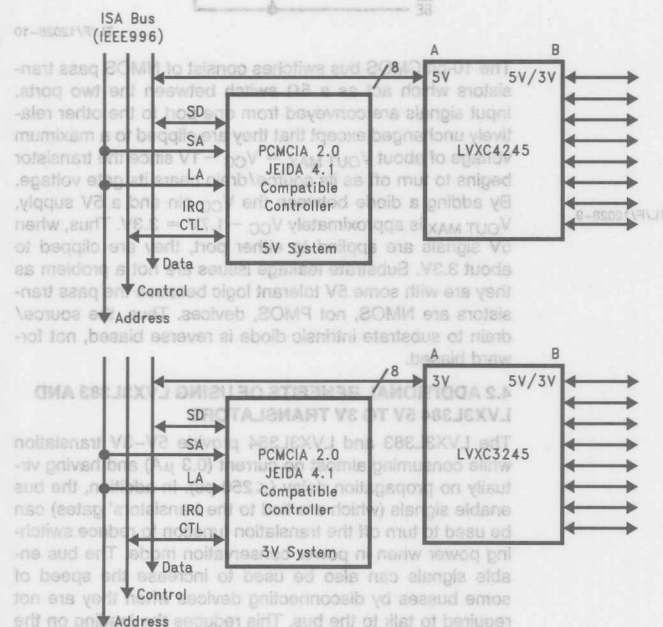
### 4.3 LVX3L383 AND LVX3L384 APPLICATION PRECAUTIONS

The LVX3L383 and LVX3L384 bus switches do not have any drive capability and must rely on the driving device. Thus, the same precautions must be taken as when interfacing various other logic types (see Table I).

## 5.0 Using LVX Dual Supply Translating Logic

### 5.1 USING THE LVX4245 AND LVX3245 IN MIXED SUPPLY SYSTEMS

Translating with the LVX dual supply translating bidirectional transceiver is simple and is performed by connecting  $V_{CCA}$  to one supply and  $V_{CCB}$  to the other supply. The LVX4245 and LVX3245 are identical except that Port A and Port B are swapped. For the LVX4245, Port A is 5V while Port B is 3V, while for the LVX3245 Port A is 3V and Port B is 5V.

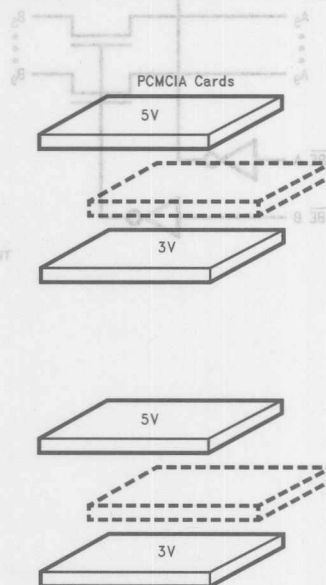


### 5.2 USING THE LVXC4245 AND LVXC3245 FOR PCMCIA CARD INTERFACE

The flexible PCMCIA 2.0 standard allows for both 3V and 5V PCMCIA cards as well as for supply voltage to be reduced from 5V to 3V for power conservation. Such requirements necessitate a configurable port-to-card interface design. National Semiconductor's LVXC4245 and LVXC3245 provide on demand B-port supply voltage configuration for PCMCIA card and other real time configurable I/O applications.

The A Port supply voltages for the LVXC4245 and LVXC3245 are 5V and 3V, respectively. The devices' B-ports are configurable by changing the supply voltage on the B-port  $V_{CC}$  pin. Changing the supply voltage on the B-port  $V_{CC}$  pin between 3V and 5V will configure the B-port I/O to either 3V or 5V I/O levels. Thus, for PCMCIA applications, 3V and 5V cards are accommodated by tying the B-port  $V_{CC}$  to the card voltage supply.

There are other PCMCIA port-to-card interface considerations. For instance, the B-port supply and I/O pins will float coincidentally when the PCMCIA card is removed from the slot. Standard transceivers power and I/O pin connections must be biased to remain active, but LVXC4245 and LVXC3245 B-port connections can be left floating, allowing the PCMCIA card to be inserted and removed during normal operation. In addition, these LVXC devices consume less than 1 mW of quiescent power in all modes of operation, making them ideal for low power notebook designs.



TL/F/12028-12

## 6.0 Summary

There are a variety of low voltage logic choices available to system designers. They can be classified into their level of 5V tolerance; pure 3V, 5V input-only tolerant, 5V input and output tolerant, bus switches, and dual supply 3V/5V translator logic devices. At first the choices and their interface requirements may seem confusing, but each has its own benefits:

### Benefits of National Semiconductor's Low Voltage Logic

<b>LVQ</b>
<b>Octals, Gates, MSI</b>
3V Inputs and Outputs
Low Cost
Low Power
Reduced Noise
Low EMI
<b>LVX</b>
<b>Octals, Gates, MSI</b>
5V Tolerant Inputs
Low Cost
Low Power
Broad Family
<b>LVX3L383/4 Bus Switch Family</b>
5V-3V Translation
"Zero Delay" (250 ps) 5V-3V Transition
Ultra Low Power Consumption
<b>LVX Translator Family</b>
5V-3V and 3V-5V Translation
Efficient Translation
Configurable B-Port (LVXC)
Low Power
<b>LCX</b>
<b>Octals, 16-bit</b>
5V Tolerant Inputs and Outputs
High Speed
Low Power
±24 mA Drive
Powerdown High Impedance
<b>LVT</b>
<b>Octals, 16-bit</b>
5V Tolerant Inputs and Outputs
Higher Speed
Higher Drive (±64/-32 mA)
Bushold
Power up/down High Impedance

Factors such as speed, power, cost, quantity and location of 3V logic on the board, and noise should be considered when choosing the appropriate logic family. National offers multiple alternate sourced low voltage logic families to choose from in order to provide cost effective, efficient, and reliable solutions in a variety of applications.

### Line Driving and Termination (Continued)

In mostly 3V systems, National's LVQ logic provides the most cost effective solution. The LVQ family offers a wide range of logic functions from transceivers to MSI devices. LVQ devices also feature very low power consumption and patented Quiet Series EMI reduction circuitry.

LVX and LCX are recommended for interfacing between 3V and 5V signals. Both are based on a CMOS process. Because it is CMOS based, both consume very little power which make them ideal for battery powered applications. Both have guaranteed simultaneous switching noise level and dynamic threshold performance. This is where the similarity ends.

LVX is recommended for slower and more cost sensitive mixed supply systems. It has very low noise due to its lower drive capability. LVX can provide the majority of logic functions because it offers the broadest family line. It can tolerate 5V signals on its inputs which makes it ideal for interfacing 5V or 3V signals.

LCX is recommended for high speed applications. This is National's flagship CMOS line. It is built on our state-of-the-art CMOS process. With a higher drive capability than LVX and National Semiconductor's patented Quiet Series EMI reduction circuitry a designer can now have the best of both worlds; low noise and high drive. It can not only tolerate 5V on its inputs and also on its outputs (or I/Os) when in TRI-STATE.

The LVX3L384 and LVX3L383 provide very fast, ultra low power translation from 5V to 3V signal levels. They can also be used to isolate signals in order to reduce switching power and bus loading.

In situations where there is a need for 3V/5V translation only, the LVX translator family provide the most reliable and efficient interface. Use the 74LVX4245 or 74LVX3245 where the supply voltages are fixed and use the LVXC4245 or LVXC3245 when it is necessary to select the B-port supply voltage on-the-fly.

In a bus/backplane environment (i.e., in telecommunication, PBx etc.) where power up/down high impedance is necessary or a high performance system (i.e., Workstations, servers etc.) where high drive or speed is required; LVT can provide the solution.

## Line Driving and Termination

With the available high-speed logic families, designers can reach new heights in system performance. Yet, these faster devices require a closer look at transmission line effects.

Although all circuit conductors have transmission line properties, these characteristics become more significant when the edge rates of the drivers are equal to or less than three times the propagation delay of the line. Significant transmission line properties may be exhibited in an example where devices have edge rates of 3 ns and lines of 8 inches or greater, assuming propagation delays of 1.7 ns/ft for an unloaded printed circuit trace.

Of the many properties of transmission lines, two are of major interest to the system designer:  $Z_0$ , the effective equivalent impedance of the line, and  $t_{pde}$ , the effective propagation delay down the line. It should be noted that the

## Line Driving and Termination (Continued)

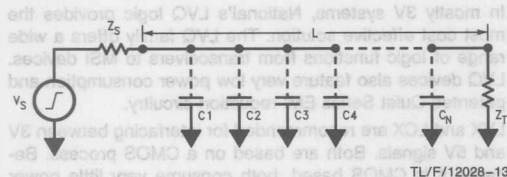


FIGURE 5a. Transmission Line with Distributed Loading

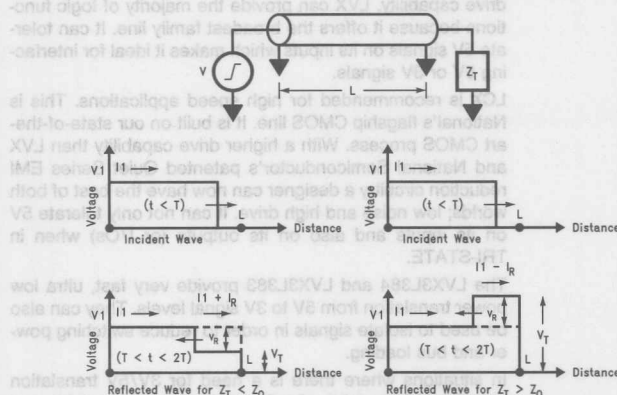


FIGURE 5b. Reflections Due to Impedance Mismatching

intrinsic values of line impedance and propagation delay,  $Z_0$  and  $t_{pd}$ , are geometry-dependent. Once the intrinsic values are known, the effects of gate loading can be calculated. The loaded values for  $Z'_0$  and  $t_{pde}$  can be calculated with:

$$Z'_0 = \frac{Z_0}{\sqrt{1 + C_D/C_L}}$$

$$t_{pde} = t_{pd} \sqrt{1 + C_D/C_L}$$

where  $C_L$  = intrinsic line capacitance and  $C_D$  = additional capacitance due to gate loading.

The formulas indicate that the loading of lines decreases the effective impedance of the line and increases the propagation delay. Lines that have a propagation delay greater than one third the rise time of the signal driver should be evaluated for transmission line effects. When performing transmission line analysis on a bus, only the longest, most heavily loaded and the shortest, least loaded lines need to be analyzed. All lines in a bus should be terminated equally; if one line requires termination, all lines in the bus should be terminated. This will ensure similar signals on all of the lines.

There are several termination schemes which may be used. Included are series, parallel, AC parallel, and Thevenin terminations. AC parallel and series terminations are the most useful for low power applications since they do not consume any DC power. Parallel and Thevenin terminations experience high DC power consumption.

Length of Transmission Line =  $L$

Distributed Load Capacitance per Unit Length =  $C_D = \sum_{n=1}^N C_L/L$

Characteristic Impedance

of a Transmission Line

Altered by Distributed Loading

$$= Z_0$$

$$= \sqrt{\frac{L_0}{C_0 + C_D}}$$

$$= \frac{Z_0}{\sqrt{1 + \frac{C_D}{C_0}}}$$

$$\text{Effective Reflection Coefficient at Termination} = \rho = \frac{Z_T - Z'_0}{Z_T + Z'_0}$$

- Length of Transmission Line =  $L$
- Delay of Transmission Line =  $T$
- Time of Sample =  $t$
- Incident Wave Current =  $I_i$
- Incident Wave Voltage =  $V_i$
- Reflected Wave Current =  $I_r$
- Reflected Wave Voltage =  $V_r$
- Characteristic Impedance of Line =  $Z_0$
- Termination Impedance =  $Z_T$
- Voltage at Termination =  $V_T$

TL/F/12028-14

## SERIES TERMINATIONS

Series terminations are most useful in high-speed applications where most of the loads are at the far end of the line or especially for single point loads. Loads that are between the driver and the end of the line will receive a two-step waveform. The first step will be the incident wave,  $V_i$ . The amplitude is dependent upon the output impedance of the driver, the value of the series resistor, and the impedance of the line according to the formula

$$V_i = V_{DD} \cdot Z'_0 / (Z'_0 + R_S + Z_S)$$

The amplitude will be one-half the voltage swing if  $R_S$  (the series resistor) plus the output impedance ( $Z_S$ ) of the driver is equal to the line impedance. The second step of the waveform is the reflection from the end of the line and will have an amplitude equal to that of the first step. All devices on the line will receive a valid level only after the wave has propagated down the line and returned to the driver. Therefore, all inputs will see the full voltage swing within two times the delay of the line.

## PARALLEL TERMINATION

Parallel terminations are not generally recommended for CMOS circuits due to their power consumption, which can exceed the power consumption of the logic itself. The power consumption of parallel terminations is a function of the resistor value and the duty cycle of the signal. In addition, parallel termination tends to bias the output levels of the driver towards either  $V_{CC}$  or ground. While this feature is not desirable for driving CMOS inputs, it can be useful for driving TTL inputs.

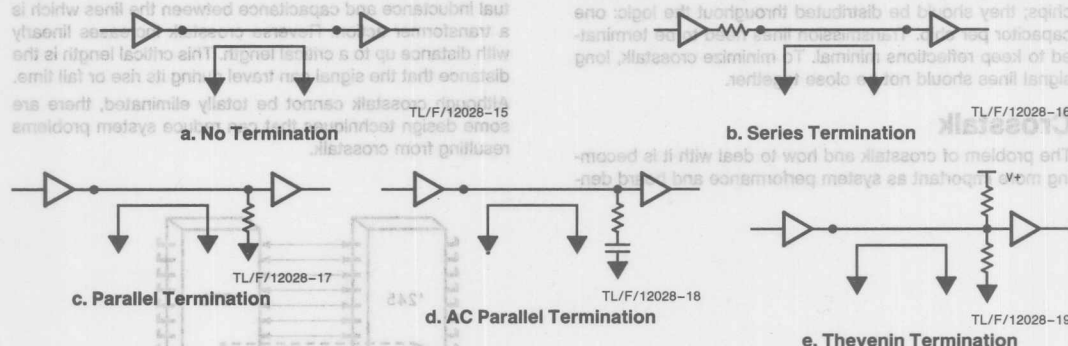
## Line Driving and Termination (Continued)

### AC PARALLEL TERMINATION

AC parallel terminations work well for applications where the delays caused by series terminations are unacceptable. The terminating effects of AC parallel terminations are similar to the effects of standard parallel terminations. The major difference is that the capacitor blocks any DC current path and helps to reduce power consumption.

### THEVENIN TERMINATION

Thevenin terminations are also not generally recommended due to their power consumption. Like parallel termination, a DC path to ground is created by the terminating resistors. The power consumption of a Thevenin termination, though, will generally not be a function of the signal duty cycle.

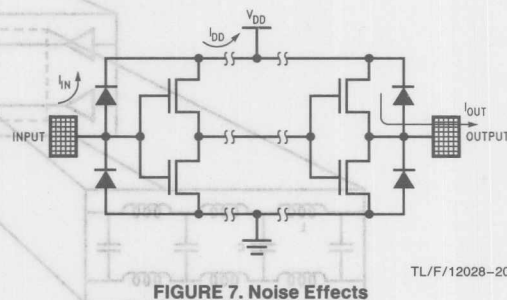


**FIGURE 6b. Termination Schemes**

## CMOS Bus Loading

CMOS logic devices have clamp diodes from all inputs and outputs to  $V_{CC}$  and ground. While these diodes increase system reliability by damping out undershoot and overshoot noise, they can cause problems if power is lost.

Figure 7 exemplifies the situation when power is removed. Any input driven above the  $V_{CC}$  pin will forward-bias the clamp diode. Current can then flow into the device, and out  $V_{CC}$  or any output that is HIGH. Depending upon the system, this current,  $I_{IN}$ , can be quite high, and may not allow the bus voltage to reach a valid HIGH state. One possible solution to eliminate this problem is to place a series resistor in the line. Another possible solution would be to ensure that the output enable input is inactive, preventing the outputs from turning on and loading down the bus. This may be accomplished by hardwiring a 4.7 k $\Omega$  pull-up resistor to the  $V_{CC}$  pin of the device.



## Noise Effects

Low Voltage Logic offers excellent noise immunity.

However, even the most advanced technology cannot alone eliminate noise problems. Good circuit board layout techniques are essential to take full advantage of the performance of Low Voltage Logic circuits.

Well-designed circuit boards also help eliminate manufacturing and testing problems.

Another recommended practice is to segment the board into a high-speed area, a medium-speed area and a low-speed area. The circuit areas with high current requirements (i.e., buffer circuits and high-speed logic) should be as close to the power supplies as possible; low-speed circuit areas can be furthest away.

Decoupling capacitors should be adjacent to all buffer chips; they should be distributed throughout the logic: one capacitor per chip. Transmission lines need to be terminated to keep reflections minimal. To minimize crosstalk, long signal lines should not be close together.

## Crosstalk

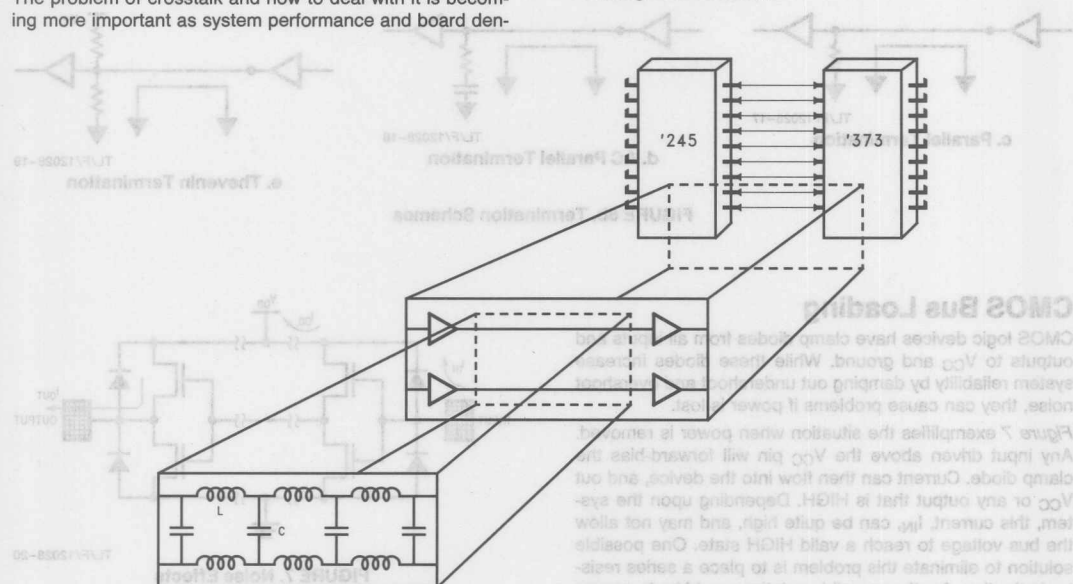
The problem of crosstalk and how to deal with it is becoming more important as system performance and board den-

sities increase. Crosstalk is the coupling of signals from one line to another. The amplitude of the noise generated on the inactive line is directly related to the edge rates of the signal on the active line, the proximity of the two lines and the distance that the two lines are adjacent. See Figure 8.

Crosstalk has two basic causes. Forward crosstalk, Figures 9 and 11, is caused by the wavefront propagating down the printed circuit trace at two different velocities. This difference in velocities is due to the difference in the dielectric constants of air ( $\epsilon_r = 1.0$ ) and epoxy glass ( $\epsilon_r = 4.7$ ). As the wave propagates down the trace, this difference in velocities will cause one edge to reach the end before the other. This delay is the cause of forward crosstalk; it increases with longer trace length, so consequently the magnitude of forward crosstalk will increase with distance.

Reverse crosstalk, Figures 10 and 12, is caused by the mutual inductance and capacitance between the lines which is a transformer action. Reverse crosstalk increases linearly with distance up to a critical length. This critical length is the distance that the signal can travel during its rise or fall time.

Although crosstalk cannot be totally eliminated, there are some design techniques that can reduce system problems resulting from crosstalk.



- Two parallel signal lines provide mutual inductance and shunt capacitance.

FIGURE 8. Where Does Crosstalk Take Place?

# Crosstalk (Continued)

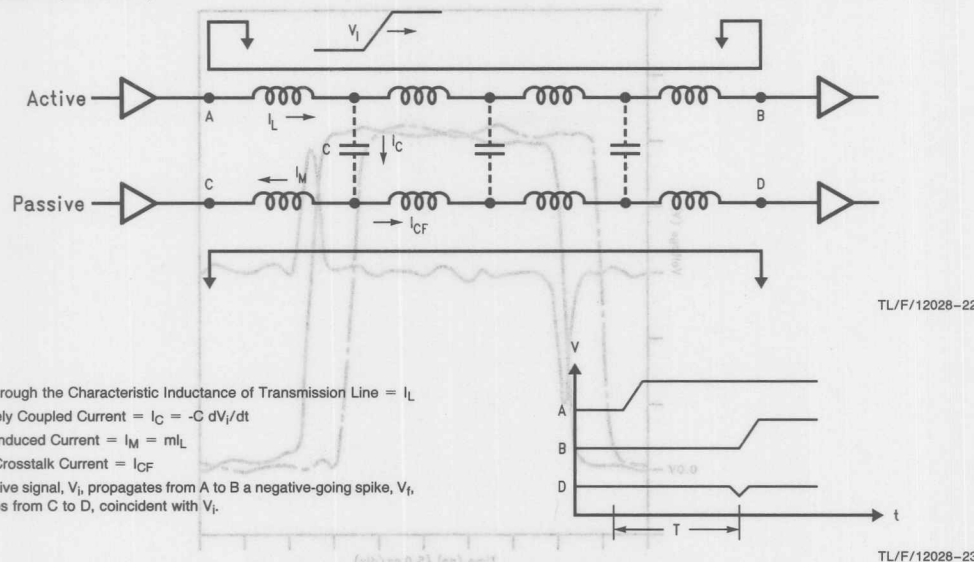


FIGURE 9. Forward Crosstalk—Refresher

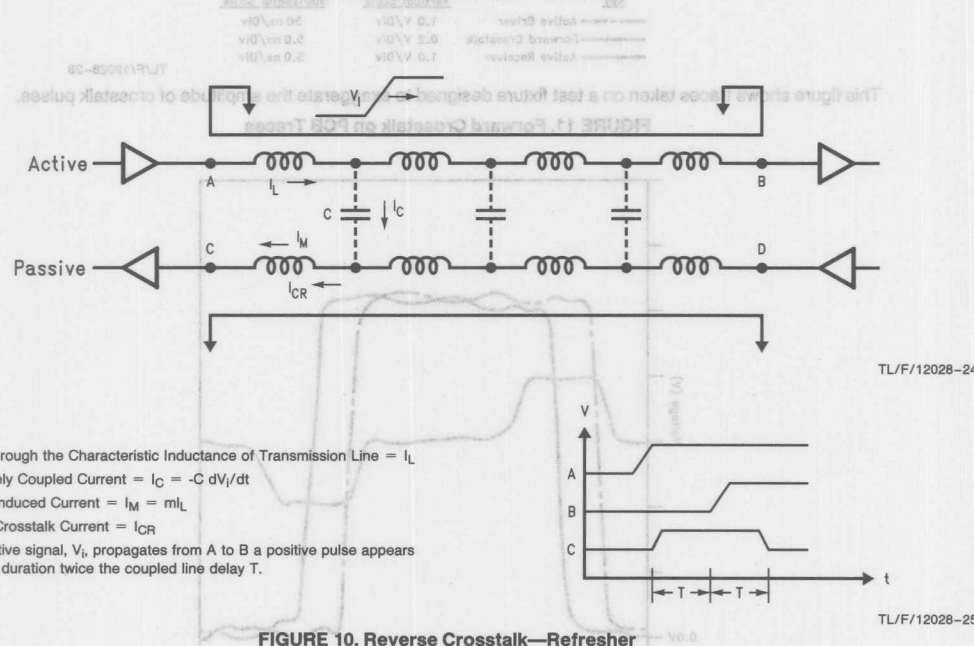
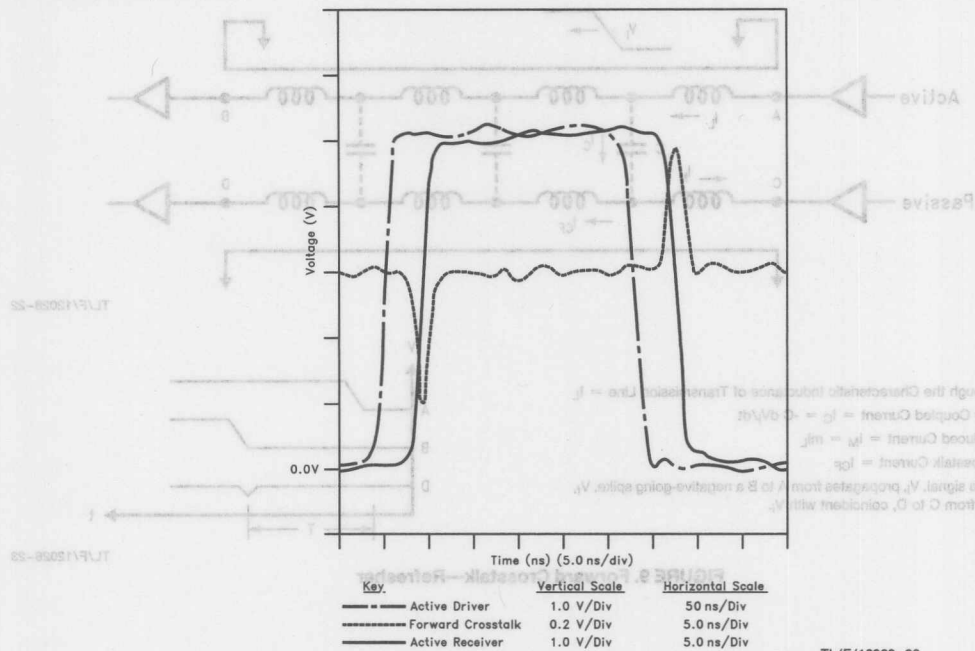


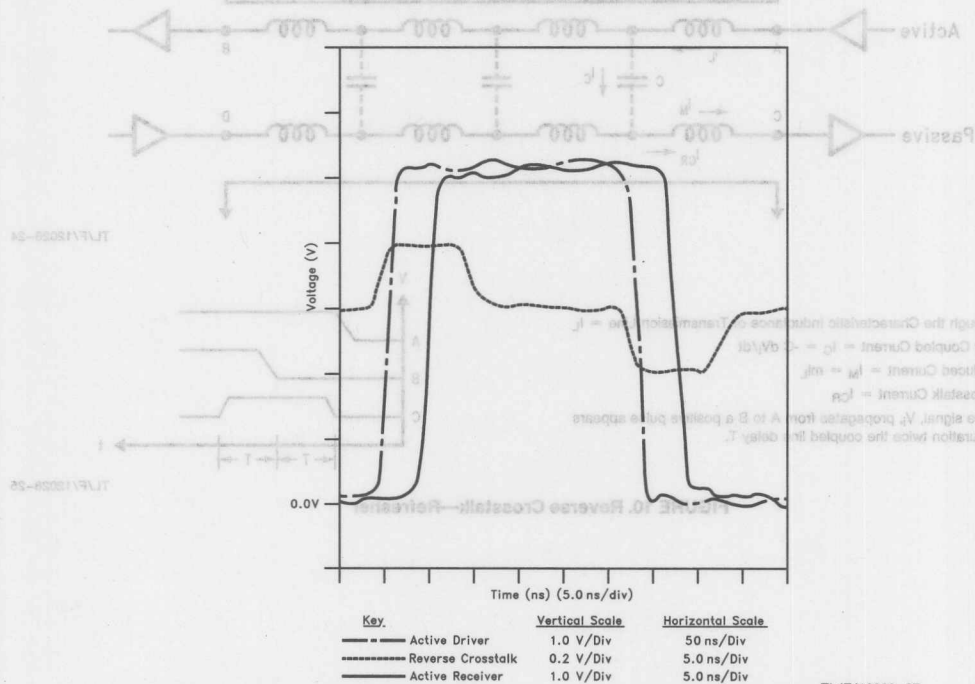
FIGURE 10. Reverse Crosstalk—Refresher

## Crosstalk (Continued)



This figure shows traces taken on a test fixture designed to exaggerate the amplitude of crosstalk pulses.

**FIGURE 11. Forward Crosstalk on PCB Traces**



This figure shows traces taken on a test fixture designed to exaggerate the amplitude of crosstalk pulses.

**FIGURE 12. Reverse Crosstalk on PCB Traces**

## Crosstalk (Continued)

In any design, the distance that lines run adjacent to each other should be kept as short as possible. The best situation is when the lines are perpendicular to each other. See Figure 13. For those situations where lines must run parallel, the effects of crosstalk can be minimized by line termina-

tion. Terminating a line in its characteristic impedance reduces the amplitude of an initial crosstalk pulse by 50%. Terminating the line will also reduce the amount of ringing. Crosstalk problems can also be reduced by moving lines further apart or by inserting ground lines or planes between them. See Figure 14.

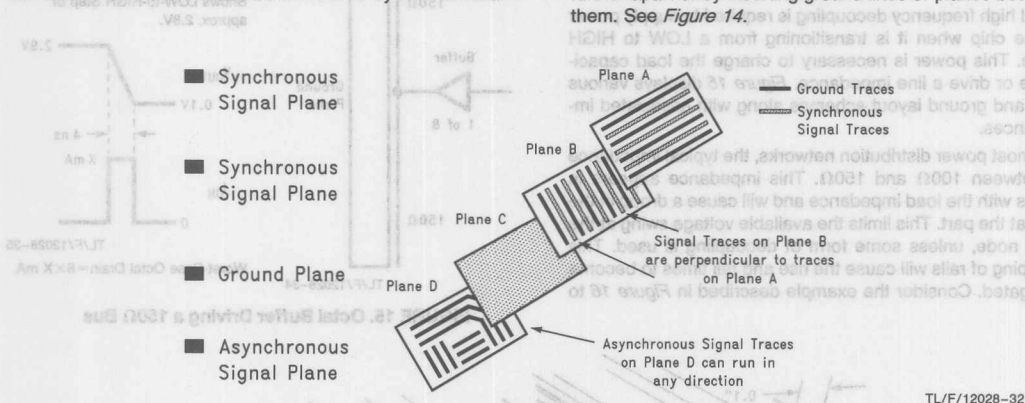


FIGURE 13. Recommended Crosstalk—Avoidance Structure

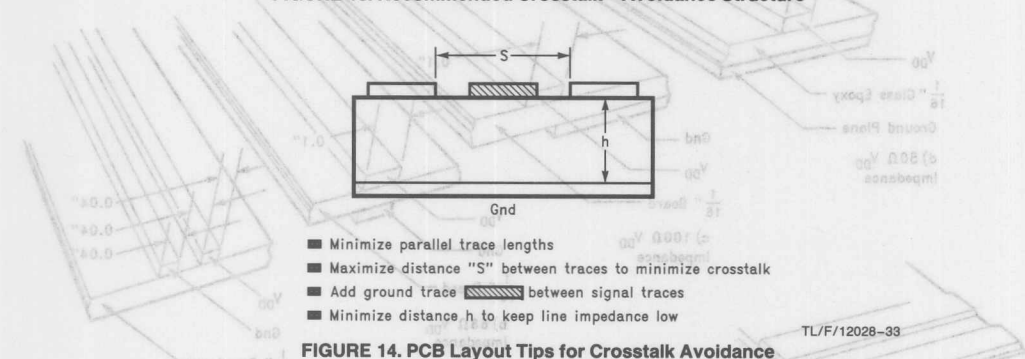


FIGURE 14. PCB Layout Tips for Crosstalk Avoidance

## Decoupling Requirements

National Semiconductor Advanced CMOS, as with other high-performance, high-drive logic families, has special decoupling and printed circuit board layout requirements. Adhering to these requirements will ensure the maximum advantages are gained with Low voltage logic products.

Local high frequency decoupling is required to supply power to the chip when it is transitioning from a LOW to HIGH value. This power is necessary to charge the load capacitance or drive a line impedance. Figure 15 displays various  $V_{DD}$  and ground layout schemes along with associated impedances.

For most power distribution networks, the typical impedance is between  $100\Omega$  and  $150\Omega$ . This impedance appears in series with the load impedance and will cause a droop in the  $V_{DD}$  at the part. This limits the available voltage swing at the local node, unless some form of decoupling is used. This drooping of rails will cause the rise and fall times to become elongated. Consider the example described in Figure 16 to

calculate the amount of decoupling necessary. This circuit utilizes a '244 driving a  $150\Omega$  bus from a point somewhere in the middle.

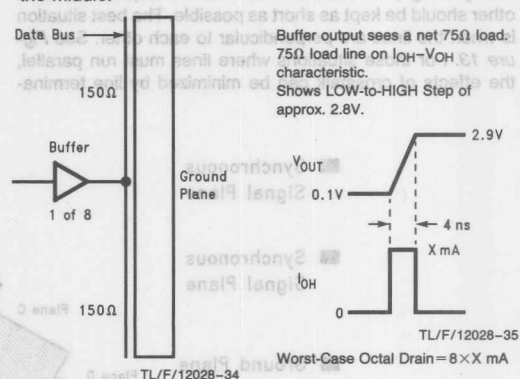


FIGURE 15. Octal Buffer Driving a  $150\Omega$  Bus

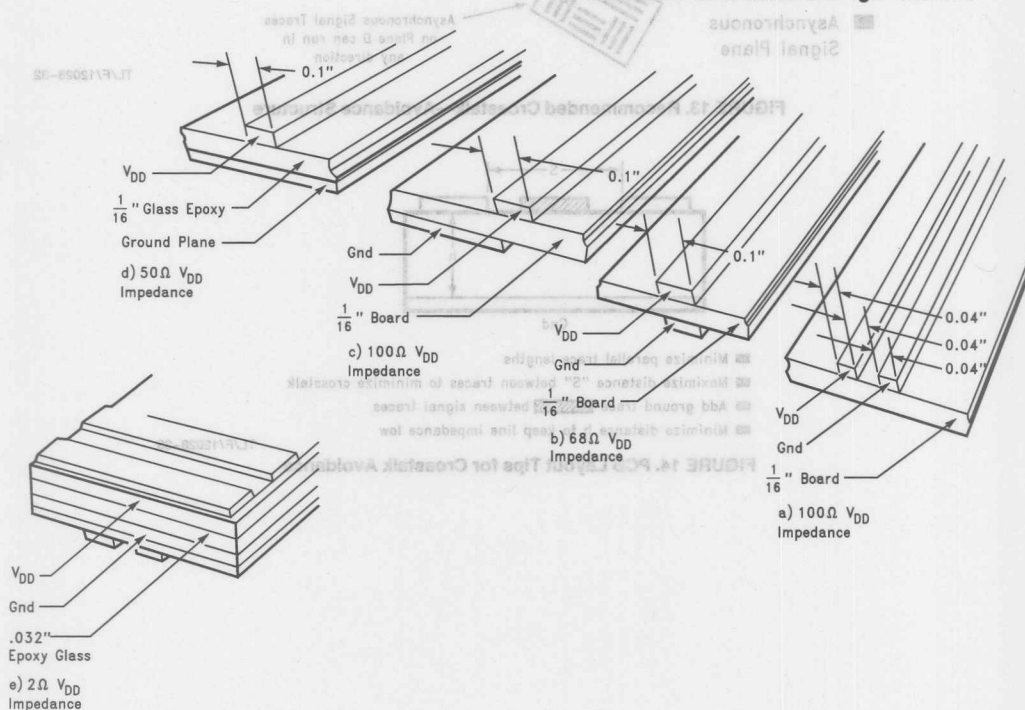


FIGURE 16. Power Distribution Impedances

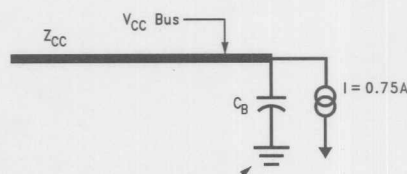
TL/F/12028-36

## Decoupling Requirements (Continued)

Being in the middle of the bus, the driver will see two 150Ω loads in parallel, or an effective impedance of 75Ω. To switch the line from rail to rail, a given drive of X mA is needed; more than X mA x 8 will be required if all eight lines switch at once. This instantaneous current requirement will generate a voltage drop across the impedance of the power lines, causing the actual  $V_{CC}$  at the chip to droop. This droop limits the voltage swing available to the driver. The net effect of the voltage droop will lengthen device rise and fall times and slow system operation. A local decoupling capacitor is required to act as a low impedance supply for the driver chip during high current conditions. It will maintain the voltage within acceptable limits and keep rise and fall times to a minimum. The necessary values for decoupling capacitors can be calculated with the formula given in Figure 17.

In this example the drive needed, if all 8 lines switch at once, is 300 mA, plus the  $V_{DD}$  droop is to be kept below 20 mV and the edge rate equals 4 ns, a 0.10 μF capacitor is needed.

It is good practice to distribute decoupling capacitors evenly through the logic, placing one capacitor for every package. See Figure 18.



$Q = CV$   
 $I = C\Delta V/\Delta t$   
 $C = I\Delta t/\Delta V$   
 $\Delta t = 4 \times 10^{-9}$

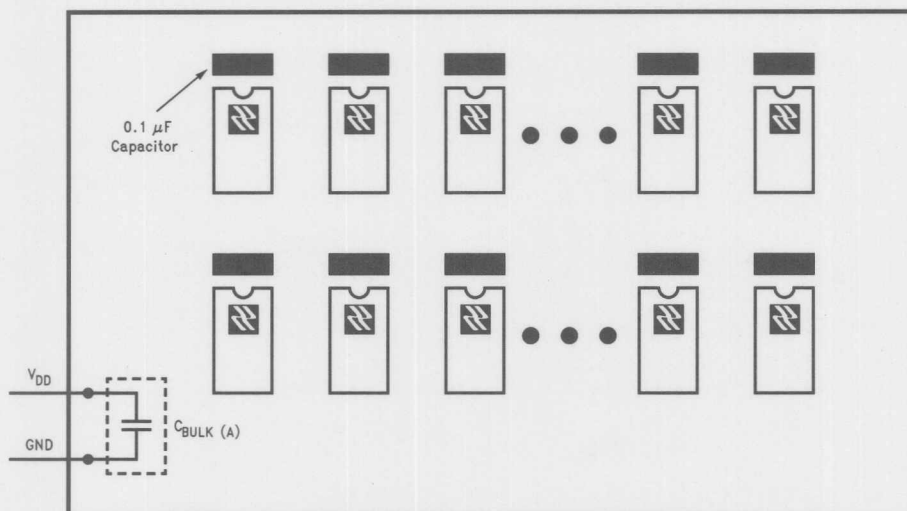
Bypass Capacitor  
Specify  $V_{CC}$  Droop c.g. 30 mV Max

TL/F/12028-37

$$C = \frac{0.3 \times 4 \times 10^{-9}}{0.02} = 60 \times 10^{-9} = 0.06 \mu F$$

Select  $C_B \geq 0.10 \mu F$

FIGURE 17. Formula for Calculating Decoupling Capacitors



TL/F/12028-38

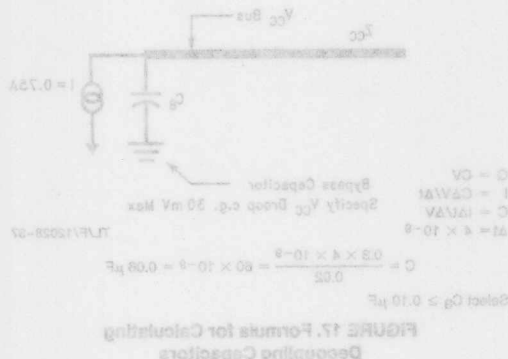
- Need to decouple board at the point of power supply entry
- This capacitor (A) will smooth low frequency bulk switching noise
- A large value electrolytic capacitor is typically used (50 μF–100 μF)

FIGURE 18. Board-Level Decoupling Capacitor

## Capacitor Types

Decoupling capacitors need to be of the high K ceramic type with low equivalent series resistance (ESR), consisting primarily of series inductance and series resistance. Capacitors

using 5ZU dielectric have suitable properties and make a good choice for decoupling capacitors; they offer minimum cost and effective performance.



## Decoupling Requirements (Continued)

Being in the middle of the bus, the driver will see two 150 $\Omega$  loads in parallel, or an effective impedance of 75 $\Omega$ . To switch the line from rail to rail, a given drive of X mA is needed; more than X mA will be required if all eight lines switch at once. This instantaneous current requirement will generate a voltage drop across the impedance of the power lines, causing the actual  $V_{CC}$  at the chip to drop. The drop limits the voltage swing available to the driver. The net effect of the voltage drop will lengthen device rise and fall times and slow system operation. A local decoupling capacitor is required to act as a low impedance supply for the driver chip during high current conditions. It will maintain the voltage within acceptable limits and keep rise and fall times to a minimum. The necessary values for decoupling capacitors can be calculated with the formulas given in Figure 17.

In this example the drive needed, if all 8 lines switch at once, is 300 mA; plus the  $V_{CC}$  drop is to be kept below 30 mV and the edge rate equals 4 ns, a 0.10  $\mu F$  capacitor is needed.

It is good practice to distribute decoupling capacitors evenly through the logic, placing one capacitor for every package. See Figure 18.

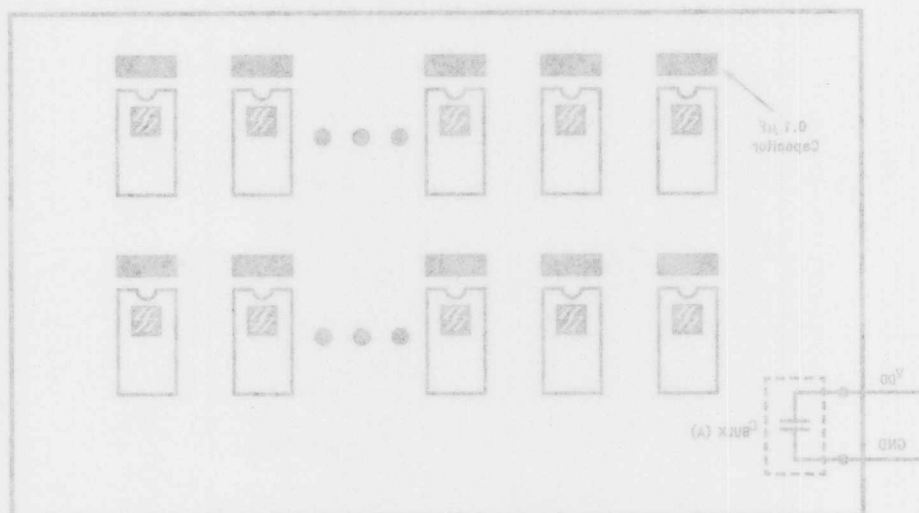


FIGURE 18. Board-Level Decoupling Capacitor

- Used to decouple board at the point of power supply entry
- This capacitor (A) will smooth low frequency bulk switching noise
- A large value electrolytic capacitor is typically used (50  $\mu F$ –100  $\mu F$ )

## Capacitor Types

Decoupling capacitors need to be of the high K ceramic type with low equivalent series resistance (ESR), consisting primarily of series inductance and series resistance. Capac-

itors using ECU dielectrics have suitable properties and make a good choice for decoupling capacitors; they offer minimum cost and effective performance.



## Section 5 Contents

LCX Family Features .....	5-3
7ALCX240 Low-Voltage Octal Buffer/Line Driver with 5V Tolerant Inputs and Outputs .....	5-4
7ALCX244 Low-Voltage Buffer/Line Driver with 5V Tolerant Inputs and Outputs .....	5-7
7ALCX245 Low-Voltage Bidirectional Transceiver with 5V Tolerant Inputs and Outputs .....	5-10
7ALCX373 Low-Voltage Octal Transparent Latch with 5V Tolerant Inputs and Outputs .....	5-14
7ALCX374 Low-Voltage Octal D Flip-Flop with 5V Tolerant Inputs and Outputs .....	5-18
7ALCX448 Low-Voltage Octal Transceiver/Register with 5V Tolerant Inputs and Outputs .....	5-22
7ALCX682 Low-Voltage Transceiver/Register with 5V Tolerant Inputs and Outputs .....	5-26
7ALCX18240 Low-Voltage 18-Bit Buffer/Line Driver with 5V Tolerant Inputs/Outputs .....	5-31
7ALCX18244 Low-Voltage 18-Bit Buffer/Line Driver with 5V Tolerant Inputs and Outputs .....	5-35
7ALCX18245 Low-Voltage 18-Bit Bidirectional Transceiver with 5V Tolerant Inputs and Outputs .....	5-39
7ALCX18373 Low-Voltage 18-Bit Transparent Latch with 5V Tolerant Inputs and Outputs .....	5-43
7ALCX18374 Low-Voltage 18-Bit D Flip-Flop with 5V Tolerant Inputs and Outputs .....	5-47
7ALCX18448 Low-Voltage 18-Bit Transceiver/Register with 5V Tolerant Inputs and Outputs .....	5-51
7ALCX18682 Low-Voltage Transceiver/Register with 5V Tolerant Inputs and Outputs .....	5-55

## Section 5 LCX Family

## Section 5 Contents

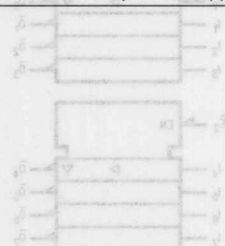
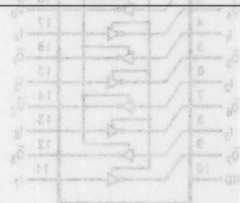
LCX Family Features .....	5-3
74LCX240 Low-Voltage Octal Buffer/Line Driver with 5V Tolerant Inputs and Outputs .....	5-4
74LCX244 Low-Voltage Buffer/Line Driver with 5V Tolerant Inputs and Outputs .....	5-7
74LCX245 Low-Voltage Bidirectional Transceiver with 5V Tolerant Inputs and Outputs .....	5-10
74LCX373 Low-Voltage Octal Transparent Latch with 5V Tolerant Inputs and Outputs .....	5-14
74LCX374 Low-Voltage Octal D Flip-Flop with 5V Tolerant Inputs and Outputs .....	5-18
74LCX646 Low-Voltage Octal Transceiver/Register with 5V Tolerant Inputs and Outputs ....	5-22
74LCX652 Low-Voltage Transceiver/Register with 5V Tolerant Inputs and Outputs .....	5-26
74LCX16240 Low-Voltage 16-Bit Inverting Buffer/Line Driver with 5V Tolerant Inputs/Outputs .....	5-31
74LCX16244 Low-Voltage 16-Bit Buffer/Line Driver with 5V Tolerant Inputs and Outputs ....	5-35
74LCX16245 Low-Voltage 16-Bit Bidirectional Transceiver with 5V Tolerant Inputs and Outputs .....	5-39
74LCX16373 Low-Voltage 16-Bit Transparent Latch with 5V Tolerant Inputs and Outputs ....	5-43
74LCX16374 Low-Voltage 16-Bit D Flip-Flop with 5V Tolerant Inputs and Outputs .....	5-47
74LCX16646 Low-Voltage 16-Bit Transceiver/Register with 5V Tolerant Inputs and Outputs .	5-51
74LCX16652 Low-Voltage Transceiver/Register with 5V Tolerant Inputs and Outputs .....	5-56

# LCX

## Low Voltage High Speed CMOS Logic

### with 5V Tolerant Inputs and Outputs

Features	Advantages
Extended $V_{CC}$ range from 2.7V to 3.6V, compatible with JEDEC Std. No. 8-1B	Fully characterized for unregulated battery operation
Advanced 0.8 $\mu\text{m}$ CMOS process	High performance with propagation delays as fast as 6.5 ns max for octals
No input-diode clamp to $V_{CC}$ . Advanced overvoltage circuit design techniques.	5V tolerant inputs and outputs. Interfaces directly to standard 5V buses and 5V devices.
Low standby current ( $I_{CC}$ 10 $\mu\text{A}$ max for octal over temp)	Saves power, extends battery life
Power down overvoltage protection	Device is protected at inputs and outputs if $V_{CC}$ drops to zero volts
$\pm 24$ mA drive current	Guaranteed incident wave switching into 50 $\Omega$ transmission lines
SOIC, EIAJ-SOIC, and TSSOP packaging	Saves board space and weight; TSSOP compatible with PCMCIA standards
Alternate sources available	Product standardization. Ensured product supply.



Pin Name	Description
$\overline{OE}$ , $\overline{OZ}$	TRI-STATE <sup>®</sup> Output Enable Inputs
$I_1$ - $I_8$	Inputs
$O_1$ - $O_8$	Outputs

Inputs		Outputs (Pins 1, 2, 14, 15, 16)
$\overline{OE}$	$I_n$	
L	L	H
L	H	L
H	X	Z

Order Number	SOIC JEDEC	SOIC EIAJ	TSSOP
7ALCX40WM	7ALCX40JL	7ALCX40JL	7ALCX40JL
7ALCX40WMX	7ALCX40JLX	7ALCX40JLX	7ALCX40JLX
See NS Package Number	M208	M209	M209

Preliminary Data: National Semiconductor reserves the right to make changes at any time without notice.



PRELIMINARY

## 74LCX240

Low-Voltage Octal Buffer/Line Driver  
with 5V Tolerant Inputs and Outputs

## General Description

The LCX240 is an inverting octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter or receiver. The device is designed for low voltage (3.3V)  $V_{CC}$  applications with capability of interfacing to a 5V signal environment.

The LCX240 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

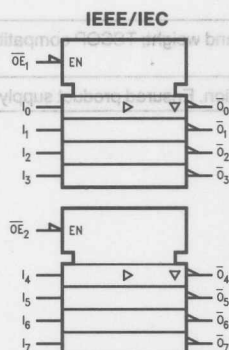
## Features

- 5V tolerant inputs and outputs
- Ideal for low power/low noise 2.7V to 3.6V applications

- Power-down static overvoltage protection on inputs and outputs
- Outputs source/sink 24 mA
- Guaranteed simultaneous switching noise level
- Available in SOIC JEDEC, SOIC EIAJ and TSSOP
- Implements patented Quiet Series noise/EMI reduction circuitry
- Functionally compatible with the 74 series 240
- Latchup performance exceeds 300 mA
- ESD performance:
  - Human body model > 2000V;
  - Machine Model > 250V

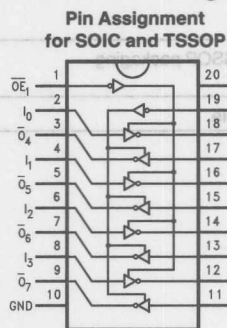
Ordering Code: See Section 11

## Logic Symbol



TL/F/11993-1

## Connection Diagram



TL/F/11993-2

Pin Names	Description
$\overline{OE}_1, \overline{OE}_2$	TRI-STATE® Output Enable Inputs
$I_0-I_7$	Inputs
$O_0-O_7$	Outputs

## Truth Tables

Inputs		Outputs (Pins 12, 14, 16, 18)
$\overline{OE}_1$	$I_n$	
L	L	H
L	H	L
H	X	Z

Inputs		Outputs (Pins 3, 5, 7, 9)
$\overline{OE}_2$	$I_n$	
L	L	H
L	H	L
H	X	Z

H = HIGH Voltage Level L = LOW Voltage Level X = Immaterial Z = High Impedance

	SOIC JEDEC	SOIC EIAJ	TSSOP
Order Number	74LCX240WM 74LCX240WMX	74LCX240SJ 74LCX240SJX	74LCX240MTCX
See NS Package Number	M20B	M20D	MTC20

Preliminary Data: National Semiconductor reserves the right to make changes at any time without notice.

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Input Voltage ( $V_I$ )	-0.5V to +7.0V
Output Voltage ( $V_O$ )	-0.5V to +7.0V
Outputs Tri-stated	-0.5V to +7.0V
Outputs Active (Note 2)	-0.5V to $V_{CC} + 0.5V$
DC Input Diode Current ( $I_{IK}$ ) $V_I < 0V$	-50 mA
DC Output Diode Current ( $I_{OK}$ )	
$V_O < 0V$	-50 mA
$V_O < V_{CC}$	+50 mA
DC Output Source/Sink Current ( $I_{OH}/I_{OL}$ )	±50 mA
DC $V_{CC}$ or Ground Current per Supply Pin ( $I_{CC}$ or $I_{GND}$ )	±100 mA
Storage Temperature Range ( $T_{STG}$ )	-65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2:  $I_O$  Absolute Maximum Rating must be observed.

**Recommended Operating Conditions**

Supply Voltage	2.0V to 3.6V
Operating	1.5V to 3.6V
Data Retention Only	0.0V to 5.5V
Input Voltage ( $V_I$ )	0.0V to 5.5V
Output Voltage ( $V_O$ )	0V to $V_{CC}$
Output in Active State	0.0V to 5.5V
Output in "OFF" State	0.0V to 5.5V
Output Current $I_{OH}/I_{OL}$	±24 mA
$V_{CC} = 3.0V$ to 3.6V	±12 mA
$V_{CC} = 2.7V$ to 3.0V	±12 mA
Free Air Operating Temperature ( $T_A$ )	-40°C to +85°C
Minimum Input Edge Rate ( $\Delta t/\Delta V$ )	10 ns/V
$V_{IN} = 0.8V$ to 0.2, $V_{CC} = 3.0V$	

**DC Electrical Characteristics**

Symbol	Parameter	$V_{CC}$ (V)	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		Units	Conditions
			Min	Max		
$V_{IH}$	High Level Input Voltage	2.7-3.6	2.0		V	$V_{OUT} \leq 0.1V$ or $\geq V_{CC} - 0.1V$
$V_{IL}$	Low Level Input Voltage	2.7-3.6		0.8	V	
$V_{OH}$	High Level Output Voltage	2.7-3.6	$V_{CC} - 0.2$		V	$I_{OH} = -100 \mu A$
		2.7	2.2		V	$I_{OH} = -12 \text{ mA}$
		3.0	2.4		V	$I_{OH} = -18 \text{ mA}$
		3.0	2.2		V	$I_{OH} = -24 \text{ mA}$
$V_{OL}$	Low Level Output Voltage	2.7-3.6		0.2	V	$I_{OL} = 100 \mu A$
		3.7		0.4	V	$I_{OL} = 12 \text{ mA}$
		3.0		0.55	V	$I_{OL} = 24 \text{ mA}$
$I_I$	Input Leakage Current	2.7-3.6		±5.0	$\mu A$	$0 \leq V_I \leq 5.5V$
$I_{OZ}$	TRI-STATE Output Leakage	2.7-3.6		±5.0	$\mu A$	$0 \leq V_O \leq 5.5V$ $V_I = V_{IH}$ or $V_{IL}$
$I_{OFF}$	Power Off Leakage Current	0		100	$\mu A$	$V_I$ or $V_O = 5.5V$
$I_{CC}$	Quiescent Supply Current	2.7-3.6		10	$\mu A$	$V_I = V_{CC}$ or GND
				±10	$\mu A$	$3.6 \leq (V_I, V_O) \leq 5.5V$
$\Delta I_{CC}$	Increase in $I_{CC}$ per Input	2.7-3.6		500	$\mu A$	$V_{IH} = V_{CC} - 0.6V$

**AC Electrical Characteristics:** See Section 2 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF		Units
			Min	Max (Note 2)	
t <sub>PHL</sub>	Propagation Delay	2.7	1.5	7.5	ns
t <sub>PLH</sub>	Data to Output	3.0–3.6	1.5	6.5	ns
t <sub>PZL</sub>	Output Enable Time	2.7	1.5	9.0	ns
t <sub>PZH</sub>		3.0–3.6	1.5	8.0	ns
t <sub>PHZ</sub>	Output Disable Time	2.7	1.5	8.0	ns
t <sub>PLZ</sub>		3.0–3.6	1.5	7.0	ns
t <sub>OSSL</sub>	Output to Output	3.0		1.0	ns
t <sub>OSHL</sub>	Skew (Note 1)				ns

**Note 1:** Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t<sub>OSSL</sub>) or LOW to HIGH (t<sub>OSHL</sub>). Parameter guaranteed by design.

**Note 2:** The maximum AC limits are design targets. Actual performance will be specified upon completion of characterization.

**Dynamic Switching Characteristics:** See Section 2 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = 25°C		Conditions
			Typical	Units	
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	3.3	0.8	V	C <sub>L</sub> = 50 pF, V <sub>IH</sub> = 3.3V, V <sub>IL</sub> = 0V
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	3.3	0.8	V	C <sub>L</sub> = 50 pF, V <sub>IH</sub> = 3.3V, V <sub>IL</sub> = 0V

**Capacitance**

Symbol	Parameter	Typical	Units	Conditions
C <sub>IN</sub>	Input Capacitance	7	pF	V <sub>CC</sub> = Open V <sub>I</sub> = 0V or V <sub>CC</sub>
C <sub>OUT</sub>	Output Capacitance	8	pF	V <sub>CC</sub> = 3.3V V <sub>I</sub> = 0V or V <sub>CC</sub>
C <sub>PD</sub>	Power Dissipation Capacitance	32	pF	V <sub>CC</sub> = 3.3V V <sub>I</sub> = 0V or V <sub>CC</sub> F = 10 MHz

V <sub>OL</sub>	Low Level Output Voltage	0.2	0.4	0.8	2.7–3.8
I <sub>I</sub>	Input Leakage Current	±0.5	±0.5	±0.5	2.7–3.8
I <sub>OL</sub>	TRI-STATE Output Leakage	±0.5	±0.5	±0.5	2.7–3.8
I <sub>OFF</sub>	Power Off Leakage Current	100			0
I <sub>CC</sub>	Quiescent Supply Current	10			2.7–3.8
ΔI <sub>CC</sub>	Increase in I <sub>CC</sub> per Input	500			2.7–3.8



## 74LCX244

### Low-Voltage Buffer/Line Driver with 5V Tolerant Inputs and Outputs

#### General Description

The LCX244 contains eight non-inverting buffers with TRI-STATE® outputs. The device may be employed as a memory address driver, clock driver and bus-oriented transmitter/receiver. The LCX244 is designed for low voltage (3.3V)  $V_{CC}$  applications with capability of interfacing to a 5V signal environment.

The LCX244 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

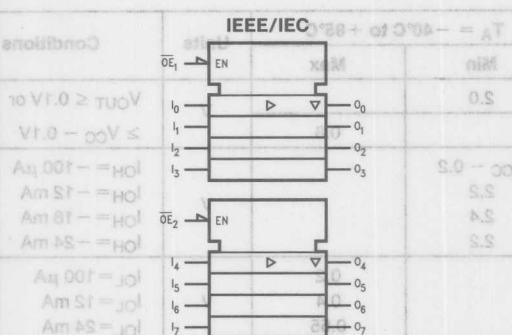
#### PRELIMINARY

#### Features

- 5V tolerant inputs and outputs
- Ideal for low power/low noise 2.7 to 3.6V applications
- Power-down static overvoltage protection on inputs and outputs
- Outputs source/sink 24 mA
- Guaranteed simultaneous switching noise level
- Available in SOIC JEDEC, SOIC EIAJ and TSSOP
- Implements patented Quiet Series noise/EMI reduction circuitry
- Functionally compatible with the 74 series 244
- Latch-up performance exceeds 300 mA
- ESD performance: Human Body Model > 2000V; Machine Model > 250V

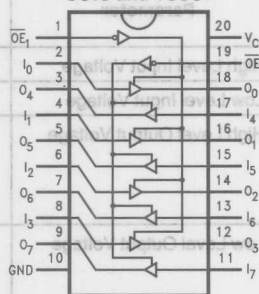
**Ordering Code:** See Section 11

#### Logic Symbol



#### Connection Diagram

Pin Assignment for  
SOIC and TSSOP



Pin Names	Description
$\overline{OE}_1, \overline{OE}_2$	TRI-STATE Output Enable Inputs
$I_0-I_7$	Inputs
$O_0-O_7$	Outputs

#### Truth Tables

Inputs		Outputs (Pins 12, 14, 16, 18)	
$\overline{OE}_1$	$I_n$		
L	L	L	
L	H	H	
H	X	Z	

Inputs		Outputs (Pins 3, 5, 7, 9)	
$\overline{OE}_2$	$I_n$		
L	L	L	
L	H	H	
H	X	Z	

H = HIGH Voltage Level X = Immaterial L = LOW Voltage Level Z = High Impedance

	SOIC JEDEC	SOIC EIAJ	TSSOP JEDEC
Order Number	74LCX244WM 74LCX244WMX	74LCX244SJ 74LCX244SJX	74LCX244MTCX
See NS Package Number	M20B	M20D	MTC20

Preliminary Data: National Semiconductor reserves the right to make changes at any time without notice.

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Input Voltage ( $V_I$ )	-0.5V to +7.0V
Output Voltage ( $V_O$ )	-0.5V to +7.0V
Outputs Tri-Stated	-0.5V to +7.0V
Outputs Active (Note 2)	-0.5V to $V_{CC} + 0.5V$
DC Input Diode Current ( $I_{IK}$ ) $V_I < 0$	-50 mA
DC Output Diode Current ( $I_{OK}$ ) $V_O < 0$	-50 mA
$V_O > V_{CC}$	+50 mA
DC Output Source/Sink Current ( $I_{OH}/I_{OL}$ )	$\pm 50$ mA
DC $V_{CC}$ or Ground Current per Supply Pin ( $I_{CC}$ or $I_{GND}$ )	$\pm 100$ mA
Storage Temperature Range ( $T_{STG}$ )	-65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2:  $I_O$  Absolute Maximum Rating must be observed.

**Recommended Operating Conditions**

Supply Voltage ( $V_{CC}$ )	2.0V to 3.6V
Operating	1.5V to 3.6V
Data Retention Only	0V to 5.5V
Input Voltage ( $V_I$ )	0V to 5.5V
Output Voltage ( $V_O$ )	0.0V to $V_{CC}$
Output in Active State	0.0V to 5.5V
Output in "OFF" State	0.0V to 5.5V
Output Current $I_{OH}/I_{OL}$	$\pm 24$ mA
$V_{CC} = 3.0V$ to $3.6V$	$\pm 12$ mA
$V_{CC} = 2.7V$ to $3.0V$	
Free Air Operating Temperature ( $T_A$ )	-40°C to +85°C
Minimum Input Edge Rate ( $\Delta t/\Delta V$ )	10 ns/V
$V_{IN} = 0.8V$ to $2.0V$ , $V_{CC} = 3.0V$	

**DC Electrical Characteristics**

Symbol	Parameter	$V_{CC}$ (V)	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		Units	Conditions
			Min	Max		
$V_{IH}$	High Level Input Voltage	2.7-3.6	2.0		V	$V_{OUT} \leq 0.1V$ or $\geq V_{CC} - 0.1V$
$V_{IL}$	Low Level Input Voltage	2.7-3.6		0.8	V	
$V_{OH}$	High Level Output Voltage	2.7-3.6 2.7 3.0 3.0	$V_{CC} - 0.2$ 2.2 2.4 2.2		V	$I_{OH} = -100 \mu\text{A}$ $I_{OH} = -12 \text{ mA}$ $I_{OH} = -18 \text{ mA}$ $I_{OH} = -24 \text{ mA}$
$V_{OL}$	Low Level Output Voltage	2.7-3.6 2.7 3.0		0.2 0.4 0.55	V	$I_{OL} = 100 \mu\text{A}$ $I_{OL} = 12 \text{ mA}$ $I_{OL} = 24 \text{ mA}$
$I_I$	Input Leakage Current	2.7-3.6		$\pm 5.0$	$\mu\text{A}$	$0 \leq V_I \leq 5.5V$
$I_{OZ}$	TRI-STATE Output Leakage	2.7-3.6		$\pm 5.0$	$\mu\text{A}$	$0 \leq V_O \leq 5.5V$ $V_I = V_{IH}$ or $V_{IL}$
$I_{OFF}$	Power Off Leakage Current	0V		100	$\mu\text{A}$	$V_I$ or $V_O = 5.5V$
$I_{CC}$	Quiescent Supply Current	2.7-3.6		10	$\mu\text{A}$	$V_I = V_{CC}$ or GND
				$\pm 10$	$\mu\text{A}$	$3.6 \leq (V_I, V_O) \leq 5.5V$
$\Delta I_{CC}$	Increase in $I_{CC}$ per Input	2.7-3.6		500	$\mu\text{A}$	$V_{IH} = V_{CC} - 0.6V$

H = High Voltage Level, X = Indeterminate, L = Low Voltage Level, Z = High Impedance

Order Number	TA10X244MM	TA10X244SL	TA10X244MTX
See NS Package Number	MS08	MS0D	MT08

Preliminary Data: National Semiconductor reserves the right to make changes at any time without notice.

**AC Electrical Characteristics:** See Section 2 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = -40°C to +85°C, C <sub>L</sub> = 50 pF		Units
			Min	Max (Note 2)	
t <sub>PHL</sub> t <sub>PLH</sub>	Propagation Delay Data to Output	2.7 3.0–3.6	1.5 1.5	7.5 6.5	ns
t <sub>PZL</sub> t <sub>PZH</sub>	Output Enable Time	2.7 3.0–3.6	1.5 1.5	9.0 8.0	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time	2.7 3.0–3.6	1.5 1.5	8.0 7.0	ns
t <sub>OSSL</sub> , t <sub>OSLH</sub>	Output to Output Skew (Note 1)	3.0		1.0	ns

**Note 1:** Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t<sub>OSSL</sub>) or LOW to HIGH (t<sub>OSLH</sub>). Parameter guaranteed by design.

**Note 2:** The maximum AC limits are design targets. Actual performance will be specified upon completion of characterization.

**Dynamic Switching Characteristics:** See Section 2 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = 25°C	Units	Conditions
			Typical		
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	3.3	0.8	V	C <sub>L</sub> = 50 pF, V <sub>IH</sub> = 3.3V, V <sub>IL</sub> = 0V
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	3.3	0.8	V	C <sub>L</sub> = 50 pF, V <sub>IH</sub> = 3.3V, V <sub>IL</sub> = 0V

**Capacitance**

Symbol	Parameter	Typical	Units	Conditions
C <sub>IN</sub>	Input Capacitance	7	pF	V <sub>CC</sub> = Open V <sub>I</sub> = 0V or V <sub>CC</sub>
C <sub>OUT</sub>	Output Capacitance	8	pF	V <sub>CC</sub> = 3.3V V <sub>I</sub> = 0V or V <sub>CC</sub>
C <sub>PD</sub>	Power Dissipation Capacitance	32	pF	V <sub>CC</sub> = 3.3V V <sub>I</sub> = 0V or V <sub>CC</sub> F = 10 MHz



## 74LCX245

### Low-Voltage Bidirectional Transceiver with 5V Tolerant Inputs and Outputs

#### General Description

The LCX245 contains eight non-inverting bidirectional buffers with TRI-STATE® outputs and is intended for bus oriented applications. The device is designed for low voltage (3.3V)  $V_{CC}$  applications with capability of interfacing to a 5V signal environment. The T/R input determines the direction of data flow through the device. The OE input disables both the A and B ports by placing them in a high impedance state.

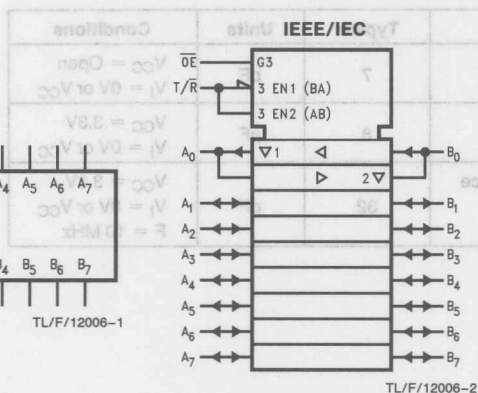
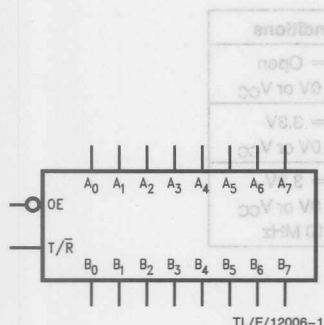
The LCX245 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

#### Features

- 5V tolerant inputs and outputs
- Ideal for low power/low noise 2.7V to 3.6V applications
- Power-down static overvoltage protection on inputs and outputs
- Outputs source/sink 24 mA
- Guaranteed simultaneous switching noise level
- Available in SOIC JEDEC, SOIC EIAJ and TSSOP
- Implements patented Quiet Series noise/EMI reduction circuitry
- Functionally compatible with the 74 series 245
- Latch performance exceeds 300 mA
- ESD performance: Human Body Model > 2000V; Machine Model > 250V

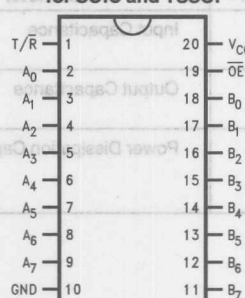
#### Ordering Code: See Section 11

#### Logic Symbols



#### Connection Diagram

##### Pin Assignment for SOIC and TSSOP



Pin Names	Description
OE	Output Enable Input
T/R	Transmit/Receive Input
A <sub>0</sub> –A <sub>7</sub>	Side A Inputs or TRI-STATE Outputs
B <sub>0</sub> –B <sub>7</sub>	Side B Inputs or TRI-STATE Outputs

	SOIC JEDEC	SOIC EIAJ	TSSOP JEDEC
Order Number	74LCX245WM 74LCX245WMX	74LCX245SJ 74LCX245SJX	74LCX245MTCX
See NS Package Number	M20B	M20D	MTC20

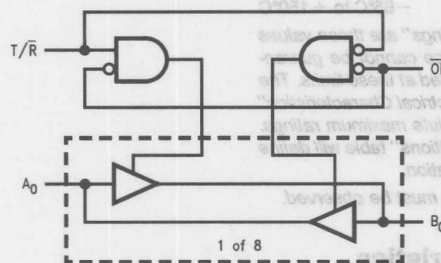
Preliminary Data: National Semiconductor reserves the right to make changes at any time without notice.

# Truth Table

Inputs		Outputs
OE	T/R	
L	L	Bus B <sub>0</sub> –B <sub>7</sub> Data to Bus A <sub>0</sub> –A <sub>7</sub>
L	H	Bus A <sub>0</sub> –A <sub>7</sub> Data to Bus B <sub>0</sub> –B <sub>7</sub>
H	X	HIGH Z State on A <sub>0</sub> –A <sub>7</sub> , B <sub>0</sub> –B <sub>7</sub>

H = High Voltage Level  
L = Low Voltage Level  
X = Immaterial  
Z = High Impedance

## Logic Diagram



Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = –40°C to +85°C		Units	Conditions
			Min	Max		
V <sub>IH</sub>	High Level Input Voltage	2.7–3.8	2.0		V	V <sub>OUT</sub> ≤ 0.1V or ≥ V <sub>CC</sub> – 0.1V
V <sub>IL</sub>	Low Level Input Voltage	2.7–3.8		0.8		
V <sub>OH</sub>	High Level Output Voltage	2.7–3.8	V <sub>CC</sub> – 0.2		V	I <sub>OH</sub> = –100 μA I <sub>OH</sub> = –12 mA I <sub>OH</sub> = –18 mA I <sub>OH</sub> = –24 mA
V <sub>OL</sub>	Low Level Output Voltage	2.7–3.8		0.2	V	I <sub>OL</sub> = 100 μA I <sub>OL</sub> = 12 mA I <sub>OL</sub> = 24 mA
I <sub>I</sub>	Input Leakage Current @ OE, T/R	2.7–3.8	±0.5		μA	0 ≤ V <sub>I</sub> ≤ 3.5V
I <sub>OS</sub>	TRI-STATE VO Leakage	2.7–3.8	±0.5		μA	0 ≤ V <sub>CC</sub> ≤ 3.5V V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>
I <sub>OFF</sub>	Power Off Leakage Current	0	100		μA	V <sub>I</sub> or V <sub>CC</sub> = 3.5V
I <sub>CC</sub>	Quiescent Supply Current	2.7–3.8	±10		μA	V <sub>I</sub> = V <sub>CC</sub> or GND
ΔI <sub>CC</sub>	Increase in I <sub>CC</sub> per Input	2.7–3.8	±10		μA	3.8 ≤ (V <sub>I</sub> or V <sub>CC</sub> ) ≤ 3.5V

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Input Voltage ( $V_I$ )	-0.5V to +7.0V
Output Voltage ( $V_O$ )	-0.5V to +7.0V
Outputs Tri-Stated	-0.5V to +7.0V
Outputs Active (Note 2)	-0.5V to $V_{CC} + 0.5V$
DC Input Diode Current ( $I_{IK}$ ) $V_I < 0$	-50 mA
DC Output Diode Current ( $I_{OK}$ )	
$V_O < 0$	-50 mA
$V_O > V_{CC}$	+50 mA
DC Output Source/Sink Current ( $I_{OH}/I_{OL}$ )	±50 mA
DC $V_{CC}$ or Ground Current per Supply Pin ( $I_{CC}$ or $I_{GND}$ )	±100 mA
Storage Temperature Range ( $T_{STG}$ )	-65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2:  $I_O$  Absolute Maximum Rating must be observed.

**Recommended Operating Conditions**

Supply Voltage	2.0V to 3.6V
Operating	1.5V to 3.6V
Data Retention Only	0V to 5.5V
Input Voltage ( $V_I$ )	0V to $V_{CC}$
Output Voltage ( $V_O$ )	0V to $V_{CC}$
Output in Active State	±24 mA
Output in "OFF" State	±12 mA
Output Current $I_{OH}/I_{OL}$	
$V_{CC} = 3.0V$ to $3.6V$	±24 mA
$V_{CC} = 2.7V$ to $3.0V$	±12 mA
Free Air Operating Temperature ( $T_A$ )	-40°C to +85°C
Minimum Input Edge Rate ( $\Delta t/\Delta V$ )	10 ns/V
$V_{IN} = 0.8V$ to $2.0V$ , $V_{CC} = 3.0V$	

**DC Electrical Characteristics**

Symbol	Parameter	$V_{CC}$ (V)	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		Units	Conditions
			Min	Max		
$V_{IH}$	High Level Input Voltage	2.7–3.6	2.0		V	$V_{OUT} \leq 0.1V$ or $\geq V_{CC} - 0.1V$
$V_{IL}$	Low Level Input Voltage	2.7–3.6		0.8	V	
$V_{OH}$	High Level Output Voltage	2.7–3.6 2.7 3.0 3.0	$V_{CC} - 0.2$ 2.2 2.4 2.2		V	$I_{OH} = -100 \mu A$ $I_{OH} = -12 \text{ mA}$ $I_{OH} = -18 \text{ mA}$ $I_{OH} = -24 \text{ mA}$
$V_{OL}$	Low Level Output Voltage	2.7–3.6 2.7 3.0		0.2 0.4 0.55	V	$I_{OL} = 100 \mu A$ $I_{OL} = 12 \text{ mA}$ $I_{OL} = 24 \text{ mA}$
$I_I$	Input Leakage Current @ $\overline{OE}$ , $T/\overline{R}$	2.7–3.6		±5.0	$\mu A$	$0 \leq V_I \leq 5.5V$
$I_{OZ}$	TRI-STATE I/O Leakage	2.7–3.6		±5.0	$\mu A$	$0 \leq V_O \leq 5.5V$ $V_I = V_{IH}$ or $V_{IL}$
$I_{OFF}$	Power Off Leakage Current	0		100	$\mu A$	$V_I$ or $V_O = 5.5V$
$I_{CC}$	Quiescent Supply Current	2.7–3.6		10 ±10	$\mu A$	$V_I = V_{CC}$ or GND $3.6 \leq (V_I, V_O) \leq 5.5V$
$\Delta I_{CC}$	Increase in $I_{CC}$ per Input	2.7–3.6		500	$\mu A$	$V_{IH} = V_{CC} - 0.6V$

			Min	Max (Note 2)	
$t_{PHL}$	Propagation Delay	2.7	1.5	8.0	ns
$t_{PLH}$	$A_n$ to $B_n$ or $B_n$ to $A_n$	3.0–3.6	1.5	7.0	ns
$t_{PZL}$	Output Enable Time	2.7	1.5	9.5	ns
$t_{PZH}$		3.0–3.6	1.5	8.5	ns
$t_{PHZ}$	Output Disable Time	2.7	1.5	8.5	ns
$t_{PLZ}$		3.0–3.6	1.5	7.5	ns
$t_{OSH}$ $t_{OSLH}$	Output to Output Skew (Note 1)	3.0		1.0	ns

**Note 1:** Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW ( $t_{OSH}$ ) or LOW to HIGH ( $t_{OSLH}$ ). Parameter guaranteed by design.

**Note 2:** The maximum AC limits are design targets. Actual performance will be specified upon completion of characterization.

## Dynamic Switching Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	$V_{CC}$ (V)	$T_A = 25^\circ C$ Typical	Units	Conditions
$V_{OLP}$	Quiet Output Maximum Dynamic $V_{OL}$	3.3	0.8	V	$C_L = 50$ pF, $V_{IH} = 3.3$ V, $V_{IL} = 0$ V
$V_{OLV}$	Quiet Output Minimum Dynamic $V_{OL}$	3.3	0.8	V	$C_L = 50$ pF, $V_{IH} = 3.3$ V, $V_{IL} = 0$ V

## Capacitance

Symbol	Parameter	Typical	Units	Conditions
$C_{IN}$	Input Capacitance	7	pF	$V_{CC} = \text{Open}$ $V_I = 0$ V or $V_{CC}$
$C_{I/O}$	Input/Output Capacitance	8	pF	$V_{CC} = 3.3$ V $V_I = 0$ V or $V_{CC}$
$C_{PD}$	Power Dissipation Capacitance	32	pF	$V_{CC} = 3.3$ V $V_I = 0$ V or $V_{CC}$ $F = 10$ MHz



PRELIMINARY

## 74LCX373

### Low-Voltage Octal Transparent Latch with 5V Tolerant Inputs and Outputs

#### General Description

The LCX373 consists of eight latches with TRI-STATE® outputs for bus organized system applications. The device is designed for low voltage (3.3V)  $V_{CC}$  applications with capability of interfacing to a 5V signal environment.

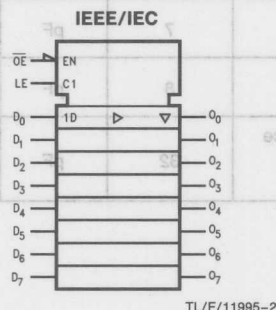
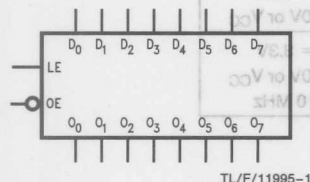
The LCX373 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

#### Features

- 5V tolerant inputs and outputs
- Ideal for low power/low noise 2.7V to 3.6V applications
- Power-down static overvoltage protection on inputs and outputs
- Outputs source/sink 24 mA
- Guaranteed simultaneous switching noise level
- Available in SOIC JEDEC, SOIC EIAJ and TSSOP
- Implements patented Quiet Series noise/EMI reduction circuitry
- Functionally compatible with the 74 series 373
- Latchup performance exceeds 300 mA
- ESD performance:
  - Human Body Model > 2000V
  - Machine Model > 250V

**Ordering Code:** See Section 11

#### Logic Symbols



#### Connection Diagram

##### Pin Assignment for SOIC and TSSOP



Pin Names	Description
$D_0$ – $D_7$	Data Inputs
LE	Latch Enable Input
$\overline{OE}$	Output Enable Input
$Q_0$ – $Q_7$	TRI-STATE Latch Outputs

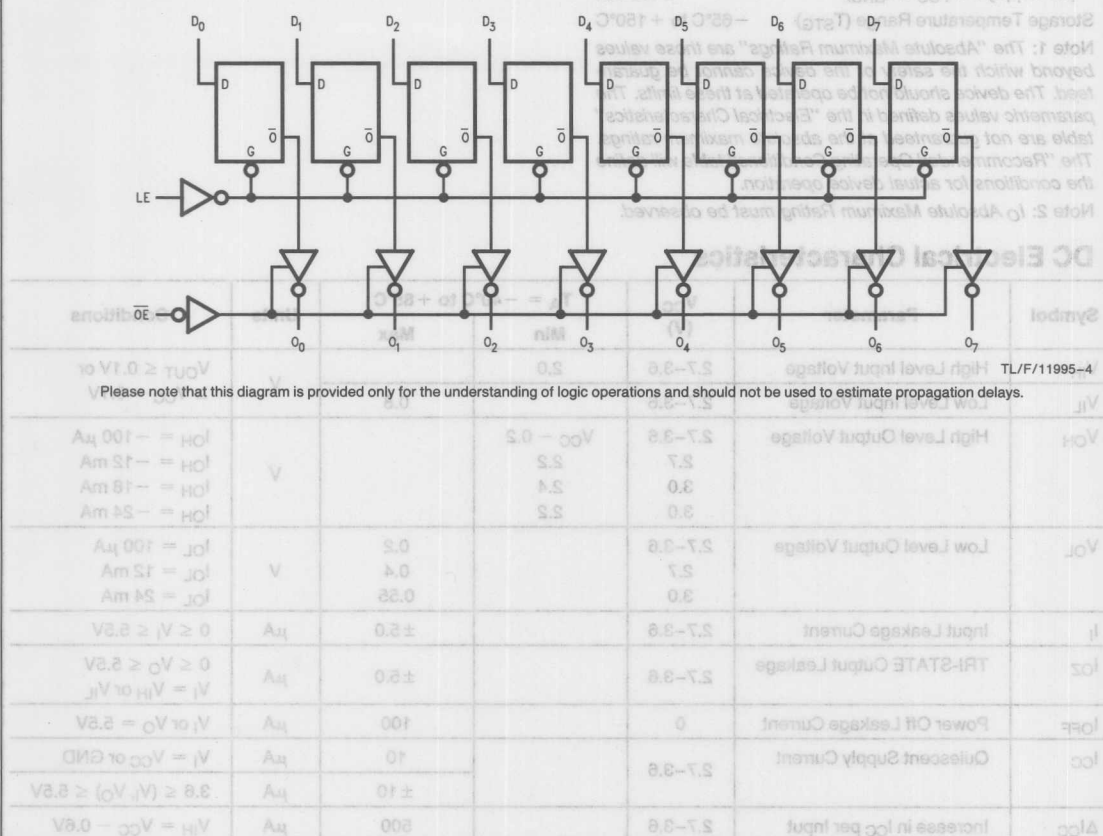
	SOIC JEDEC	SOIC EIAJ	TSSOP JEDEC
Order Number	74LCX373WM 74LCX373WMX	74LCX373SJ 74LCX373SJX	74LCX373MTCX
See NS Package Number	M20B	M20D	MTC20

Preliminary Data: National Semiconductor reserves the right to make changes at any time without notice.

## Functional Description

The LCX373 contains eight D-type latches with TRI-STATE standard outputs. When the Latch Enable (LE) input is HIGH, data on the  $D_n$  inputs enters the latches. In this condition the latches are transparent, i.e. a latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE standard outputs are controlled by the Output Enable ( $\overline{OE}$ ) input. When  $\overline{OE}$  is LOW, the standard outputs are in the 2-state mode. When  $\overline{OE}$  is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

## Logic Diagram



**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Input Voltage ( $V_I$ )	-0.5V to +7.0V
Output Voltage ( $V_O$ )	
Outputs TRI-STATE	-0.5V to +7.0V
Outputs Active (Note 2)	-0.5V to $V_{CC} + 0.5V$
DC Input Diode Current ( $I_{IK}$ ) $V_I < 0$	50 mA
DC Output Diode Current ( $I_{OK}$ )	
$V_O < 0$	-50 mA
$V_O > V_{CC}$	+50 mA
DC Output Source/Sink Current ( $I_{OH}/I_{OL}$ )	$\pm 50$ mA
DC $V_{CC}$ or Ground Current per Supply Pin ( $I_{CC}$ or $I_{GND}$ )	$\pm 100$ mA
Storage Temperature Range ( $T_{STG}$ )	-65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2:  $I_O$  Absolute Maximum Rating must be observed.

**DC Electrical Characteristics**

Symbol	Parameter	$V_{CC}$ (V)	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		Units	Conditions
			Min	Max		
$V_{IH}$	High Level Input Voltage	2.7-3.6	2.0		V	$V_{OUT} \leq 0.1V$ or $\geq V_{CC} - 0.1V$
$V_{IL}$	Low Level Input Voltage	2.7-3.6		0.8		
$V_{OH}$	High Level Output Voltage	2.7-3.6 2.7 3.0 3.0	$V_{CC} - 0.2$ 2.2 2.4 2.2		V	$I_{OH} = -100 \mu\text{A}$ $I_{OH} = -12 \text{ mA}$ $I_{OH} = -18 \text{ mA}$ $I_{OH} = -24 \text{ mA}$
$V_{OL}$	Low Level Output Voltage	2.7-3.6 2.7 3.0		0.2 0.4 0.55	V	$I_{OL} = 100 \mu\text{A}$ $I_{OL} = 12 \text{ mA}$ $I_{OL} = 24 \text{ mA}$
$I_I$	Input Leakage Current	2.7-3.6		$\pm 5.0$	$\mu\text{A}$	$0 \leq V_I \leq 5.5V$
$I_{OZ}$	TRI-STATE Output Leakage	2.7-3.6		$\pm 5.0$	$\mu\text{A}$	$0 \leq V_O \leq 5.5V$ $V_I = V_{IH}$ or $V_{IL}$
$I_{OFF}$	Power Off Leakage Current	0		100	$\mu\text{A}$	$V_I$ or $V_O = 5.5V$
$I_{CC}$	Quiescent Supply Current	2.7-3.6		10 $\pm 10$	$\mu\text{A}$	$V_I = V_{CC}$ or GND $3.6 \leq (V_I, V_O) \leq 5.5V$
$\Delta I_{CC}$	Increase in $I_{CC}$ per Input	2.7-3.6		500	$\mu\text{A}$	$V_{IH} = V_{CC} - 0.6V$

**Recommended Operating Conditions**

Supply Voltage	
Operating	2.0V to 3.6V
Data Retention Only	1.5V to 3.6V
Input Voltage ( $V_I$ )	0V to 5.5V
Output Voltage ( $V_O$ )	
Output in Active State	0V to $V_{CC}$
Output in "OFF" State	0V to 5.5V
Output Current $I_{OH}/I_{OL}$	
$V_{CC} = 3.0V$ to $3.6V$	$\pm 24$ mA
$V_{CC} = 2.7V$ to $3.0V$	$\pm 12$ mA
Free Air Operating Temperature ( $T_A$ )	-40°C to +85°C
Minimum Input Edge Rate ( $\Delta t/\Delta V$ )	
$V_{IN} = 0.8V$ to $2.0V$ , $V_{CC} = 3.0V$	10 ns/V

**AC Electrical Characteristics:** See Section 2 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF		Units
			Min	Max (Note 2)	
t <sub>PHL</sub>	Propagation Delay	2.7	1.5	9.0	ns
t <sub>PLH</sub>	D <sub>n</sub> to O <sub>n</sub>	3.0–3.6	1.5	8.0	
t <sub>PHL</sub>	Propagation Delay	2.7	1.5	9.5	ns
t <sub>PLH</sub>	LE to O <sub>n</sub>	3.0–3.6	1.5	8.5	
t <sub>PZH</sub>	Output Enable Time	2.7	1.5	9.5	ns
t <sub>PZL</sub>		3.0–3.6	1.5	8.5	
t <sub>PHZ</sub>	Output Disable Time	2.7	1.5	8.5	ns
t <sub>PLZ</sub>		3.0–3.6	1.5	7.5	
t <sub>s</sub>	Setup Time D <sub>n</sub> to LE	2.7 3.0–3.6	2.5 2.5		ns
t <sub>H</sub>	Hold Time D <sub>n</sub> to LE	2.7 3.0–3.6	1.5 1.5		
t <sub>w</sub>	LE Pulse Width	2.7 3.0–3.6	4.0 4.0		ns
t <sub>OSHL</sub> t <sub>OSLH</sub>	Output to Output Skew (Note 1)	3.0		1.0	

**Note 1:** Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t<sub>OSHL</sub>) or LOW to HIGH (t<sub>OSLH</sub>). Parameter guaranteed by design.

**Note 2:** The maximum AC limits are design targets. Actual performance will be specified upon completion of characterization.

**Dynamic Switching Characteristics:** See Section 2 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = 25°C	Units	Conditions
			Typical		
V <sub>OLP</sub>	Quiet Output Dynamic Peak V <sub>OL</sub>	3.3	0.8	V	C <sub>L</sub> = 50 pF, V <sub>IH</sub> = 3.3V, V <sub>IL</sub> = 0V
V <sub>OLV</sub>	Quiet Output Dynamic Valley V <sub>OL</sub>	3.3	0.8	V	C <sub>L</sub> = 50 pF, V <sub>IH</sub> = 3.3V, V <sub>IL</sub> = 0V

**Capacitance**

Symbol	Parameter	Typical	Units	Conditions
C <sub>IN</sub>	Input Capacitance	7	pF	V <sub>CC</sub> = Open V <sub>I</sub> = 0V or V <sub>CC</sub>
C <sub>OUT</sub>	Output Capacitance	12	pF	V <sub>CC</sub> = 3.3V V <sub>I</sub> = 0V or V <sub>CC</sub>
C <sub>PD</sub>	Power Dissipation Capacitance	32	pF	V <sub>CC</sub> = 3.3V V <sub>I</sub> = 0V or V <sub>CC</sub> F = 10 MHz

**Note 1:** Guaranteed by design.



PRELIMINARY

## 74LCX374

### Low-Voltage Octal D Flip-Flop with 5V Tolerant Inputs and Outputs

#### General Description

The LCX374 consists of eight D-type flip-flops featuring separate D-type inputs for each flip-flop and TRI-STATE® outputs for bus-oriented applications. A buffered clock (CP) and Output Enable ( $\overline{OE}$ ) are common to all flip-flops. The LCX374 is designed for low-voltage (3.3V)  $V_{CC}$  applications with capability of interfacing to a 5V signal environment.

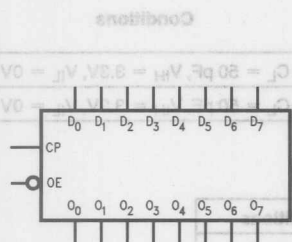
The LCX374 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

#### Features

- 5V tolerant inputs and outputs
- Ideal for low power/low noise 2.7V to 3.6V applications
- Power-down static overvoltage protection on inputs and outputs
- Outputs source/sink 24 mA
- Guaranteed simultaneous switching noise level
- Available in SOIC JEDEC, SOIC EIAJ and TSSOP
- Implements patented Quiet Series noise/EMI reduction circuitry
- Functionally compatible with the 74 series 374
- Latchup performance exceeds 300 mA
- ESD performance:  
Human Body Model > 2000V  
Machine Model > 250V

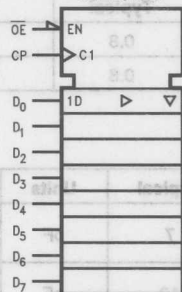
**Ordering Code:** See Section 11

#### Logic Symbols



TL/F/11996-1

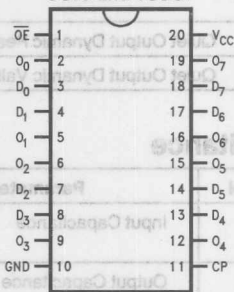
#### IEEE/IEC



TL/F/11996-2

#### Connection Diagram

##### Pin Assignment for SOIC and TSSOP



TL/F/11996-3

Pin Names	Description
D <sub>0</sub> -D <sub>7</sub>	Data Inputs
CP	Clock Pulse Input
$\overline{OE}$	Output Enable Input
Q <sub>0</sub> -Q <sub>7</sub>	TRI-STATE Outputs

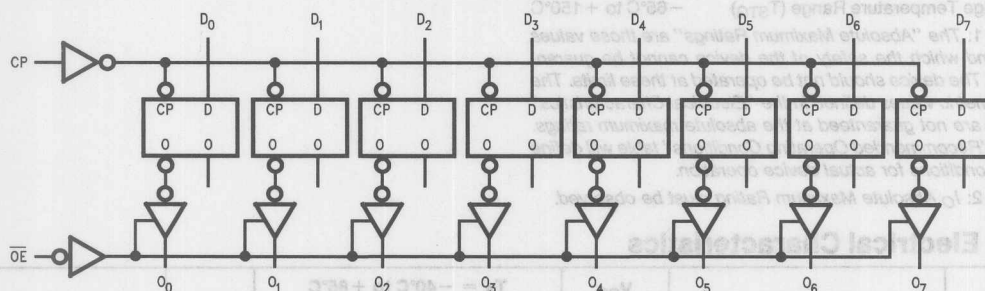
	SOIC JEDEC	SOIC EIAJ	TSSOP JEDEC
Order Number	74LCX374WM 74LCX374WMX	74LCX374SJ 74LCX374SJX	74LCX374MTCX
See NS Package Number	M20B	M20D	MTC20

Preliminary Data: National Semiconductor reserves the right to make changes at any time without notice.

## Functional Description

The LCX374 consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ( $\overline{OE}$ ) LOW, the contents of the eight flip-flops are available at the outputs. When the  $\overline{OE}$  is HIGH, the outputs go to the high impedance state. Operation of the  $\overline{OE}$  input does not affect the state of the flip-flops.



## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.				
V <sub>ih</sub>	High Level Input Voltage	2.7-3.8	2.0	V <sub>ih</sub> ≥ 2.0 V
V <sub>il</sub>	Low Level Input Voltage	2.7-3.8	0.8	V <sub>il</sub> ≤ 0.8 V
V <sub>oh</sub>	High Level Output Voltage	2.7-3.8	V <sub>oh</sub> - 0.2	I <sub>oh</sub> = -100 μA I <sub>oh</sub> = -12 mA I <sub>oh</sub> = -18 mA I <sub>oh</sub> = -24 mA
V <sub>ol</sub>	Low Level Output Voltage	2.7-3.8	0.2	I <sub>ol</sub> = 100 μA I <sub>ol</sub> = 12 mA I <sub>ol</sub> = 24 mA
I <sub>l</sub>	Input Leakage Current	2.7-3.8	±2.0	0 ≤ V <sub>i</sub> ≤ 3.8 V
I <sub>os</sub>	TRI-STATE Output Leakage	2.7-3.8	±2.0	0 ≤ V <sub>o</sub> ≤ 3.8 V V <sub>i</sub> = V <sub>ih</sub> or V <sub>il</sub>
I <sub>off</sub>	Power Off Leakage Current	0	100	V <sub>i</sub> or V <sub>o</sub> = 3.8 V
I <sub>cc</sub>	Quiescent Supply Current	2.7-3.8	10	V <sub>i</sub> = V <sub>CC</sub> or GND
			±10	3.8 ≤ (V <sub>i</sub> V <sub>o</sub> ) ≤ 3.8 V
I <sub>ic</sub>	Increase in I <sub>cc</sub> per input	2.7-3.8	500	V <sub>ih</sub> (V <sub>CC</sub> - 0.8 V)

## Truth Table

Inputs			Outputs
D <sub>n</sub>	CP	OE	O <sub>n</sub>
H		L	H
L		L	L
X	L	L	O <sub>0</sub>
X	X	H	Z

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial  
Z = High Impedance  
↘ = LOW-to-HIGH Transition  
O<sub>0</sub> = Previous O<sub>0</sub> before HIGH to LOW of CP

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Input Voltage ( $V_I$ )	-0.5V to +7.0V
Output Voltage ( $V_O$ )	-0.5V to +7.0V
Outputs TRI-STATE	-0.5V to $V_{CC} + 0.5V$
Outputs Active (Note 2)	-0.5V to $V_{CC} + 0.5V$
DC Input Diode Current ( $I_{IK}$ ) $V_I < 0$	-50 mA
DC Output Diode Current ( $I_{OK}$ )	-50 mA
$V_O < 0$	-50 mA
$V_O > V_{CC}$	+50 mA
DC Output Source/Sink Current ( $I_{OH}/I_{OL}$ )	$\pm 50$ mA
DC $V_{CC}$ or Ground Current per Supply Pin ( $I_{CC}$ or $I_{GND}$ )	$\pm 100$ mA
Storage Temperature Range ( $T_{STG}$ )	-65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2:  $I_O$  Absolute Maximum Rating must be observed.

**DC Electrical Characteristics**

Symbol	Parameter	$V_{CC}$ (V)	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		Units	Conditions
			Min	Max		
$V_{IH}$	High Level Input Voltage	2.7-3.6	2.0		V	$V_{OUT} \leq 0.1V$ or $\geq V_{CC} - 0.1V$
$V_{IL}$	Low Level Input Voltage	2.7-3.6		0.8		
$V_{OH}$	High Level Output Voltage	2.7-3.6	$V_{CC} - 0.2$		V	$I_{OH} = -100 \mu A$
		2.7	2.2			$I_{OH} = -12 \text{ mA}$
		3.0	2.4			$I_{OH} = -18 \text{ mA}$
		3.0	2.2			$I_{OH} = -24 \text{ mA}$
$V_{OL}$	Low Level Output Voltage	2.7-3.6		0.2	V	$I_{OL} = 100 \mu A$
		2.7		0.4		$I_{OL} = 12 \text{ mA}$
		3.0		0.55		$I_{OL} = 24 \text{ mA}$
$I_I$	Input Leakage Current	2.7-3.6		$\pm 5.0$	$\mu A$	$0 \leq V_I \leq 5.5V$
$I_{OZ}$	TRI-STATE Output Leakage	2.7-3.6		$\pm 5.0$	$\mu A$	$0 \leq V_O \leq 5.5V$ $V_I = V_{IH}$ or $V_{IL}$
$I_{OFF}$	Power Off Leakage Current	0		100	$\mu A$	$V_I$ or $V_O = 5.5V$
$I_{CC}$	Quiescent Supply Current	2.7-3.6		10	$\mu A$	$V_I = V_{CC}$ or GND
				$\pm 10$	$\mu A$	$3.6 \leq (V_I, V_O) \leq 5.5V$
$\Delta I_{CC}$	Increase in $I_{CC}$ per Input	2.7-3.6		500	$\mu A$	$V_{IH} = V_{CC} - 0.6V$

**Recommended Operating Conditions**

Supply Voltage	2.0V to 3.6V
Operating	1.5V to 3.6V
Data Retention Only	0V to 5.5V
Input Voltage ( $V_I$ )	0V to 5.5V
Output Voltage ( $V_O$ )	0V to $V_{CC}$
Output in Active State	0V to 5.5V
Output in "OFF" State	0V to 5.5V
Output Current $I_{OH}/I_{OL}$	$\pm 24$ mA
$V_{CC} = 3.0V$ to $3.6V$	$\pm 12$ mA
$V_{CC} = 2.7V$ to $3.0V$	
Free Air Operating Temperature ( $T_A$ )	-40°C to +85°C
Minimum Input Edge Rate ( $\Delta t/\Delta V$ )	10 ns/V
$V_{IN} = 0.8V$ to $2.0V$ , $V_{CC} = 3.0V$	

**AC Electrical Characteristics:** See Section 2 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF		Units
			Min	Max (Note 2)	
t <sub>PHL</sub>	Propagation Delay	2.7	1.5	9.5	ns
t <sub>PLH</sub>	CP to Output	3.0-3.6	1.5	8.5	
t <sub>PZH</sub>	Output Enable Time	2.7	1.5	9.5	ns
t <sub>PZL</sub>		3.0-3.6	1.5	8.5	
t <sub>PHZ</sub>	Output Disable Time	2.7	1.5	8.5	ns
t <sub>PLZ</sub>		3.0-3.6	1.5	7.5	
t <sub>s</sub>	Setup Time	2.7	2.5		ns
		3.0-3.6	2.5		
t <sub>H</sub>	Hold Time	2.7	1.5		ns
		3.0-3.6	1.5		
t <sub>w</sub>	Pulse Width	2.7	4.0		ns
		3.0-3.6	4.0		
t <sub>OSHL</sub> , t <sub>OSLH</sub>	Output to Output Skew (Note 1)	3.0		1.0	ns

**Note 1:** Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t<sub>OSHL</sub>) or LOW to HIGH (t<sub>OSLH</sub>). Parameter guaranteed by design.

**Note 2:** The maximum AC limits are design targets. Actual performance will be specified upon completion of characterization.

**Dynamic Switching Characteristics:** See Section 2 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = 25°C	Units	Conditions
			Typical		
V <sub>OLP</sub>	Quiet Output Dynamic Peak V <sub>OL</sub>	3.3	0.8	V	C <sub>L</sub> = 50 pF, V <sub>IH</sub> = 3.3V, V <sub>IL</sub> = 0V
V <sub>OLV</sub>	Quiet Output Dynamic Valley V <sub>OL</sub>	3.3	0.8	V	C <sub>L</sub> = 50 pF, V <sub>IH</sub> = 3.3V, V <sub>IL</sub> = 0V

**Capacitance**

Symbol	Parameter	Typical	Units	Conditions
C <sub>IN</sub>	Input Capacitance	7	pF	V <sub>CC</sub> = Open V <sub>I</sub> = 0V or V <sub>CC</sub>
C <sub>OUT</sub>	Output Capacitance	8	pF	V <sub>CC</sub> = 3.3V V <sub>I</sub> = 0V or V <sub>CC</sub>
C <sub>PD</sub>	Power Dissipation Capacitance	32	pF	V <sub>CC</sub> = 3.3V V <sub>I</sub> = 0V or V <sub>CC</sub> F = 10 MHz



# 74LCX646 Low-Voltage Octal Transceiver/Register with 5V Tolerant Inputs and Outputs

## General Description

The LCX646 consists of registered bus transceiver circuits, with outputs, D-type flip-flops, and control circuitry providing multiplexed transmission of data directly from the input bus or from the internal storage registers. Data on the A or B bus will be loaded into the respective registers on the LOW-to-HIGH transition of the appropriate pin (CPAB or CPBA). The four fundamental handling functions available are illustrated in Figure 1 through Figure 4.

The LCX646 is designed for low voltage (3.3V)  $V_{CC}$  applications with capability of interfacing to a 5V signal environment.

The LCX646 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

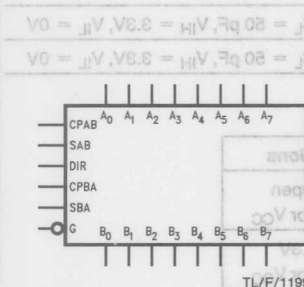
## Features

- 5V tolerant inputs and outputs
- Ideal for low power/low noise 2.7V to 3.6V applications
- Power-down static overvoltage protection on inputs and outputs
- Outputs source/sink 24 mA
- Guaranteed simultaneous switching noise level
- Available in SOIC JEDEC and TSSOP
- Implements patented Quiet Series noise/EMI reduction circuitry
- Functionally compatible with the 74 series 646
- Latch performance exceeds 300 mA

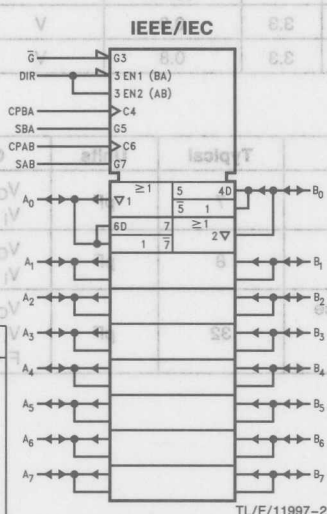
- ESD performance:  
Human body Model > 2000V  
Machine Model > 250V

Ordering Code: See Section 11

## Logic Symbols

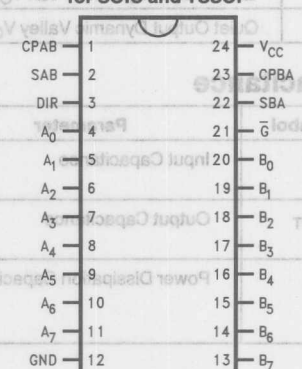


Pin Names	Description
A <sub>0</sub> -A <sub>7</sub>	Data Register A Inputs
B <sub>0</sub> -B <sub>7</sub>	Data Register B Inputs
CPAB, CPBA	Clock Pulse Inputs
SAB, SBA	Transmit/Receive Inputs
$\bar{G}$	Output Enable Input
DIR	Direction Control Input



## Connection Diagram

Pin Assignment for SOIC and TSSOP

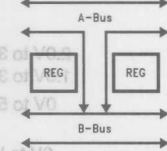


TL/F/11997-3

	SOIC JEDEC	TSSOP JEDEC
Order Number	74LCX646WM 74LCX646WMX	74LCX646MTCX
See NS Package Number	M24B	MTC24

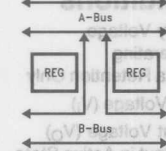
Preliminary Data: National Semiconductor reserves the right to make changes at any time without notice.

Real Time Transfer  
A-Bus to B-Bus



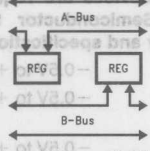
TL/F/11997-4  
FIGURE 1

Real Time Transfer  
B-Bus to A-Bus



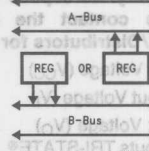
TL/F/11997-5  
FIGURE 2

Storage from  
Bus to Register



TL/F/11997-6  
FIGURE 3

Transfer from  
Register to Bus



TL/F/11997-7  
FIGURE 4

Function Table (Note)

Inputs					Data I/O		Function
$\bar{G}_n$	DIR	CPAB	CPBA	SAB	SBA	A <sub>0</sub> -A <sub>7</sub> B <sub>0</sub> -B <sub>7</sub>	
H	X	H or L	H or L	X	X	Input	Isolation
H	X	X	X	X	X		Clock A <sub>n</sub> Data into A Register
H	X	X	X	X	X		Clock B <sub>n</sub> Data into B Register
L	H	X	X	L	X	Input	A <sub>n</sub> to B <sub>n</sub> —Real Time (Transparent Mode)
L	H	X	X	L	X		Clock A <sub>n</sub> Data into A Register
L	H	H or L	X	H	X		A Register to B <sub>n</sub> (Stored Mode)
L	H	X	X	H	X	Output	Clock A <sub>n</sub> Data into A Register and Output to B <sub>n</sub>
L	L	X	X	X	L		B <sub>n</sub> to A <sub>n</sub> —Real Time (Transparent Mode)
L	L	X	X	X	L		Clock B <sub>n</sub> Data into B Register
L	L	X	H or L	X	H		B Register to A <sub>n</sub> (Stored Mode)
L	L	X	X	X	H		Clock B <sub>n</sub> Data into B Register and Output to A <sub>n</sub>

Note: The data output functions may be enabled or disabled by various signals at the  $\bar{G}_n$  and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the appropriate clock inputs.

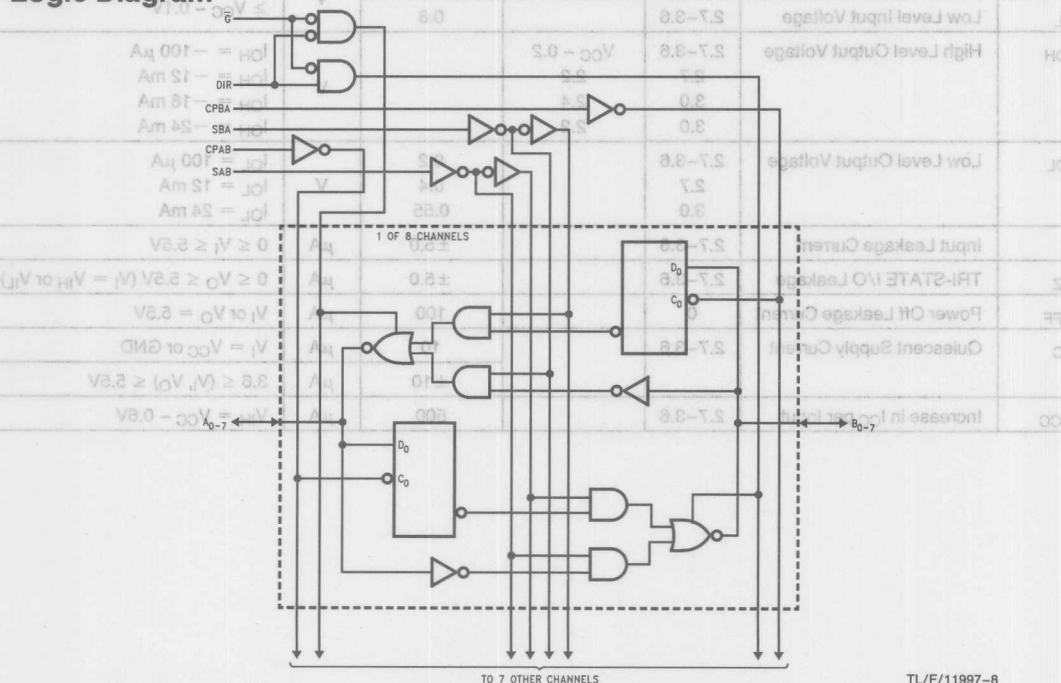
H = HIGH Voltage Level

X = Immaterial

L = LOW Voltage Level

— = LOW-to-HIGH Transition

Logic Diagram



TL/F/11997-8

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Input Voltage ( $V_I$ )	-0.5V to +7.0V
Output Voltage ( $V_O$ )	-0.5V to +7.0V
Outputs TRI-STATE®	-0.5V to +7.0V
Outputs Active (Note 2)	-0.5V to $V_{CC}$ + 0.5V
DC Input Diode Current ( $I_{IK}$ ) $V_I < 0$	-50 mA
DC Output Diode Current ( $I_{OK}$ )	
$V_O < 0$	-50 mA
$V_O > V_{CC}$	+50 mA
DC Output Source/Sink Current ( $I_{OH}/I_{OL}$ )	±50 mA
DC $V_{CC}$ or Ground Current per Supply Pin ( $I_{CC}$ or $I_{GND}$ )	±100 mA
Storage Temperature Range ( $T_{STG}$ )	-65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2:  $I_O$  Absolute Maximum Rating must be observed.

**DC Electrical Characteristics**

Symbol	Parameter	$V_{CC}$ (V)	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		Units	Conditions
			Min	Max		
$V_{IH}$	High Level Input Voltage	2.7-3.6	2.0		V	$V_{OUT} \leq 0.1V$ or $\geq V_{CC} - 0.1V$
$V_{IL}$	Low Level Input Voltage	2.7-3.6		0.8		
$V_{OH}$	High Level Output Voltage	2.7-3.6	$V_{CC} - 0.2$		V	$I_{OH} = -100 \mu A$ $I_{OH} = -12 \text{ mA}$ $I_{OH} = -18 \text{ mA}$ $I_{OH} = -24 \text{ mA}$
		2.7	2.2			
		3.0	2.4			
		3.0	2.2			
$V_{OL}$	Low Level Output Voltage	2.7-3.6		0.2	V	$I_{OL} = 100 \mu A$ $I_{OL} = 12 \text{ mA}$ $I_{OL} = 24 \text{ mA}$
		2.7		0.4		
		3.0		0.55		
$I_I$	Input Leakage Current	2.7-3.6		±5.0	μA	$0 \leq V_I \leq 5.5V$
$I_{OZ}$	TRI-STATE I/O Leakage	2.7-3.6		±5.0	μA	$0 \leq V_O \leq 5.5V$ ( $V_I = V_{IH}$ or $V_{IL}$ )
$I_{OFF}$	Power Off Leakage Current	0		100	μA	$V_I$ or $V_O = 5.5V$
$I_{CC}$	Quiescent Supply Current	2.7-3.6		10	μA	$V_I = V_{CC}$ or GND
				±10	μA	$3.6 \leq (V_I, V_O) \leq 5.5V$
$\Delta I_{CC}$	Increase in $I_{CC}$ per Input	2.7-3.6		500	μA	$V_{IH} = V_{CC} - 0.6V$

**Recommended Operating Conditions**

Supply Voltage	
Operating	2.0V to 3.6V
Data Retention Only	1.5V to 3.6V
Input Voltage ( $V_I$ )	0V to 5.5V
Output Voltage ( $V_O$ )	
Output in Active State	0V to $V_{CC}$
Output in "OFF" State	0V to 5.5V
Output Current $I_{OH}/I_{OL}$	
$V_{CC} = 3.0V$ to $3.6V$	±24 mA
$V_{CC} = 2.7V$ to $3.0V$	±12 mA
Free Air Operating Temperature ( $T_A$ )	-40°C to +85°C
Minimum Input Edge Rate ( $\Delta t/\Delta V$ )	
$V_{IN} = 0.8V$ to $2.0V$ , $V_{CC} = 3.0V$	10 ns/V

**AC Electrical Characteristics:** See Section 2 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF		Units
			Min	Max (Note 2)	
t <sub>PHL</sub> , t <sub>PLH</sub>	Propagation Delay Bus to Bus	2.7 3.0-3.6	1.5 1.5	8.0 7.0	ns
t <sub>PHL</sub> , t <sub>PLH</sub>	Propagation Delay Clock to Bus	2.7 3.0-3.6	1.5 1.5	9.5 8.5	ns
t <sub>PHL</sub> , t <sub>PLH</sub>	Propagation Delay SAB or SBA to A <sub>n</sub> or B <sub>n</sub>	2.7 3.0-3.6	1.5 1.5	9.5 8.5	ns
t <sub>PZH</sub> , t <sub>PZL</sub>	Output Enable Time $\bar{G}$ to A <sub>n</sub> or B <sub>n</sub>	2.7 3.0-3.6	1.5 1.5	9.5 8.5	ns
t <sub>PHZ</sub> , t <sub>PLZ</sub>	Output Disable Time $\bar{G}$ to A <sub>n</sub> or B <sub>n</sub>	2.7 3.0-3.6	1.5 1.5	9.5 8.5	ns
t <sub>PHZ</sub> , t <sub>PLZ</sub>	Output Disable Time DIR to A <sub>n</sub> or B <sub>n</sub>	2.7 3.0-3.6	1.5 1.5	9.5 8.5	ns
t <sub>PHZ</sub> , t <sub>PLZ</sub>	Output Disable Time DIR to A <sub>n</sub> or B <sub>n</sub>	2.7 3.0-3.6	1.5 1.5	9.5 8.5	ns
t <sub>S</sub>	Setup Time	2.7 3.0-3.6	2.5 2.5		ns
t <sub>H</sub>	Hold Time	2.7 3.0-3.6	1.5 1.5		ns
t <sub>W</sub>	Pulse Width	2.7 3.0-3.6	4.0 4.0		ns
t <sub>OSSL</sub> , t <sub>OSLH</sub>	Output to Output Skew (Note 1)	3.0		1.0	ns

**Note 1:** Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t<sub>OSSL</sub>) or LOW to HIGH (t<sub>OSLH</sub>). Parameter guaranteed by design.

**Note 2:** The maximum AC limits are design targets. Actual performance will be specified upon completion of characterization.

**Dynamic Switching Characteristics:** See Section 2 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = 25°C	Units	Conditions
			Typical		
V <sub>OLP</sub>	Quiet Output Dynamic Peak V <sub>OL</sub>	3.3	0.8	V	C <sub>L</sub> = 50 pF, V <sub>IH</sub> = 3.3V, V <sub>IL</sub> = 0V
V <sub>OLV</sub>	Quiet Output Dynamic Valley V <sub>OL</sub>	3.3	0.8	V	C <sub>L</sub> = 50 pF, V <sub>IH</sub> = 3.3V, V <sub>IL</sub> = 0V

**Capacitance**

Symbol	Parameter	Typical	Units	Conditions
C <sub>IN</sub>	Input Capacitance	7	pF	V <sub>CC</sub> = Open V <sub>I</sub> = 0V or V <sub>CC</sub>
C <sub>I/O</sub>	Input/Output Capacitance	8	pF	V <sub>CC</sub> = 3.3V V <sub>I</sub> = 0V or V <sub>CC</sub>
C <sub>PD</sub>	Power Dissipation Capacitance	32	pF	V <sub>CC</sub> = 3.3V V <sub>I</sub> = 0V or V <sub>CC</sub> F = 10 MHz



PRELIMINARY

## 74LCX652

# Low-Voltage Transceiver/Register with 5V Tolerant Inputs and Outputs

## General Description

The LCX652 consists of bus transceiver circuits with D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to the HIGH logic level. Output Enable pins (OEAB, OEBA) are provided to control the transceiver function.

The LCX652 is designed for low voltage (3.3V)  $V_{CC}$  applications with capability of interfacing to a 5V signal environment.

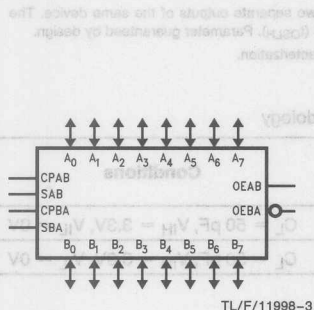
The LCX652 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

## Features

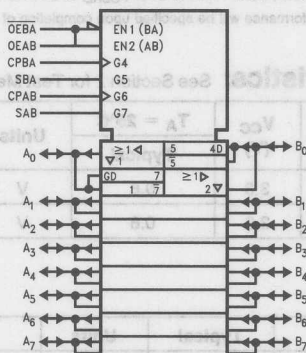
- 5V tolerant inputs and outputs
- Ideal for low power/low noise 2.7V to 3.6V applications
- Power-down static overvoltage protection on inputs and outputs
- Outputs source/sink 24 mA
- Guaranteed simultaneous switching noise level
- Available in SOIC JEDEC and TSSOP
- Implements patented Quiet Series noise/EMI reduction circuitry
- Functionally compatible with the 74 Series 652
- Latchup performance exceeds 300 mA
- ESD performance:
  - Human Body Model >2000V
  - Machine/Model >250V

**Ordering Code:** See Section 11

## Logic Symbols

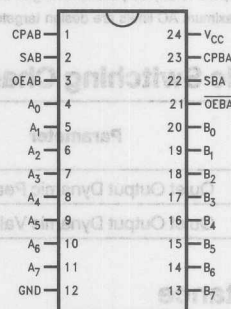


IEEE/IEC



## Connection Diagram

Pin Assignment  
for SOIC and TSSOP



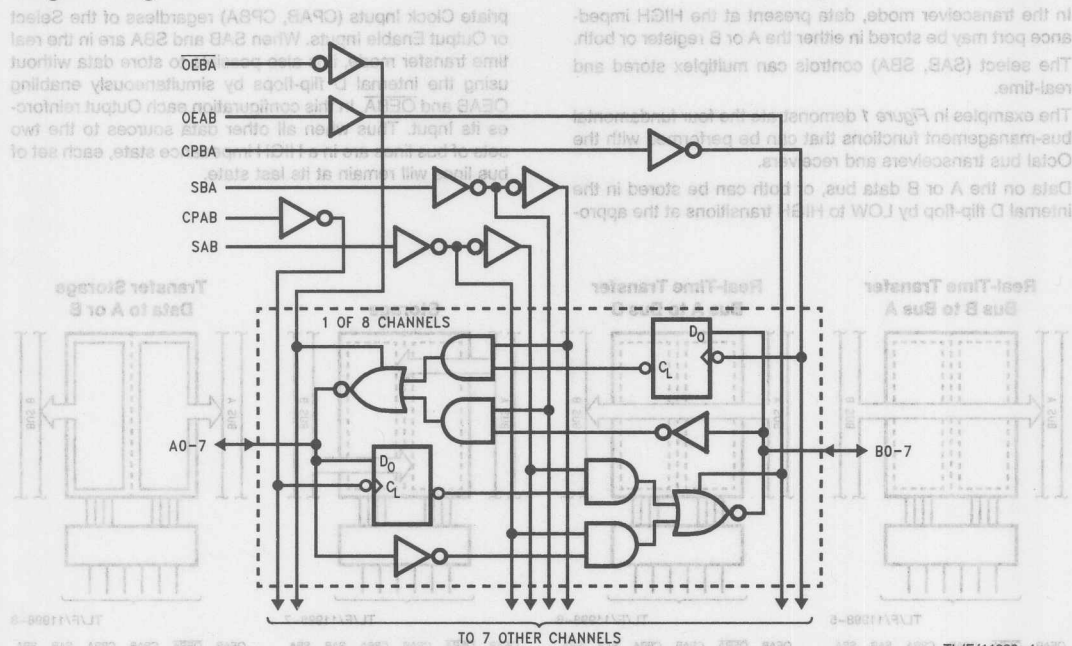
Pin Names	Description
A <sub>0</sub> -A <sub>7</sub> , B <sub>0</sub> -B <sub>7</sub>	A and B Inputs/TRI-STATE® Outputs
CPAB, CPBA	Clock Inputs
SAB, SBA	Select Inputs
OEAB, OEBA	Output Enable Inputs

	SOIC JEDEC	TSSOP JEDEC
Order Number	74LCX652WM 74LCX652WMX	74LCX652MTCX
See NS Package Number	M24B	MTC24

Preliminary Data: National Semiconductor reserves the right to make changes at any time without notice.



# Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Function Table (Note)

Inputs						Inputs/Outputs		Operating Mode
OEAB	OEBA	CPAB	CPBA	SAB	SBA	A <sub>0</sub> thru A <sub>7</sub>	B <sub>0</sub> thru B <sub>7</sub>	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	↗	↗	X	X			Store A and B Data
X	H	↗	H or L	X	X	Input	Not Specified	Store A, Hold B
H	H	↗	↗	X	X	Input	Output	Store A in Both Registers
L	X	H or L	↗	X	X	Not Specified	Input	Hold A, Store B
L	L	↗	↗	X	X	Output	Input	Store B in Both Registers
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus
L	L	X	H or L	X	H			Store B Data to A Bus
H	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus
H	H	H or L	X	H	X			Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored A Data to B Bus and Stored B Data to A Bus

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial  
↗ = LOW to HIGH Clock Transition

**Note:** The data output functions may be enabled or disabled by various signals at OEAB or OEBA inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW to HIGH transition on the clock inputs.

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Input Voltage ( $V_I$ )	-0.5V to +7.0V
Output Voltage ( $V_O$ )	-0.5V to +7.0V
Outputs TRI-STATE	-0.5V to +7.0V
Outputs Active (Note 2)	-0.5V to $V_{CC} + 0.5V$
DC Input Diode Current ( $I_{IK}$ ) ( $V_I < 0$ )	-50 mA
DC Output Diode Current ( $I_{OK}$ )	
$V_O < 0$	-50 mA
$V_O > V_{CC}$	+50 mA
DC Output Source/Sink Current ( $I_{OH}/I_{OL}$ )	$\pm 50$ mA
DC $V_{CC}$ or Ground Current per Supply Pin ( $I_{CC}$ or $I_{GND}$ )	$\pm 100$ mA
Storage Temperature Range ( $T_{STG}$ )	-65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2:  $I_O$  Absolute Maximum Ratings must be observed.

**Recommended Operating Conditions**

Supply Voltage	2.0V to 3.6V
Operating	1.5V to 3.6V
Data Retention Only	0.0V to 5.5V
Input Voltage ( $V_I$ )	0.0V to 5.5V
Output Voltage ( $V_O$ )	0.0V to $V_{CC}$
Output in Active State	0.0V to 5.5V
Output in "OFF" State	
Output Current $I_{OH}/I_{OL}$	
$V_{CC} = 3.0V$ to $3.6V$	
$V_{CC} = 2.7V$ to $3.0V$	
Free Air Operating Temperature ( $T_A$ )	-40°C to +85°C
Minimum Input Edge Rate ( $\Delta t/\Delta V$ )	10 ns/V
$V_{IN} = 0.8V$ to $2.0V$ , $V_{CC} = 3.0V$	

**DC Electrical Characteristics**

Symbol	Parameter	$V_{CC}$ (V)	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		Units	Conditions
			Min	Max		
$V_{IH}$	High Level Input Voltage	2.7-3.6	2.0		V	$V_{OUT} \leq 0.1V$ or $\geq V_{CC} - 0.1V$
$V_{IL}$	Low Level Input Voltage	2.7-3.6		0.8		
$V_{OH}$	High Level Output Voltage	2.7-3.6	$V_{CC} - 0.2$		V	$I_{OH} = -100 \mu A$ $I_{OH} = -12 \text{ mA}$ $I_{OH} = -18 \text{ mA}$ $I_{OH} = -24 \text{ mA}$
$V_{OL}$	Low Level Output Voltage	2.7-3.6		0.2	V	$I_{OL} = 100 \mu A$ $I_{OL} = 12 \text{ mA}$ $I_{OL} = 24 \text{ mA}$
$I_I$	Input Leakage Current	2.7-3.6		$\pm 5.0$	$\mu A$	$0 \leq V_I \leq 5.5V$
$I_{OZ}$	TRI-STATE I/O Leakage	2.7-3.6		$\pm 5.0$	$\mu A$	$0 \leq V_O \leq 5.5B$ $V_I = V_{IH}$ or $V_{IL}$
$I_{OFF}$	Power Off Leakage Current	0		100	$\mu A$	$V_I$ or $V_O = 5.5V$
$I_{CC}$	Quiescent Supply Current	2.7-3.6		10	$\mu A$	$V_I = V_{CC}$ or GND
$\Delta I_{CC}$	Increase in $I_{CC}$ per Input	2.7-3.6		$\pm 10$	$\mu A$	$3.6 \leq (V_I, V_O) \leq 5.5V$
				500	$\mu A$	$V_{IH} = V_{CC} - 0.6V$

**AC Electrical Characteristics:** See Section 2 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> <sup>*</sup> (V)	T <sub>A</sub> = +40°C to +85°C C <sub>L</sub> = 50 pF		Units
			Min	Max (Note 2)	
t <sub>PHL</sub> , t <sub>PLH</sub>	Propagation Delay Clock to Bus	2.7 3.0–3.6	1.5 1.5	9.5 8.5	ns
t <sub>PHL</sub> , t <sub>PLH</sub>	Propagation Delay Bus to Bus	2.7 3.0–3.6	1.5 1.5	8.0 7.0	ns
t <sub>PHL</sub> , t <sub>PLH</sub>	Propagation Delay SAB or SBA to A or B	2.7 3.0–3.6	1.5 1.5	9.5 8.5	ns
t <sub>PZH</sub> , t <sub>PZL</sub>	Output Enable Time OEBA to A	2.7 3.0–3.6	1.5 1.5	9.5 8.5	ns
t <sub>PHZ</sub> , t <sub>PLZ</sub>	Output Disable Time OEBA to A	2.7 3.0–3.6	1.5 1.5	9.5 8.5	ns
t <sub>PZH</sub> , t <sub>PZL</sub>	Output Enable Time OEBA to A	2.7 3.0–3.6	1.5 1.5	9.5 8.5	ns
t <sub>PHZ</sub> , t <sub>PLZ</sub>	Output Disable Time OEAB to B	2.7 3.0–3.6	1.5 1.5	9.5 8.5	ns
t <sub>S</sub>	Setup Time Bus to Clock	2.7 3.0–3.6	2.5 2.5		ns
t <sub>H</sub>	Hold Time Bus to Clock	2.7 3.0–3.6	1.5 1.5		ns
t <sub>W</sub>	Clock Pulse Width	2.7 3.0–3.6	4.0 4.0		ns
t <sub>OSHL</sub> , t <sub>OSLH</sub>	Output to Output Skew (Note 1)	3.0		1.0	ns

**Note 1:** Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t<sub>OSHL</sub>) or LOW to HIGH (t<sub>OSLH</sub>). Parameter guaranteed by design.

**Note 2:** The maximum AC limits are design targets. Actual performance will be specified upon completion of characterization.

**Dynamic Switching Characteristics** See Section 0 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = 25°C	Units	Conditions
			Typical		
V <sub>OLP</sub>	Quiet Output Dynamic Peak V <sub>OL</sub>	3.3	0.8	V	C <sub>L</sub> = 50 pF, V <sub>IH</sub> = 3.3V, V <sub>IL</sub> = 0V
V <sub>OLV</sub>	Quiet Output Dynamic Valley V <sub>OL</sub>	3.3	0.8	V	C <sub>L</sub> = 50 pF, V <sub>IH</sub> = 3.3V, V <sub>IL</sub> = 0V

**Capacitance**

Symbol	Parameter	Typical	Units	Conditions
C <sub>IN</sub>	Input Capacitance	7	pF	V <sub>CC</sub> = Open V <sub>I</sub> = 0V or V <sub>CC</sub>
C <sub>I/O</sub>	Input/Output Capacitance	8	pF	V <sub>CC</sub> = 3.3V V <sub>I</sub> = 0V or V <sub>CC</sub>
C <sub>PD</sub>	Power Dissipation Capacitance	32	pF	V <sub>CC</sub> = 3.3V V <sub>I</sub> = 0V or V <sub>CC</sub> F = 10 MHz



## 74LCX16240

# Low-Voltage 16-Bit Inverting Buffer/Line Driver with 5V Tolerant Inputs/Outputs

## General Description

The LCX16240 contains sixteen inverting buffers with TRI-STATE® outputs designed to be employed as a memory and address driver, clock driver, or bus-oriented transmitter/receiver. The device is nibble controlled. Each nibble has separate TRI-STATE control inputs which can be shorted together for full 16-bit operation.

The LCX16240 is designed for low voltage (3.3V)  $V_{CC}$  applications with capacity of interfacing to a 5V signal environment.

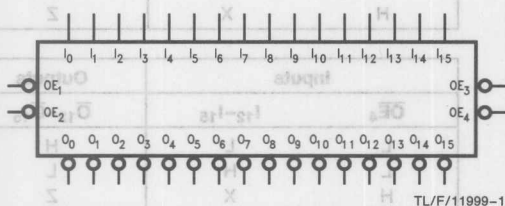
The LCX16240 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

## Features

- 5V tolerant inputs and outputs
- Ideal for low power/low noise 2.7V to 3.6V applications
- Power-down static overvoltage protection on inputs and outputs
- Outputs source/sink 24 mA
- Guaranteed simultaneous switching noise level
- Available in SSOP and TSSOP
- Implements patented Quiet Series noise/EMI reduction circuitry
- Functionally compatible with the 74 series 16240
- Latchup performance exceeds 300 mA
- ESD performance:
  - Human body model > 2500V
  - Machine model > 250V

**Ordering Code:** See Section 11

## Logic Symbol



Pin Names	Description
$\overline{OE}_n$	Output Enable Inputs (Active Low)
$I_0-I_{15}$	Inputs
$O_0-O_{15}$	Outputs

	SSOP EIAJ	TSSOP JEDEC
Order Number	74LCX16240MEA 74LCX16240MEAX	74LCX16240MTD 74LCX16240MTDX
See NS Package Number	MS48A	MTD48

## Connection Diagram

### Pin Assignment for SSOP and TSSOP



TL/F/11999-2

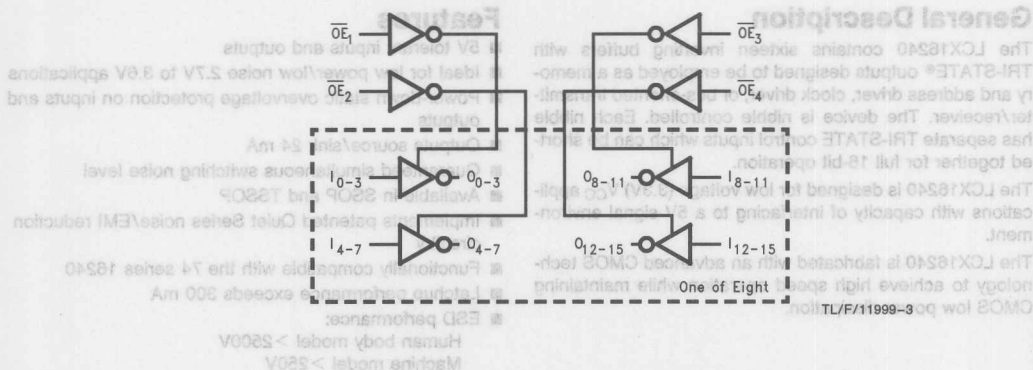
Preliminary Data: National Semiconductor reserves the right to make changes at any time without notice.

# Functional Description

The LCX16240 contains sixteen inverting buffers with TRI-STATE standard outputs. The device is nibble (4 bits) controlled with each nibble functioning identically, but independent of the other. The control pins may be shorted together to obtain full 16-bit operation. The TRI-STATE out-

puts are controlled by an Output Enable ( $\overline{OE}_n$ ) input for each nibble. When  $\overline{OE}_n$  is LOW, the outputs are in 2-state mode. When  $\overline{OE}_n$  is HIGH, the outputs are in the high impedance mode, but this does not interfere with entering new data into the inputs.

## Logic Diagram



## Truth Tables

Inputs		Outputs
$\overline{OE}_1$	$I_0-I_3$	$\overline{O}_0-\overline{O}_3$
L	L	H
L	H	L
H	X	Z

Inputs		Outputs
$\overline{OE}_2$	$I_4-I_7$	$\overline{O}_4-\overline{O}_7$
L	L	H
L	H	L
H	X	Z

Inputs		Outputs
$\overline{OE}_3$	$I_8-I_{11}$	$\overline{O}_8-\overline{O}_{11}$
L	L	H
L	H	L
H	X	Z

Inputs		Outputs
$\overline{OE}_4$	$I_{12}-I_{15}$	$\overline{O}_{12}-\overline{O}_{15}$
L	L	H
L	H	L
H	X	Z

H = High Voltage Level  
L = Low Voltage Level  
X = Immaterial  
Z = High Impedance

Pin	Description
$\overline{OE}_n$	Output Enable Input (Active Low)
$I_0-I_{15}$	Inputs
$\overline{O}_0-\overline{O}_{15}$	Outputs

Order Number	See NS Package	MS48A	MS48B
74LCX16240MEAX	74LCX16240MTDX	74LCX16240MEATD	74LCX16240MTDET
MS48A	MS48B	MS48A	MS48B

Preliminary Data: National Semiconductor reserves the right to make changes at any time without notice.

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Input Voltage ( $V_I$ )	-0.5V to +7.0V
Output Voltage ( $V_O$ )	-0.5V to +7.0V
Output TRI-STATE	-0.5V to $V_{CC} + 0.5V$
Outputs Active (Note 2)	-0.5V to $V_{CC} + 0.5V$
DC Input Diode Current ( $I_{IK}$ ) $V_I < 0$	-50 mA
DC Output Diode Current ( $I_{OK}$ )	
$V_O < 0$	-50 mA
$V_O > V_{CC}$	+50 mA
DC Output Source/Sink Curr. ( $I_{OH}/I_{OL}$ )	±50 mA
DC $V_{CC}$ or Ground Current per Supply Pin ( $I_{CC}$ or $I_{GND}$ )	±100 mA
Storage Temperature Range (TSTG)	-65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2:  $I_O$  Absolute Maximum Rating must be observed.

**Recommended Operating Conditions**

Supply Voltage	2.0V to 3.6V
Operating	1.5V to 3.6V
Data Retention only	0.0V to 5.5V
Input Voltage ( $V_I$ )	0.0V to 5.5V
Output Voltage ( $V_O$ )	0.0V to $V_{CC}$
Output in Active State	0.0V to 5.5V
Output in "OFF" State	±24 mA
Output Current $I_{OH}/I_{OL}$	±12 mA
$V_{CC} = 3.0V$ to 3.6V	
$V_{CC} = 2.7V$ to 3.0V	
Free Air Operating Temperature ( $T_A$ )	-40°C to +85°C
Minimum Input Edge Rate ( $\Delta t/\Delta V$ )	10 ns/V
$V_{IN} = 0.8V$ to 2.0V, $V_{CC} = 3.0V$	

**DC Electrical Characteristics**

Symbol	Parameter	$V_{CC}$ (V)	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		Units	Conditions
			Min	Max		
$V_{IH}$	High Level Input Voltage	2.7-3.6	2.0		V	$V_{OUT} \leq 0.1V$ or $\geq V_{CC} - 0.1V$
$V_{IL}$	Low Level Input Voltage	2.7-3.6		0.8	V	
$V_{OH}$	High Level Output Voltage	2.7-3.6	$V_{CC} - 0.2$		V	$I_{OH} = -100 \mu A$
		2.7	2.2		V	$I_{OH} = -12 \text{ mA}$
		3.0			V	$I_{OH} = -18 \text{ mA}$
		3.0	2.2		V	$I_{OH} = -24 \text{ mA}$
$V_{OL}$	Low Level Output Voltage	2.7-3.6		0.2	V	$I_{OL} = 100 \mu A$
		2.7		0.4	V	$I_{OL} = 12 \text{ mA}$
		3.0		0.55	V	$I_{OL} = 24 \text{ mA}$
$I_I$	Input Leakage Current	2.7-3.6		±5.0	$\mu A$	$0 \leq V_I \leq 5.5V$
$I_{OZ}$	TRI-STATE Output Leakage	2.7-3.6		±5.0	$\mu A$	$0 \leq V_O \leq 5.5V$ $V_I = V_{IH}$ or $V_{IL}$
$I_{CC}$	Quiescent Supply Current	2.7-3.6		20	$\mu A$	$V_I = V_{CC}$ or GND
				±20	$\mu A$	$3.6 \leq (V_I, V_O) \leq 5.5V$
$\Delta I_{CC}$	Increase in $I_{CC}$ per Input	2.7-3.6		500	$\mu A$	$V_{IH} = V_{CC} - 0.6V$
$I_{OFF}$	Power Off Leakage Current	0		100	$\mu A$	$V_I$ or $V_O = 5.5V$

**AC Electrical Characteristics:** See Section 2 for test methodology

Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF		Units
			Min	Max (Note 2)	
t <sub>PHL</sub> , t <sub>PLH</sub>	Propagation Delay Data to Output	2.7 3.0–3.6	1.5 1.5	5.6 4.9	ns
t <sub>PZL</sub> , t <sub>PZH</sub>	Output Enable Time	2.7 3.0–3.6	1.5 1.5	7.7 7.0	ns
t <sub>PHZ</sub> , t <sub>PLZ</sub>	Output Disable Time	2.7 3.0–3.6	1.5 1.5	7.7 7.0	ns
t <sub>OSHL</sub> , t <sub>OSLH</sub>	Output to Output Skew (Note 1)	3.0		1.0	ns

**Note 1:** Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t<sub>OSHL</sub>) or LOW to HIGH (t<sub>OSLH</sub>). Parameter guaranteed by design.

**Note 2:** The maximum AC limits are design targets. Actual performance will be specified upon completion of characterization.

**Dynamic Switching Characteristics:** See Section 2 for test methodology

Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = 25°C		Units	Conditions
			Typical			
V <sub>OLP</sub>	Quiet Output Dynamic Peak V <sub>OL</sub>	3.3	0.8		V	C <sub>L</sub> = 50 pF, V <sub>IH</sub> = 3.3V, V <sub>IL</sub> = 0V
V <sub>OLV</sub>	Quiet Output Dynamic Valley V <sub>OL</sub>	3.3	0.8		V	C <sub>L</sub> = 50 pF, V <sub>IH</sub> = 3.3V, V <sub>IL</sub> = 0V

**Capacitance**

Symbol	Parameter	Typical	Units	Conditions
C <sub>IN</sub>	Input Capacitance	7	pF	V <sub>CC</sub> = Open V <sub>I</sub> = 0V or V <sub>CC</sub>
C <sub>OUT</sub>	Output Capacitance	8	pF	V <sub>CC</sub> = 3.3V V <sub>I</sub> = 0V or V <sub>CC</sub>
C <sub>PD</sub>	Power Dissipation Capacitance	32	pF	V <sub>CC</sub> = 3.3V V <sub>I</sub> = 0V or V <sub>CC</sub> F = 10 MHz



## 74LCX16244

### Low-Voltage 16-Bit Buffer/Line Driver with 5V Tolerant Inputs and Outputs

#### General Description

The 74LCX16244 contains sixteen non-inverting buffers with TRI-STATE® outputs designed to be employed as a memory and address driver, clock driver, or bus oriented transmitter/receiver. The device is nibble controlled. Each nibble has separate TRI-STATE control inputs which can be shorted together for full 16-bit operation.

The LCX16244 is designed for low voltage (3.3V)  $V_{CC}$  applications with capability of interfacing to a 5V signal environment.

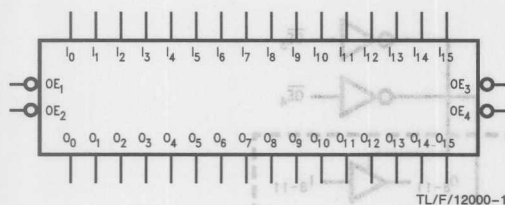
The LCX16244 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

#### Features

- 5V tolerant inputs and outputs
- Ideal for low power/low noise 2.7V to 3.6V applications
- Power-down static overvoltage protection on inputs and outputs
- Outputs source/sink 24 mA
- Guaranteed simultaneous switching noise level
- Available in SSOP and TSSOP
- Implements patented Quiet Series noise/EMI reduction circuitry
- Functionally compatible with the 74 series 16244
- Latch performance exceeds 300 mA
- ESD performance:  
Human Body Model > 2000V  
Machine Model > 250V

**Ordering Code:** See Section 11

#### Logic Symbol

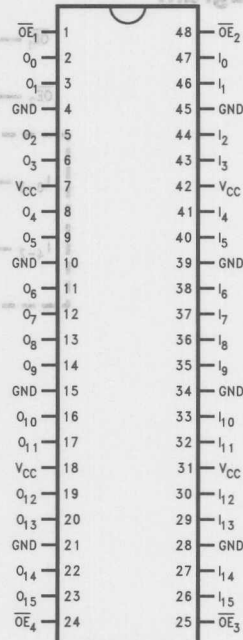


Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active Low)
$I_0-I_{15}$	Inputs
$O_0-O_{15}$	Outputs

	SSOP EIAJ	TSSOP JEDEC
Order Number	74LCX16244MEA 74LCX16244MEAX	74LCX16244MTD 74LCX16244MTDX
See NS Package Number	MS48A	MTD48

#### Connection Diagram

Pin Assignment for  
SSOP and TSSOP



TL/F/12000-2

Preliminary Data: National Semiconductor reserves the right to make changes at any time without notice.

# Functional Description

The LCX16244 contains sixteen non-inverting buffers with TRI-STATE standard outputs. The device is nibble (4 bits) controlled with each nibble functioning identically, but independent of the other. The control pins can be shorted together to obtain full 16-bit operation. The TRI-STATE out-

puts are controlled by an Output Enable ( $\overline{OE}_n$ ) input for each nibble. When  $\overline{OE}_n$  is LOW, the outputs are in 2-state mode. When  $\overline{OE}_n$  is HIGH, the outputs are in the high impedance mode, but this does not interfere with entering new data into the inputs.

## Truth Tables

Inputs		Outputs
$\overline{OE}_1$	$I_0-I_3$	$O_0-O_3$
L	L	L
L	H	H
H	X	Z

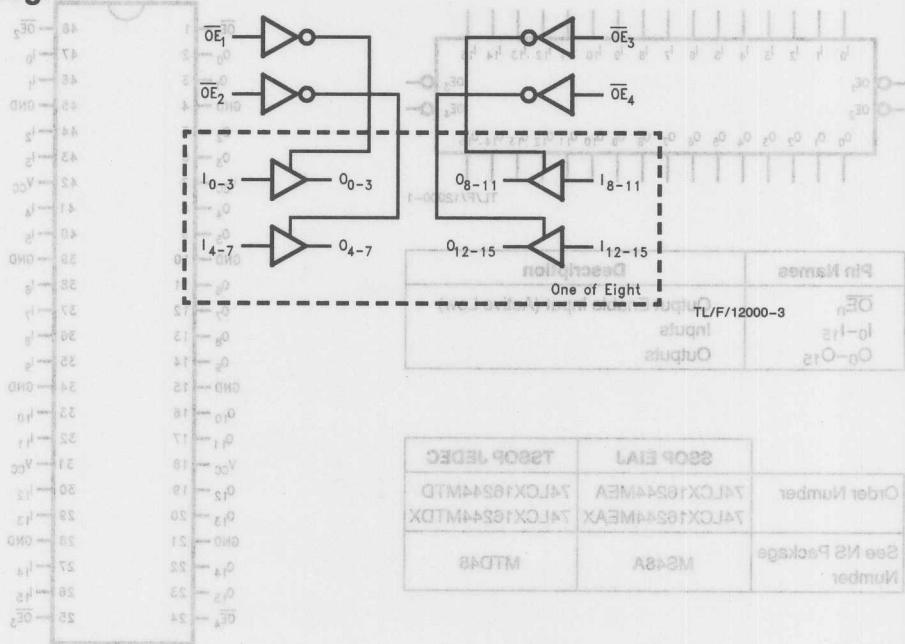
Inputs		Outputs
$\overline{OE}_3$	$I_8-I_{11}$	$O_8-O_{11}$
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
$\overline{OE}_2$	$I_4-I_7$	$O_4-O_7$
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
$\overline{OE}_4$	$I_{12}-I_{15}$	$O_{12}-O_{15}$
L	L	L
L	H	H
H	X	Z

H = High Voltage Level  
L = Low Voltage Level  
X = Immaterial  
Z = High Impedance

## Logic Diagram



TLF/12000-3

Preliminary Data: National Semiconductor reserves the right to make changes at any time without notice.

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Input Voltage ( $V_I$ )	-0.5V to +7.0V
Output Voltage ( $V_O$ )	
Outputs TRI-STATE	-0.5V to +7.0V
Outputs Active (Note 2)	-0.5V to $V_{CC} + 0.5V$
DC Input Diode Current ( $I_{IK}$ ) $V_I < 0$	-50 mA
DC Output Diode Current ( $I_{OK}$ )	
$V_O < 0$	-50 mA
$V_O > V_{CC}$	+50 mA
DC Output Source/Sink Current ( $I_{OH}/I_{OL}$ )	$\pm 50$ mA
DC $V_{CC}$ or Ground Current per Supply Pin ( $I_{CC}$ or $I_{GND}$ )	$\pm 100$ mA
Storage Temperature Range (TSTG)	-65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2:  $I_O$  Absolute Maximum Rating must be observed.

**Recommended Operating Conditions**

Supply Voltage	
Operating	2.7V to 3.6V
Data Retention Only	1.5V to 3.6V
Input Voltage ( $V_I$ )	0V to 5.5V
Output Voltage ( $V_O$ )	
Output in Active State	0V to $V_{CC}$
Output in "OFF" State	0V to 5.5V
Output Current $I_{OH}/I_{OL}$	
$V_{CC} = 3.0V$ to $3.6V$	$\pm 24$ mA
$V_{CC} = 2.7V$ to $3.0V$	$\pm 12$ mA
Free Air Operating Temperature ( $T_A$ )	-40°C to +85°C
Minimum Input Edge Rate ( $\Delta t/\Delta V$ )	
$V_{IN} = 0.8V$ to $2.0V$ , $V_{CC} = 3.0V$	10 ns/V

**DC Electrical Characteristics**

Symbol	Parameter	$V_{CC}$ (V)	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		Units	Conditions
			Min	Max		
$V_{IH}$	High Level Input Voltage	2.7-3.6	2.0		V	$V_{OUT} \leq 0.1V$ or $\geq V_{CC} - 0.1V$
$V_{IL}$	Low Level Input Voltage	2.7-3.6		0.8		
$V_{OH}$	High Level Output Voltage	2.7-3.6	$V_{CC} - 0.2$			$I_{OH} = -100 \mu A$
		2.7	2.2		V	$I_{OH} = -12 \text{ mA}$
		3.0	2.4			$I_{OH} = -18 \text{ mA}$
		3.0	2.2			$I_{OH} = -24 \text{ mA}$
$V_{OL}$	Low Level Output Voltage	2.7-3.6		0.2		$I_{OL} = 100 \mu A$
		2.7		0.4	V	$I_{OL} = 12 \text{ mA}$
		3.0		0.55		$I_{OL} = 24 \text{ mA}$
$I_I$	Input Leakage Current	2.7-3.6		$\pm 5.0$	$\mu A$	$0 \leq V_I \leq 5.5V$
$I_{OZ}$	TRI-STATE Output Leakage	2.7-3.6		$\pm 5.0$	$\mu A$	$0 \leq V_O \leq 5.5V$ $V_I = V_{IH}$ or $V_{IL}$
$I_{OFF}$	Power Off Leakage Current	0		100	$\mu A$	$V_I$ or $V_O = 5.5V$
$I_{CC}$	Quiescent Supply Current	2.7-3.6		20	$\mu A$	$V_I = V_{CC}$ or GND
				$\pm 20$	$\mu A$	$3.6 \leq (V_I, V_O) \leq 5.5V$
$\Delta I_{CC}$	Increase in $I_{CC}$ per Input	2.7-3.6		500	$\mu A$	$V_{IH} = V_{CC} - 0.6V$

**AC Electrical Characteristics:** See Section 2 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF		Units
			Min	Max (Note 2)	
t <sub>PHL</sub> t <sub>PHL</sub>	Propagation Delay	2.7 3.0–3.6	1.5 1.5	5.8 5.2	ns
t <sub>PZL</sub> t <sub>PZH</sub>	Output Enable Time	2.7 3.0–3.6	1.5 1.5	7.7 7.0	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time	2.7 3.0–3.6	1.5 1.5	7.7 7.0	ns
t <sub>OSSL</sub> t <sub>OSLH</sub>	Output to Output Skew (Note 1)	3.0		1.0	ns

**Note 1:** Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t<sub>OSSL</sub>) or LOW to HIGH (t<sub>OSLH</sub>). Parameter guaranteed by design.

**Note 2:** The maximum AC limits are design targets. Actual performance will be specified upon completion of characterization.

**Dynamic Switching Characteristics:** See Section 2 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = 25°C		Units	Conditions
			Typical			
V <sub>OLP</sub>	Quiet Output Dynamic Peak V <sub>OL</sub>	3.3	0.8		V	C <sub>L</sub> = 50 pF, V <sub>IH</sub> = 3.3V, V <sub>IL</sub> = 0V
V <sub>OLV</sub>	Quiet Output Dynamic Valley V <sub>OL</sub>	3.3	0.8		V	C <sub>L</sub> = 50 pF, V <sub>IH</sub> = 3.3V, V <sub>IL</sub> = 0V

**Capacitance**

Symbol	Parameter	Typical	Units	Conditions	Symbol
C <sub>IN</sub>	Input Capacitance	7	pF	V <sub>CC</sub> = Open V <sub>I</sub> = 0V or V <sub>CC</sub>	V <sub>IH</sub>
C <sub>OUT</sub>	Output Capacitance	8	pF	V <sub>CC</sub> = 3.3V V <sub>I</sub> = 0V or V <sub>CC</sub>	V <sub>OL</sub>
C <sub>PD</sub>	Power Dissipation Capacitance	32	pF	V <sub>CC</sub> = 3.3V V <sub>I</sub> = 0V or V <sub>CC</sub> F = 10 MHz	V <sub>OL</sub>
I <sub>IL</sub>	Input Leakage Current	±0.5	μA	0 ≤ V <sub>I</sub> ≤ 5.5V	I <sub>IL</sub>
I <sub>OL</sub>	Output Leakage Current	±0.5	μA	0 ≤ V <sub>O</sub> ≤ 5.5V V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub>
I <sub>OFF</sub>	Power Off Leakage Current	100	μA	V <sub>I</sub> or V <sub>O</sub> = 5.5V	I <sub>OFF</sub>
I <sub>CC</sub>	Quiescent Supply Current	50	μA	V <sub>I</sub> = V <sub>CC</sub> or GND	I <sub>CC</sub>
ΔI <sub>CC</sub>	Increase in I <sub>CC</sub> per Input	±50	μA	0 ≤ V <sub>I</sub> ≤ 5.5V V <sub>OH</sub> = V <sub>CC</sub> - 0.8V	ΔI <sub>CC</sub>



PRELIMINARY

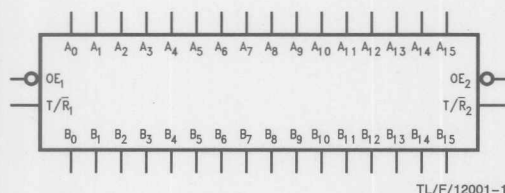
**74LCX16245****Low-Voltage 16-Bit Bidirectional Transceiver  
with 5V Tolerant Inputs and Outputs****General Description**

The 74LCX16245 contains sixteen non-inverting bidirectional buffers with TRI-STATE® outputs and is intended for bus oriented applications. The device is designed for low voltage (3.3V)  $V_{CC}$  applications with capability of interfacing to a 5V signal environment. The device is byte controlled. Each byte has separate control inputs which could be shorted together for full 16-bit operation. The T/R inputs determine the direction of data flow through the device. The OE inputs disable both the A and B ports by placing them in a high impedance state.

The LCX16245 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

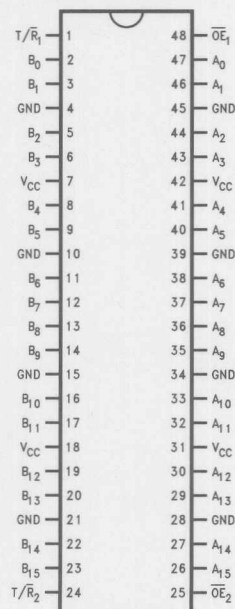
**Features**

- 5V tolerant inputs and outputs
- Ideal for low power/low noise 2.7V to 3.6V applications
- Power-down static overvoltage protection on inputs and outputs
- Outputs source/sink 24 mA
- Separate control logic for each 8-bit
- Guaranteed simultaneous switching noise level
- Available in SSOP, TSSOP
- Implements patented Quiet Series noise/EMI reduction circuitry
- Functionally compatible with 74 series 16245
- Latchup performance exceeds 300 mA
- ESD performance:
  - Human body model >2000V
  - Machine model >250V

**Ordering Code:** See Section 11**Logic Symbol**

Pin Names	Description
OE	Output Enable Input
T/R	Transmit/Receive Input
A <sub>0</sub> -A <sub>15</sub>	Side A Inputs or TRI-STATE Outputs
B <sub>0</sub> -B <sub>15</sub>	Side B Inputs or TRI-STATE Outputs

	SSOP EIAJ	TSSOP JEDEC
Order Number	74LCX16245MEA 74LCX16245MEAX	74LCX16245MTD 74LCX16245MTDX
See NS Package Number	MS48A	MTD48

**Connection Diagram****Pin Assignment for  
SSOP and TSSOP**

TL/F/12001-2

**Preliminary Data:** National Semiconductor reserves the right to make changes at any time without notice.

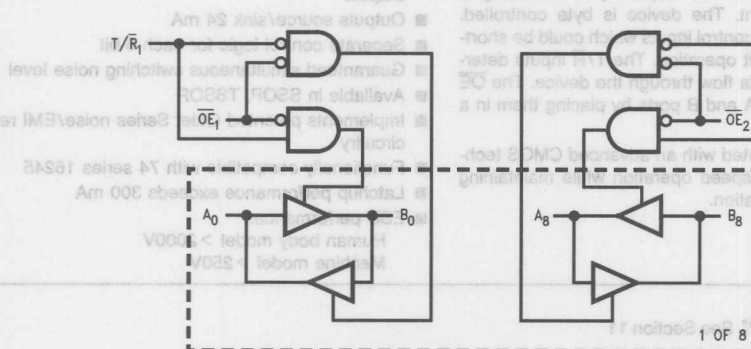
# Truth Tables

Inputs		Outputs
$\overline{OE}_1$	$T/\overline{R}_1$	
L	L	Bus B <sub>0</sub> –B <sub>7</sub> Data to Bus A <sub>0</sub> –A <sub>7</sub>
L	H	Bus A <sub>0</sub> –A <sub>7</sub> Data to Bus B <sub>0</sub> –B <sub>7</sub>
H	X	HIGH Z State on A <sub>0</sub> –A <sub>7</sub> , B <sub>0</sub> –B <sub>7</sub>

H = High Voltage Level  
L = Low Voltage Level  
X = Immaterial  
Z = High Impedance

Inputs		Outputs
$\overline{OE}_2$	$T/\overline{R}_2$	
L	L	Bus B <sub>8</sub> –B <sub>15</sub> Data to Bus A <sub>8</sub> –A <sub>15</sub>
L	H	Bus A <sub>8</sub> –A <sub>15</sub> Data to Bus B <sub>8</sub> –B <sub>15</sub>
H	X	HIGH Z State on A <sub>8</sub> –A <sub>15</sub> , B <sub>8</sub> –B <sub>15</sub>

## Logic Diagram



## Connection Diagram

Pin Assignment for  
TSOP and TSOP



Pin	Function
1	Output Enable Input
2	Transmit/Receive Input
3	Side A Inputs or TRI-STATE Outputs
4	Side B Inputs or TRI-STATE Outputs

Order Number	MS48A	MS48B
TSOP EIAJ	LCX16245MEA	LCX16245MTD
TSOP JEDEC	LCX16245MEAX	LCX16245MTDX

TLF/12001-5

Preliminary Data: National Semiconductor reserves the right to make changes at any time without notice.

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Input Voltage ( $V_I$ )	-0.5V to +7.0V
Output Voltage ( $V_O$ )	-0.5V to +7.0V
Outputs TRI-STATE	-0.5V to $V_{CC} + 0.5V$
Outputs Active (Note 2)	-0.5V to $V_{CC} + 0.5V$
DC Input Diode Current ( $I_{IK}$ ) ( $V_I < 0$ )	-50 mA
DC Output Diode Current ( $I_{OK}$ )	
$V_O < 0$	-50 mA
$V_O > V_{CC}$	+50 mA
DC Output Source/Sink Current ( $I_{OH}/I_{OL}$ )	$\pm 50$ mA
DC $V_{CC}$ or Ground Current per Supply Pin ( $I_{CC}$ or $I_{GND}$ )	$\pm 100$ mA
Storage Temperature Range ( $T_{STG}$ )	-65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2:  $I_O$  Absolute Maximum Rating must be observed.

**Recommended Operating Conditions**

Supply Voltage	2.0V to 3.6V
Operating	1.5V to 3.6V
Data Retention only	0.0V to 5.5V
Input Voltage ( $V_I$ )	0.0V to 5.5V
Output Voltage ( $V_O$ )	0.0V to $V_{CC}$
Output in Active State	0.0V to 5.5V
Output in "OFF" State	
Output Current $I_{OH}/I_{OL}$	
$V_{CC} = 3.0V$ to 3.6V	
$V_{CC} = 2.7V$ to 3.0V	
Free Air Operating Temperature ( $T_A$ )	-40°C to +85°C
Minimum Input Edge Rate $\Delta t/\Delta V$	10 ns/V
$V_{IN} = 0.8V$ to 2.0V, $V_{CC} = 3.0V$	

**DC Electrical Characteristics**

Symbol	Parameter	$V_{CC}$ (V)	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		Units	Conditions
			Min	Max		
$V_{IH}$	High Level Input Voltage	2.7-3.6	2.0		V	$V_{OUT} \leq 0.1V$ or $\geq V_{CC} - 0.1V$
$V_{IL}$	Low Level Input Voltage	2.7-3.6		0.8		
$V_{OH}$	High Level Output Voltage	2.7-3.6	$V_{CC} - 0.2$		V	$I_{OH} = -100 \mu A$ $I_{OH} = -12 \text{ mA}$ $I_{OH} = -18 \text{ mA}$ $I_{OH} = -24 \text{ mA}$
		2.7	2.2			
		3.0	2.4			
		3.0	2.2			
$V_{OL}$	Low Level Output Voltage	2.7-3.6		0.2	V	$I_{OL} = 100 \mu A$ $I_{OL} = 12 \text{ mA}$ $I_{OL} = 24 \text{ mA}$
		2.7		0.4		
		3.0		0.55		
$I_I$	Input Leakage Current @ $\overline{OE}$ , $T/\overline{R}$	2.7-3.6		$\pm 5.0$	$\mu A$	$0 \leq V_I \leq 5.5V$
$I_{OZ}$	TRI-STATE I/O Leakage	2.7-3.6		$\pm 5.0$	$\mu A$	$0 \leq V_O \leq 5.5V$ $V_I = V_{IH}$ or $V_{IL}$
$I_{OFF}$	Power Off Leakage Current	0		100	$\mu A$	$V_I$ or $V_O = 5.5V$
$I_{CC}$	Quiescent Supply Current	2.7-3.6		20	$\mu A$	$V_I = V_{CC}$ or GND
				$\pm 20$	$\mu A$	$3.6 \leq (V_I, V_O) \leq 5.5V$
$\Delta I_{CC}$	Increase in $I_{CC}$ per Input	2.7-3.6		500	$\mu A$	$V_{IH} = V_{CC} - 0.6V$

**AC Electrical Characteristics:** See Section 2 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = +40°C to +85°C C <sub>L</sub> = 50 pF		Units
			Min	Max (Note 2)	
t <sub>PHL</sub>	Propagation Delay	2.7	1.5	5.8	ns
t <sub>PLH</sub>	Clock to Bus	3.0–3.6	1.5	5.2	ns
t <sub>PZL</sub>	Output Enable Time	2.7	1.5	8.0	ns
t <sub>PZH</sub>	OEBA to A	3.0–3.6	1.5	7.2	ns
t <sub>PHZ</sub>	Output Disable Time	2.7	1.5	8.0	ns
t <sub>PLZ</sub>	OEBA to A	3.0–3.6	1.5	7.2	ns
t <sub>OSHL</sub> t <sub>OSLH</sub>	Output to Output Skew (Note 1)	3.0		1.0	ns

**Note 1.** Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t<sub>OSHL</sub>) or LOW to HIGH (t<sub>OSLH</sub>). Parameter guaranteed by design.

**Note 2.** The maximum AC limits are design targets. Actual performance will be specified upon completion of characterization.

**Dynamic Switching Characteristics:** See Section 2 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = 25°C	Units	Conditions
			Typical		
V <sub>OLP</sub>	Quiet Output Dynamic Peak V <sub>OL</sub>	3.3	0.8	V	C <sub>L</sub> = 50 pF, V <sub>IH</sub> = 3.3V, V <sub>IL</sub> = 0V
V <sub>OLV</sub>	Quiet Output Dynamic Valley V <sub>OL</sub>	3.3	0.8	V	C <sub>L</sub> = 50 pF, V <sub>IH</sub> = 3.3V, V <sub>IL</sub> = 0V

**Capacitance**

Symbol	Parameter	Typical	Units	Conditions
C <sub>IN</sub>	Input Capacitance	7	pF	V <sub>CC</sub> = Open V <sub>I</sub> = 0V or V <sub>CC</sub>
C <sub>I/O</sub>	Input/Output Capacitance	8	pF	V <sub>CC</sub> = 3.3V V <sub>I</sub> = 0V or V <sub>CC</sub>
C <sub>PD</sub>	Power Dissipation Capacitance	32	pF	V <sub>CC</sub> = 3.3V V <sub>I</sub> = 0V or V <sub>CC</sub> F = 10 MHz



## 74LCX16373

# Low-Voltage 16-Bit Transparent Latch with 5V Tolerant Inputs and Outputs

### General Description

The LCX16373 contains sixteen non-inverting latches with TRI-STATE® outputs and is intended for bus oriented applications. The device is byte controlled. The flip-flops appear transparent to the data when the Latch Enable (LE) is HIGH. When LE is low, the data that meets the setup time is latched. Data appears on the bus when the Output Enable (OE) is LOW. When OE is HIGH, the outputs are in high Z state.

The LCX16373 is designed for low voltage (3.3V)  $V_{CC}$  applications with capability of interfacing to a 5V signal environment.

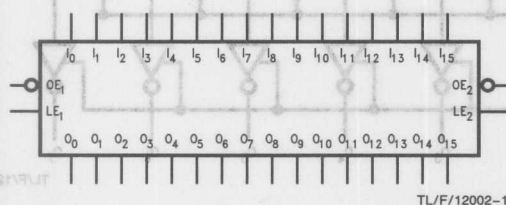
The LCX16373 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

### Features

- 5V tolerant inputs and outputs
- Ideal for low power/low noise 2.7V to 3.6V applications
- Power-down static overvoltage protection on inputs and outputs
- Outputs source/sink 24 mA
- Available in SSOP and TSSOP
- Implements patented Quiet Series noise/EMI reduction circuitry
- Functionally compatible with the 74 series 16373
- Latchup performance exceeds 300 mA
- ESD performance:
  - Human Body Model > 2000V
  - Machine Model > 250V

**Ordering Code:** See Section 11

### Logic Symbol

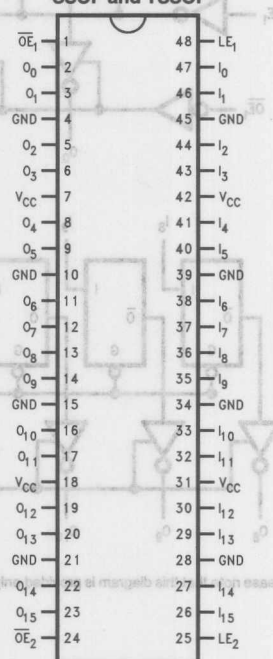


Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active Low)
$LE_n$	Latch Enable Input
$I_0-I_{15}$	Inputs
$O_0-O_{15}$	Outputs

	SSOP EIAJ	TSSOP JEDEC
Order Number	74LCX16373MEA 74LCX16373MEAX	74LCX16373MTD 74LCX16373MTDX
See NS Package Number	MS48A	MTD48

### Connection Diagram

Pin Assignment for SSOP and TSSOP



Preliminary Data: National Semiconductor reserves the right to make changes at any time without notice.

## Functional Description

The LCX16373 contains sixteen D-type latches with TRI-STATE standard outputs. The device is byte controlled with each byte functioning identically, but independent of the other. Control pins can be shorted together to obtain full 16-bit operation. The following description applies to each byte. When the Latch Enable ( $LE_n$ ) input is HIGH, data on the  $D_n$  enters the latches. In this condition the latches are transparent, i.e. a latch output will change states each time its D input changes. When  $LE_n$  is LOW, the latches store information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of  $LE_n$ . The TRI-STATE standard outputs are controlled by the Output Enable ( $\overline{OE}_n$ ) input. When  $\overline{OE}_n$  is LOW, the standard outputs are in the 2-state mode. When  $\overline{OE}_n$  is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

## Truth Tables

Inputs			Outputs
$LE_1$	$\overline{OE}_1$	$I_0-I_7$	$O_0-O_7$
X	H	X	Z
H	L	L	L
H	H	H	H
L	L	X	$O_0$

Inputs			Outputs
$LE_2$	$\overline{OE}_2$	$I_8-I_{15}$	$O_8-O_{15}$
X	H	X	Z
H	L	L	L
H	H	H	H
L	L	X	$O_0$

H = High Voltage Level

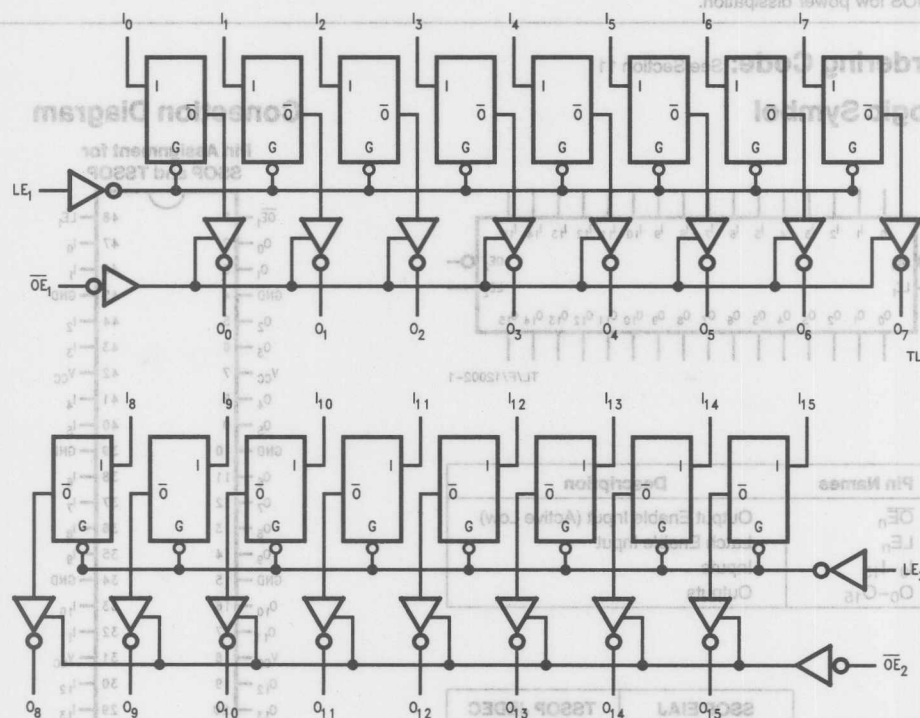
L = Low Voltage Level

X = Immaterial

Z = High Impedance

$O_0$  = Previous  $O_0$  before HIGH to LOW transition of Latch Enable

## Logic Diagrams



TL/F/12002-3

TL/F/12002-4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Input Voltage ( $V_I$ )	-0.5V to +7.0V
Output Voltage ( $V_O$ )	
Outputs TRI-STATE	-0.5V to +7.0V
Outputs Active (Note 2)	-0.5V to $V_{CC}$ + 0.5V
DC Input Diode Current ( $I_{IK}$ ) $V_I < 0$	-50 mA
DC Output Diode Current ( $I_{OK}$ )	
$V_O < 0$	-50 mA
$V_O > V_{CC}$	+50 mA
DC Output Source/Sink Current ( $I_{OH}/I_{OL}$ )	±50 mA
DC $V_{CC}$ or Ground Current per Supply Pin ( $I_{CC}$ or $I_{GND}$ )	±100 mA
Storage Temperature Range ( $T_{STG}$ )	-65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2:  $I_O$  Absolute Maximum Rating must be observed.

**Recommended Operating Conditions**

Supply Voltage	
Operating	2.0V to 3.6V
Data Retention Only	1.5V to 3.6V
Input Voltage ( $V_I$ )	0.0V to 5.5V
Output Voltage ( $V_O$ )	
Output in Active State	0.0V to $V_{CC}$
Output in "OFF" State	0.0V to 5.5V
Output Current $I_{OH}/I_{OL}$	
$V_{CC} = 3.0V$ to 3.6V	±24 mA
$V_{CC} = 2.7V$ to 3.0V	±12 mA
Free Air Operating Temperature ( $T_A$ )	-40°C to +85°C
Minimum Input Edge Rate ( $\Delta t/\Delta V$ )	
$V_{IN} = 0.8V$ to 2.0V, $V_{CC} = 3.0V$	10 ns/V

**DC Electrical Characteristics**

Symbol	Parameter	$V_{CC}$ (V)	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		Units	Conditions
			Min	Max		
$V_{IH}$	High Level Input Voltage	2.7-3.6	2.0		V	$V_{OUT} \leq 0.1V$ or $\geq V_{CC} - 0.1V$
$V_{IL}$	Low Level Input Voltage	2.7-3.6		0.8		
$V_{OH}$	High Level Output Voltage	2.7-3.6	$V_{CC} - 0.2$		V	$I_{OH} = -100 \mu A$ $I_{OH} = -12 \text{ mA}$ $I_{OH} = -18 \text{ mA}$ $I_{OH} = -24 \text{ mA}$
		2.7	2.2			
		3.0	2.4			
		3.0	2.2			
$V_{OL}$	Low Level Output Voltage	2.7-3.6		0.2	V	$I_{OL} = 100 \mu A$ $I_{OL} = 12 \text{ mA}$ $I_{OL} = 24 \text{ mA}$
		2.7		0.4		
		3.0		0.55		
$I_I$	Input Leakage Current	2.7-3.6		±5.0	$\mu A$	$0 \leq V_I \leq 5.5V$
$I_{OZ}$	TRI-STATE Output Leakage	2.7-3.6		±5.0	$\mu A$	$0 \leq V_O \leq 5.5V, V_I = V_{IH}$ or $V_{IL}$
$I_{OFF}$	Power Off Leakage Current	0		100	$\mu A$	$V_I$ or $V_O = 5.5V$
$I_{CC}$	Quiescent Supply Current	2.7-3.6		20	$\mu A$	$V_I = V_{CC}$ or GND
				±20	$\mu A$	$3.6 \leq (V_I, V_O) \leq 5.5V$
$\Delta I_{CC}$	Increase in $I_{CC}$ per Input	2.7-3.6		500	$\mu A$	$V_{IH} = V_{CC} - 0.6V$

**AC Electrical Characteristics:** See Section 2 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF		Units
			Min	Max (Note 2)	
t <sub>PHL</sub> , t <sub>PLH</sub>	Propagation Delay Data to Output	2.7 3.0–3.6	1.5 1.5	7.7 7.0	ns
t <sub>PHL</sub> , t <sub>PLH</sub>	Propagation Delay LE to Output	2.7 3.0–3.6	1.5 1.5	7.7 7.0	ns
t <sub>PZH</sub> , t <sub>PZL</sub>	Output Enable Time	2.7 3.0–3.6	1.5 1.5	8.0 7.2	ns
t <sub>PHZ</sub> , t <sub>PLZ</sub>	Output Disable Time	2.7 3.0–3.6	1.5 1.5	8.0 7.2	ns
t <sub>S</sub>	Setup Time	2.7 3.0–3.6	2.5 2.5		ns
t <sub>H</sub>	Hold Time	2.7 3.0–3.6	1.5 1.5		ns
t <sub>W</sub>	Clock Pulse Width	2.7 3.0–3.6	4.0 4.0		ns
t <sub>OSSL</sub> , t <sub>OSLH</sub>	Output to Output Skew (Note 1)	3.0		1.0	ns

**Note 1:** Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t<sub>OSSL</sub>) or LOW to HIGH (t<sub>OSLH</sub>). Parameter guaranteed by design.

**Note 2:** The maximum AC limits are design targets. Actual performance will be specified upon completion of characterization.

**Dynamic Switching Characteristics:** See Section 2 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = 25°C	Units	Conditions
			Typical		
V <sub>OLP</sub>	Quiet Output Dynamic Peak V <sub>OL</sub>	3.3	0.8	V	C <sub>L</sub> = 50 pF, V <sub>IH</sub> = 3.3V, V <sub>IL</sub> = 0V
V <sub>OLV</sub>	Quiet Output Dynamic Valley V <sub>OL</sub>	3.3	0.8	V	C <sub>L</sub> = 50 pF, V <sub>IH</sub> = 3.3V, V <sub>IL</sub> = 0V

**Capacitance**

Symbol	Parameter	Typical	Units	Conditions
C <sub>IN</sub>	Input Capacitance	7	pF	V <sub>CC</sub> = Open V <sub>I</sub> = 0V or V <sub>CC</sub>
C <sub>OUT</sub>	Output Capacitance	8	pF	V <sub>CC</sub> = 3.3V V <sub>I</sub> = 0V or V <sub>CC</sub>
C <sub>PD</sub>	Power Dissipation Capacitance	32	pF	V <sub>CC</sub> = 3.3V V <sub>I</sub> = 0V or V <sub>CC</sub> F = 10 MHz



## 74LCX16374

### Low-Voltage 16-Bit D Flip-Flop with 5V Tolerant Inputs and Outputs

#### General Description

The LCX16374 contains sixteen non-inverting D flip-flops with TRI-STATE® outputs and is intended for bus oriented applications. The device is byte controlled. A buffered clock (CP) and Output Enable (OE) are common to each byte and can be shorted together for full 16-bit operation.

The LCX16374 is designed for low voltage (3.3V)  $V_{CC}$  applications with capability of interfacing to a 5V signal environment.

The LCX16374 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

#### Features

- 5V tolerant inputs and outputs
- Ideal for low power/low noise 2.7V to 3.6V applications
- Power-down static overvoltage protection on input and output
- Outputs source/sink 24 mA
- Guaranteed simultaneous switching noise level
- Available in SSOP and TSSOP
- Implements patented Quiet Series noise/EMI reduction circuitry
- Functionally compatible with the 74 series 16374
- Latchup performance exceeds 300 mA
- ESD performance:  
Human Body Model > 2000V  
Machine Model > 250V

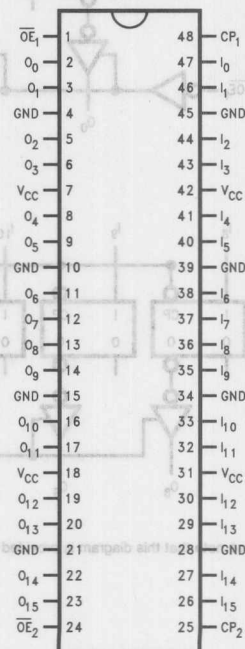
**Ordering Code:** See Section 11

#### Logic Symbol



#### Connection Diagram

##### Pin Assignment for SSOP and TSSOP



Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active Low)
$CP_n$	Clock Pulse Input
$I_0-I_{15}$	Inputs
$O_0-O_{15}$	Outputs

	SSOP EIAJ	TSSOP JEDEC
Order Number	74LCX16374MEA 74LCX16374MEAX	74LCX16374MTD 74LCX16374MTDX
See NS Package Number	MS48A	MTD48

Preliminary Data: National Semiconductor reserves the right to make changes at any time without notice.

## Functional Description

The LCX16374 consists of sixteen edge-triggered flip-flops with individual D-type inputs and TRI-STATE true outputs. The device is byte controlled with each byte functioning identically, but independent of the other. The control pins can be shorted together to obtain full 16-bit operation. Each byte has a buffered clock and buffered Output Enable common to all flip-flops within that byte. The description which follows applies to each byte. Each flip-flop will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock ( $CP_n$ ) transition. With the Output Enable ( $OE_n$ ) LOW, the contents of the flip-flops are available at the outputs. When  $OE_n$  is HIGH, the outputs go to the high impedance state. Operation of the  $OE_n$  input does not affect the state of the flip-flops.

## Truth Tables

Inputs			Outputs
$CP_1$	$OE_1$	$I_0-I_7$	$O_0-O_7$
—	L	H	H
—	L	L	L
L	L	X	$O_0$
X	H	X	Z

Inputs			Outputs
$CP_2$	$OE_2$	$I_8-I_{15}$	$O_8-O_{15}$
—	L	H	H
—	L	L	L
L	L	X	$O_8$
X	H	X	Z

H = High Voltage Level

L = Low Voltage Level

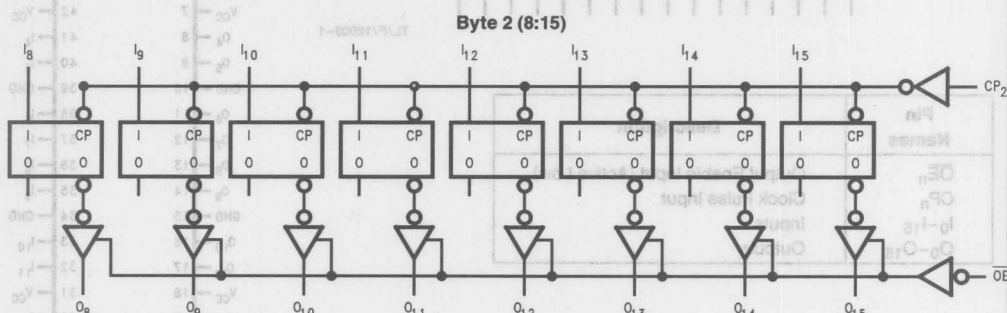
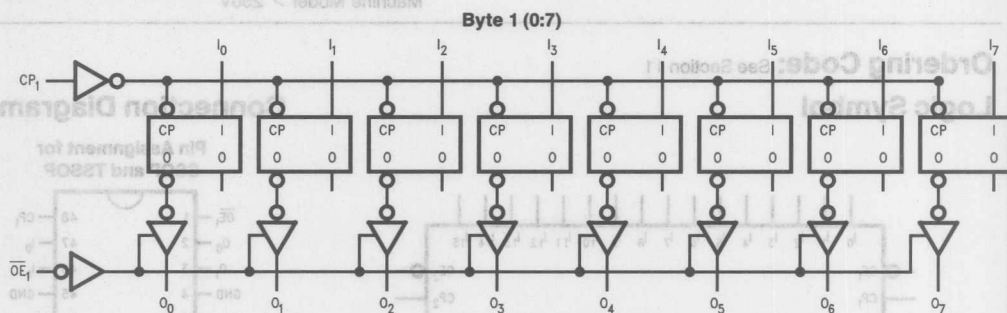
X = Immaterial

Z = High Impedance

$O_0$  = Previous  $O_0$  before HIGH to LOW of  $CP_1$

$O_8$  = Previous  $O_8$  before HIGH to LOW of  $CP_2$

## Logic Diagrams



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Input Voltage ( $V_I$ )	-0.5V to +7.0V
Output Voltage ( $V_O$ )	-0.5V to +7.0V
Outputs TRI-STATE	-0.5V to +7.0V
Outputs Active (Note 2)	-0.5V to $V_{CC} + 0.5V$
DC Input Diode Current ( $I_{IK}$ )	
$V_I < 0$	-50 mA
DC Output Diode Current ( $I_{OK}$ )	
$V_O < 0$	-50 mA
$V_O > V_{CC}$	+50 mA
DC Output Source/Sink Current ( $I_{OH}/I_{OL}$ )	+50 mA
DC $V_{CC}$ or Ground Current per Supply Pin ( $I_{CC}$ or $I_{GND}$ )	$\pm 100$ mA
Storage Temperature Range ( $T_{STG}$ )	-65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2:  $I_O$  Absolute Maximum Rating must be observed.

**Recommended Operating Conditions**

Supply Voltage ( $V_{CC}$ )		Symbol
Operating	2.0V to 3.6V	
Data Retention Only	1.5V to 3.6V	
Input Voltage ( $V_I$ )	0.0V to 5.5V	
Output Voltage ( $V_O$ )		
Output in Active State	0.0V to $V_{CC}$	
Output in "OFF" State	0.0V to 5.5V	
Output Current $I_{OH}/I_{OL}$		
$V_{CC} = 3.0V$ to $3.6V$	$\pm 24$ mA	
$V_{CC} = 2.7V$ to $3.0V$	$\pm 12$ mA	
Free Air Operating Temperature ( $T_A$ )	-40°C to +85°C	
Minimum Input Edge Rate ( $\Delta t/\Delta V$ )		
$V_{IN} = 0.8V$ to $2.0V$ , $V_{CC} = 3.0V$	10 ns/V	

**DC Electrical Characteristics**

Symbol	Parameter	$V_{CC}$ (V)	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		Units	Conditions
			Min	Max		
$V_{IH}$	High Level Input Voltage	2.7-3.6	2.0		V	$V_{OUT} \leq 0.1V$ or $\geq V_{CC} - 0.1V$
$V_{IL}$	Low Level Input Voltage	2.7-3.6		0.8		
$V_{OH}$	High Level Output Voltage	2.7-3.6	$V_{CC} - 0.2$		V	$I_{OH} = -100 \mu A$ $I_{OH} = -12 \text{ mA}$ $I_{OH} = -18 \text{ mA}$ $I_{OH} = -24 \text{ mA}$
$V_{OL}$	Low Level Output Voltage	2.7-3.6		0.2	V	$I_{OL} = 100 \mu A$ $I_{OL} = 12 \text{ mA}$ $I_{OL} = 24 \text{ mA}$
$I_I$	Input Leakage Current	2.7-3.6		$\pm 5.0$	$\mu A$	$0 \leq V_I \leq 5.5V$
$I_{OZ}$	TRI-STATE Output Leakage	2.7-3.6		$\pm 5.0$	$\mu A$	$0 \leq V_O \leq 5.5V$ $V_L = V_{IH}$ or $V_{IL}$
$I_{OFF}$	Power Off Leakage Current	0		100	$\mu A$	$V_I$ or $V_O = 5.5V$
$I_{CC}$	Quiescent Supply Current	2.7-3.6		20 $\pm 20$	$\mu A$	$V_I = V_{CC}$ or GND $3.6 \leq (V_I, V_O) \leq 5.5V$
$\Delta I_{CC}$	Increase in $I_{CC}$ per Input	2.7-3.6		500	$\mu A$	$V_{IH} = V_{CC} - 0.6V$

**AC Electrical Characteristics:** See Section 2 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF		Units
			Min	Max (Note 2)	
t <sub>PHL</sub> , t <sub>PLH</sub>	Propagation Delay CP to Output	2.7 3.0–3.6	1.5 1.5	7.7 7.0	ns
t <sub>PZH</sub> , t <sub>PZL</sub>	Output Enable Time	2.7 3.0–3.6	1.5 1.5	8.0 7.2	ns
t <sub>PHZ</sub> , t <sub>PLZ</sub>	Output Disable Time	2.7 3.0–3.6	1.5 1.5	8.0 7.2	ns
t <sub>S</sub>	Setup Time	2.7 3.0–3.6	2.5 2.5		ns
t <sub>H</sub>	Hold Time	2.7 3.0–3.6	1.5 1.5		ns
t <sub>w</sub>	Pulse Width	2.7 3.0–3.6	4.0 4.0		ns
T <sub>OSSL</sub> , T <sub>OSLH</sub>	Output to Output Skew (Note 1)	3.0		1.0	ns

**Note 1:** Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t<sub>OSSL</sub>) or LOW to HIGH (t<sub>OSLH</sub>). Parameter guaranteed by design.

**Note 2:** The maximum AC limits are design targets. Actual performance will be specified upon completion of characterization.

**Dynamic Switching Characteristics:** See Section 2 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = 25°C		Conditions
			Typical	Units	
V <sub>OLP</sub>	Quiet Output Dynamic Peak V <sub>OL</sub>	3.3	0.8	V	C <sub>L</sub> = 50 pF, V <sub>IH</sub> = 3.3V, V <sub>IL</sub> = 0V
V <sub>OLV</sub>	Quiet Output Dynamic Valley V <sub>OL</sub>	3.0	0.8	V	C <sub>L</sub> = 50 pF, V <sub>IH</sub> = 3.3V, V <sub>IL</sub> = 0V

**Capacitance**

Symbol	Parameter	Typical	Units	Conditions
C <sub>IN</sub>	Input Capacitance	7	pF	V <sub>CC</sub> = Open V <sub>I</sub> = 0V or V <sub>CC</sub>
C <sub>OUT</sub>	Output Capacitance	8	pF	V <sub>CC</sub> = 3.3V V <sub>I</sub> = 0V or V <sub>CC</sub>
C <sub>PD</sub>	Power Dissipation Capacitance	32	pF	V <sub>CC</sub> = 3.3V V <sub>I</sub> = 0V or V <sub>CC</sub> F = 10 MHz

## 74LCX16646

# Low-Voltage 16-Bit Transceiver/Register with 5V Tolerant Inputs and Outputs

## General Description

The LCX16646 contains sixteen non-inverting bidirectional registered bus transceivers with TRI-STATE® outputs, providing multiplexed transmission of data directly from the input bus or from the internal storage registers. Each byte has separate control inputs which can be shorted together for full 16-bit operation. The DIR inputs determine the direction of data flow through the device. The CPAB and CPBA inputs load data into the registers on the LOW-to-HIGH transition. The four fundamental handling functions available are illustrated in Figure 1 thru Figure 4.

The LCX16646 is designed for low voltage (3.3V)  $V_{CC}$  applications with capability of interfacing to a 5V signal environment.

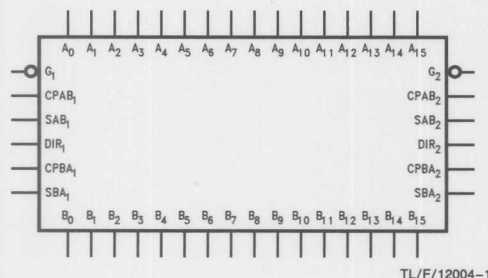
The LCX16646 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

## Features

- 5V tolerant inputs and outputs
- Ideal for low power/low noise 2.7V to 3.6V applications
- Power-down static overvoltage protection on inputs and outputs
- Outputs source/sink 24 mA
- Guaranteed simultaneous switching noise level
- Available in SSOP and TSSOP
- Implements patented Quiet Series noise/EMI reduction circuitry
- Functionally compatible with the 74 series 16646
- Latchup performance exceeds 300 mA
- ESD performance:
  - Human Body Model < 2000V
  - Machine Model < 250V

**Ordering Code:** See Section 11

## Logic Symbol

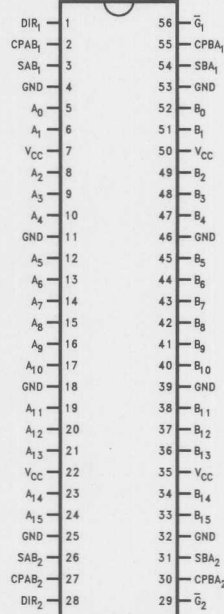


	SSOP EIAJ	TSSOP JEDEC
Order Number	74LCX16646MEA 74LCX16646MEAX	74LCX16646MTD 74LCX16646MTDX
See NS Package Number	MS56A	MTD56

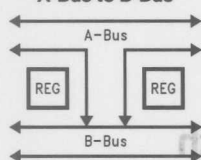
**Preliminary Data:** National Semiconductor reserves the right to make changes at any time without notice.

## Connection Diagram

### Pin Assignment for SSOP and TSSOP

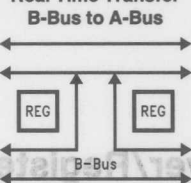


Real Time Transfer  
A-Bus to B-Bus



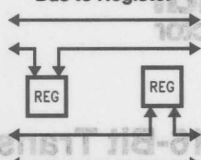
TL/F/12004-3  
FIGURE 1

Real Time Transfer  
B-Bus to A-Bus



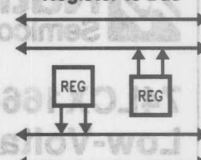
TL/F/12004-4  
FIGURE 2

Storage from  
Bus to Register



TL/F/12004-5  
FIGURE 3

Transfer from  
Register to Bus



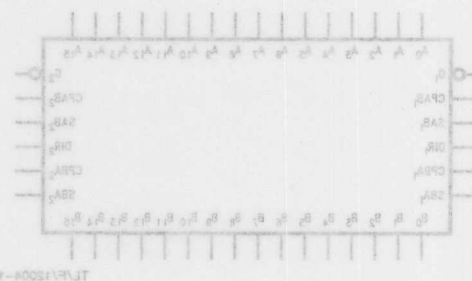
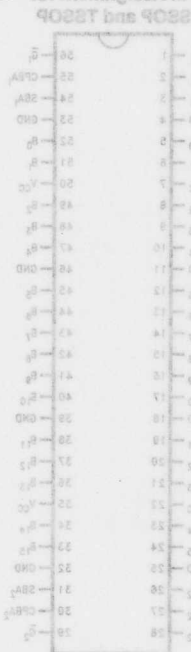
TL/F/12004-6  
FIGURE 4

# Function Table (Note)

Inputs						Data I/O		Output Operation Mode
G <sub>1</sub>	DIR <sub>1</sub>	CPAB <sub>1</sub>	CPBA <sub>1</sub>	SAB <sub>1</sub>	SBA <sub>1</sub>	A <sub>0-7</sub>	B <sub>0-7</sub>	
H	X	H or L	H or L	X	X	Input	Input	Isolation
H	X	↗	X	X	X			Clock An Data into A Register
H	X	X	↗	X	X			Clock Bn Data into B Register
L	H	X	X	L	X	Input	Output	An to Bn—Real Time (Transparent Mode)
L	H	↗	X	L	X			Clock An Data to A Register
L	H	H or L	X	H	X			A Register to Bn (Stored Mode)
L	H	↗	X	H	X	Output	Input	Clock An Data into A Register and Output to Bn
L	L	X	X	X	L			Bn to An—Real Time (Transparent Mode)
L	L	X	↗	X	L			Clock Bn Data into B Register
L	L	X	H or L	X	H			B Register to An (Stored Mode)
L	L	X	↗	X	H			Clock Bn into B Register and Output to An

**Note:** The data output functions may be enabled or disabled by various signals at the G and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the appropriate clock inputs. Also applies to data I/O (A and B; 8-15) and #2 control pins.

H = HIGH Voltage Level X = Immaterial  
L = LOW Voltage Level ↗ = LOW-to-HIGH Transition.



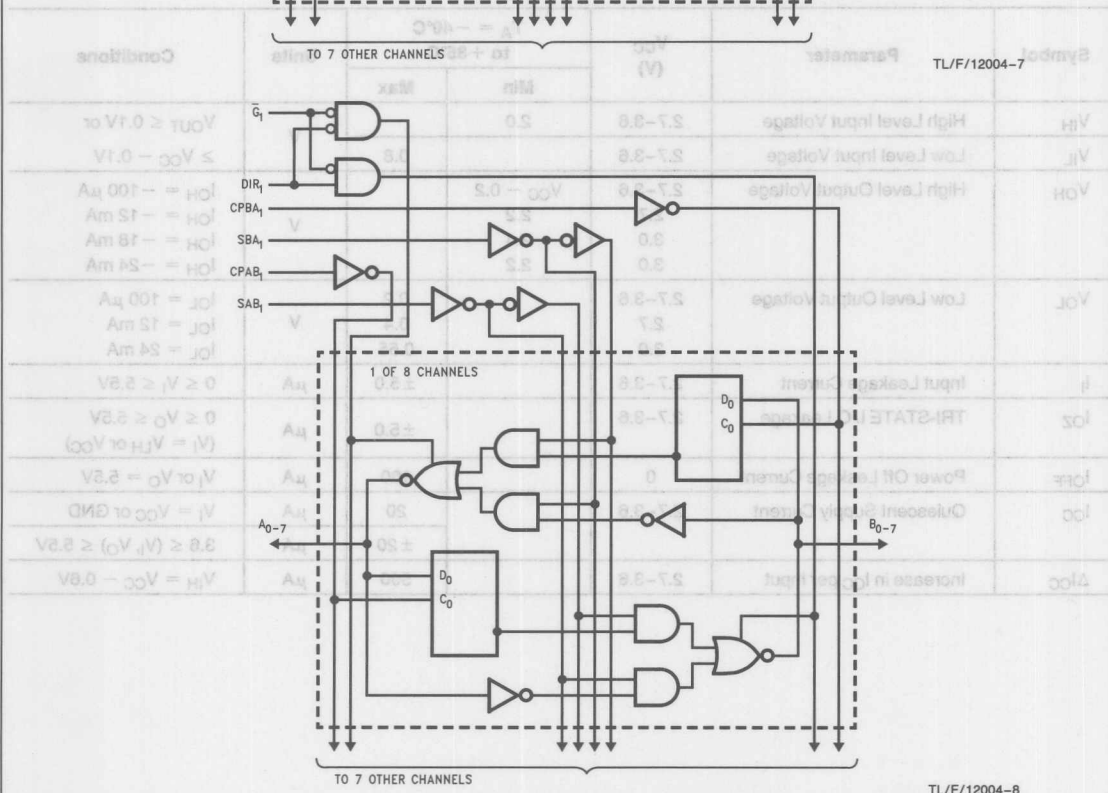
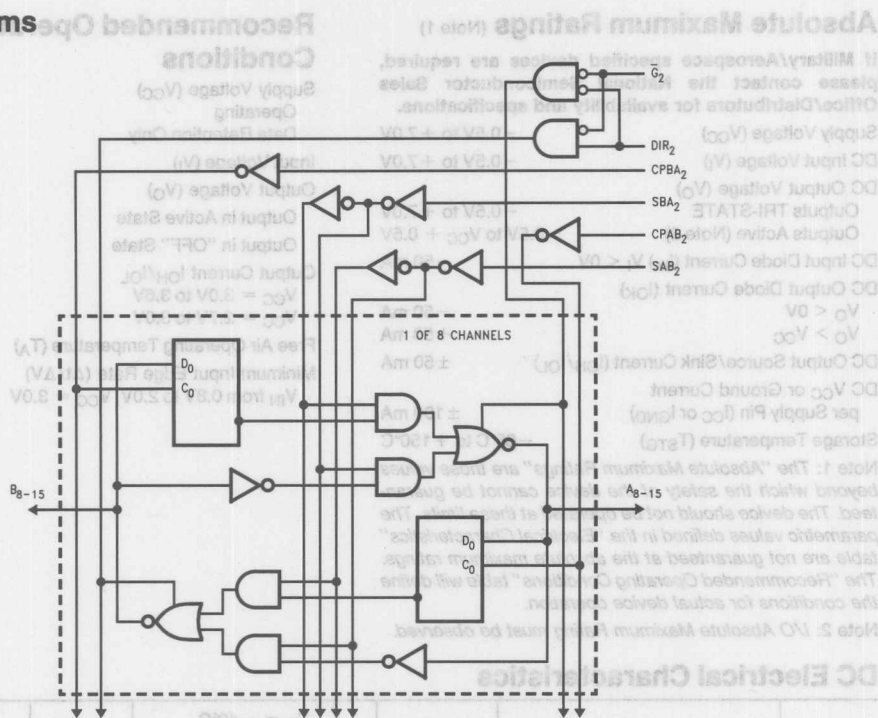
Order Number	MS8A	MS8B
74LCX16646MTD	74LCX16646MTD	74LCX16646MTD
74LCX16646MTDX	74LCX16646MTDX	74LCX16646MTDX

Preliminary Data: National Semiconductor reserves the right to make changes at any time without notice.

# Logic Diagrams

Operating  
Supply Voltage (V<sub>CC</sub>)  
0V to 5.5V  
1.5V to 3.5V  
2.0V to 3.5V

Output in Active State  
Output in "OFF" State  
Output Current (I<sub>OL</sub>)  
V<sub>CC</sub> = 3.0V to 3.5V  
±24 mA  
±15 mA  
-40°C to +85°C  
10 nA



Please note that these diagrams are provided only for the understanding of logic operations and should not be used to estimate propagation delays.

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Input Voltage ( $V_I$ )	-0.5V to +7.0V
DC Output Voltage ( $V_O$ )	-0.5V to +7.0V
Outputs TRI-STATE	-0.5V to $V_{CC} + 0.5V$
Outputs Active (Note 2)	-0.5V to $V_{CC} + 0.5V$
DC Input Diode Current ( $I_{IK}$ ) $V_I < 0V$	-50 mA
DC Output Diode Current ( $I_{OK}$ )	-50 mA
$V_O < 0V$	+50 mA
$V_O > V_{CC}$	+50 mA
DC Output Source/Sink Current ( $I_{OH}/I_{OL}$ )	$\pm 50$ mA
DC $V_{CC}$ or Ground Current per Supply Pin ( $I_{CC}$ or $I_{GND}$ )	$\pm 100$ mA
Storage Temperature ( $T_{STG}$ )	-65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I/O Absolute Maximum Rating must be observed.

**Recommended Operating Conditions**

Supply Voltage ( $V_{CC}$ )	2.0V to 3.6V
Operating	1.5V to 3.6V
Data Retention Only	0V to 5.5V
Input Voltage ( $V_I$ )	0V to 5.5V
Output Voltage ( $V_O$ )	0.0V to $V_{CC}$
Output in Active State	0V to 5.5V
Output in "OFF" State	0V to 5.5V
Output Current $I_{OH}/I_{OL}$	$\pm 24$ mA
$V_{CC} = 3.0V$ to 3.6V	$\pm 12$ mA
$V_{CC} = 2.7V$ to 3.0V	$\pm 12$ mA
Free Air Operating Temperature ( $T_A$ )	-40°C to +85°C
Minimum Input Edge Rate ( $\Delta t/\Delta V$ )	10 ns/V
$V_{IN}$ from 0.8V to 2.0V, $V_{CC} = 3.0V$	

**DC Electrical Characteristics**

Symbol	Parameter	$V_{CC}$ (V)	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$		Units	Conditions
			Min	Max		
$V_{IH}$	High Level Input Voltage	2.7-3.6	2.0		V	$V_{OUT} \leq 0.1V$ or $\geq V_{CC} - 0.1V$
$V_{IL}$	Low Level Input Voltage	2.7-3.6		0.8	V	
$V_{OH}$	High Level Output Voltage	2.7-3.6	$V_{CC} - 0.2$		V	$I_{OH} = -100 \mu A$ $I_{OH} = -12 \text{ mA}$ $I_{OH} = -18 \text{ mA}$ $I_{OH} = -24 \text{ mA}$
$V_{OL}$	Low Level Output Voltage	2.7-3.6		0.2	V	$I_{OL} = 100 \mu A$ $I_{OL} = 12 \text{ mA}$ $I_{OL} = 24 \text{ mA}$
$I_I$	Input Leakage Current	2.7-3.6		$\pm 5.0$	$\mu A$	$0 \leq V_I \leq 5.5V$
$I_{OZ}$	TRI-STATE I/O Leakage	2.7-3.6		$\pm 5.0$	$\mu A$	$0 \leq V_O \leq 5.5V$ ( $V_I = V_{LH}$ or $V_{CC}$ )
$I_{OFF}$	Power Off Leakage Current	0		100	$\mu A$	$V_I$ or $V_O = 5.5V$
$I_{CC}$	Quiescent Supply Current	2.7-3.6		20	$\mu A$	$V_I = V_{CC}$ or GND
				$\pm 20$	$\mu A$	$3.6 \leq (V_I, V_O) \leq 5.5V$
$\Delta I_{CC}$	Increase in $I_{CC}$ per Input	2.7-3.6		500	$\mu A$	$V_{IH} = V_{CC} - 0.6V$

**AC Electrical Characteristics:** See Section 2 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF		Units
			Min	Max (Note 2)	
T <sub>PHL</sub> , T <sub>PLH</sub>	Propagation Delay Bus to Bus	2.7 3.0–3.6	1.5 1.5	6.6 6.0	ns
T <sub>PHL</sub> , T <sub>PLH</sub>	Propagation Delay Clock to Bus	2.7 3.0–3.6	1.5 1.5	8.3 7.5	ns
T <sub>PHL</sub> , T <sub>PLH</sub>	Propagation Delay SAB or SBA to A <sub>n</sub> or B <sub>n</sub>	2.7 3.0–3.6	1.5 1.5	8.3 7.5	ns
T <sub>PZH</sub> , T <sub>PZL</sub>	Output Enable Time $\bar{G}$ to A <sub>n</sub> or B <sub>n</sub>	2.7 3.0–3.6	1.5 1.5	8.3 7.5	ns
T <sub>PHZ</sub> , T <sub>PLZ</sub>	Output Disable Time $\bar{G}$ to A <sub>n</sub> or B <sub>n</sub>	2.7 3.0–3.6	1.5 1.5	8.3 7.5	ns
T <sub>PZH</sub> , T <sub>PZL</sub>	Output Enable Time DIR to A <sub>n</sub> or B <sub>n</sub>	2.7 3.0–3.6	1.5 1.5	8.3 7.5	ns
T <sub>PHZ</sub> , T <sub>PLZ</sub>	Output Disable Time DIR to A <sub>n</sub> or B <sub>n</sub>	2.7 3.0–3.6	1.5 1.5	8.3 7.5	ns
t <sub>S</sub>	Setup Time	2.7 3.0–3.6	2.5 2.5		ns
t <sub>H</sub>	Hold Time	2.7 3.0–3.6	1.5 1.5		ns
t <sub>W</sub>	Pulse Width	2.7 3.0–3.6	4.0 4.0		ns
T <sub>OSSL</sub> , T <sub>OSLH</sub>	Output to Output Skew (Note 1)	3.0		1.0	ns

**Note 1:** Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t<sub>OSSL</sub>) or LOW to HIGH (t<sub>OSLH</sub>). Parameter guaranteed by design.

**Note 2:** The maximum AC limits are design targets. Actual performance will be specified upon completion of characterization.

**Dynamic Switching Characteristics:** See Section 2 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = 25°C	Units	Conditions
			Typical		
V <sub>OLP</sub>	Quiet Output Dynamic Peak V <sub>OL</sub>	3.3	0.8	V	C <sub>L</sub> = 50 pF, V <sub>IH</sub> = 3.3V, V <sub>IL</sub> = 0V
V <sub>OLV</sub>	Quiet Output Dynamic Valley V <sub>OL</sub>	3.3	0.8	V	C <sub>L</sub> = 50 pF, V <sub>IH</sub> = 3.3V, V <sub>IL</sub> = 0V

**Capacitance**

Symbol	Parameter	Typical	Units	Conditions
C <sub>IN</sub>	Input Capacitance	7	pF	V <sub>CC</sub> = Open V <sub>I</sub> = 0V or V <sub>CC</sub>
C <sub>I/O</sub>	Input/Output Capacitance	8	pF	V <sub>CC</sub> = 3.3V V <sub>I</sub> = 0V or V <sub>CC</sub>
C <sub>PD</sub>	Power Dissipation Capacitance	32	pF	V <sub>CC</sub> = 3.3V V <sub>I</sub> = 0V or V <sub>CC</sub> F = 10 MHz



PRELIMINARY

## 74LCX16652 Low-Voltage Transceiver/Register with 5V Tolerant Inputs and Outputs

### General Description

The LCX16652 contains sixteen non-inverting bidirectional bus transceivers with TRI-STATE® outputs providing multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to the HIGH logic level. Output Enable pins (OEAB, OEBA) are provided to control the transceiver function.

The LCX16652 is designed for low-voltage (3.3V)  $V_{CC}$  applications with capability of interfacing to a 5V signal environment.

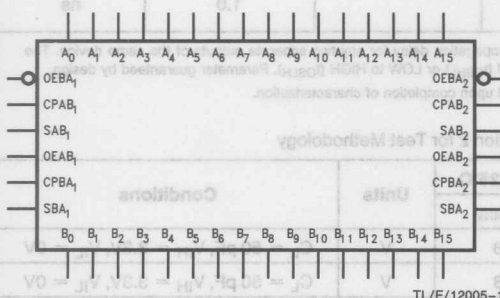
The LCX16652 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

### Features

- 5V tolerant inputs and outputs
- Ideal for low power/low noise 2.7 to 3.6V applications
- Power-down static overvoltage protection on inputs and outputs
- Outputs source/sink 24 mA
- Guaranteed simultaneous switching noise level
- Available in SSOP and TSSOP
- Implements patented Quiet Series noise/EMI reduction circuitry
- Functionally compatible with the 74 series 16652
- Latch-up performance exceeds 300 mA
- ESD performance:  
Human Body Model > 2000V  
Machine Model > 250V

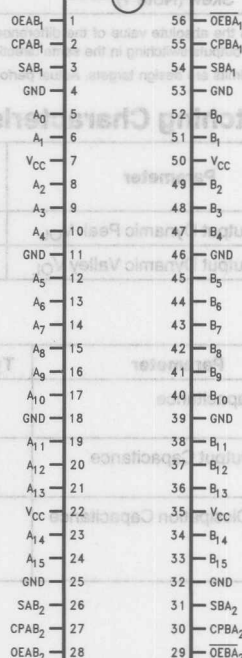
**Ordering Code:** See Section 11

### Logic Symbol



### Connection Diagram

Pin Assignment for  
SSOP and TSSOP



	SSOP EIAJ	TSSOP JEDEC
Order Number	74LCX16652MEA 74LCX16652MEAX	74LCX16652MTD 74LCX16652MTDX
See NS Package Number	MS56A	MTD56

**Preliminary Data:** National Semiconductor reserves the right to make changes at any time without notice.

## Functional Description

In the transceiver mode, data present at the HIGH impedance port may be stored in either the A or B register or both. The select ( $SAB_n$ ,  $SBA_n$ ) controls can multiplex stored and real-time.

The examples in Figure 1 demonstrate the four fundamental bus-management functions that can be performed with the 74LCX16652.

Data on the A or B data bus, or both can be stored in the internal D flip-flop by LOW to HIGH transitions at the ap-

propriate Clock Inputs ( $CPAB_n$ ,  $CPBA_n$ ) regardless of the Select or Output Enable Inputs. When  $SAB$  and  $SBA$  are in the real time transfer mode, it is also possible to store data without using the internal D flip-flops by simultaneously enabling  $OEAB_n$  and  $OEBA_n$ . In this configuration each Output reinforces its Input. Thus when all other data sources to the two sets of bus lines are in a HIGH impedance state, each set of bus lines will remain at its last state.

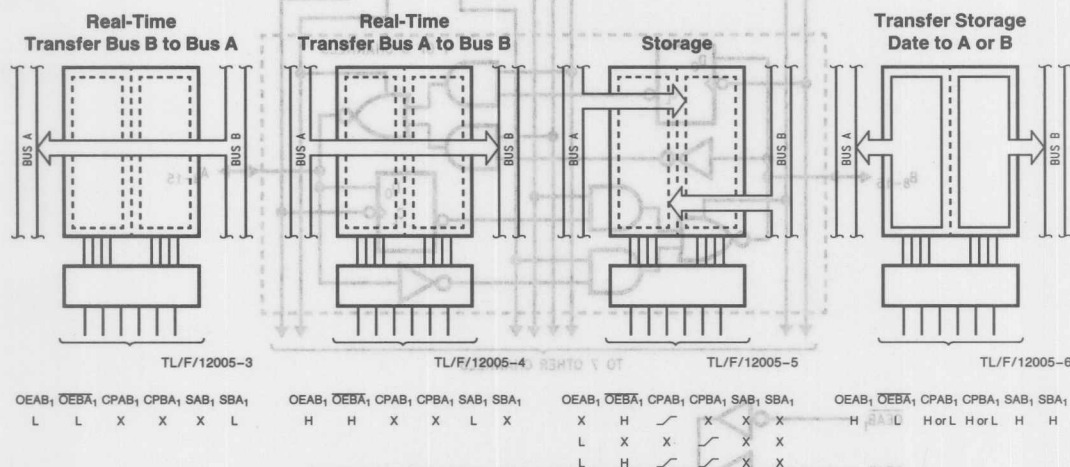


FIGURE 1

Function Table (Note)

Inputs						Inputs/Outputs		Operating Mode
OEAB <sub>1</sub>	OEBA <sub>1</sub>	CPAB <sub>1</sub>	CPBA <sub>1</sub>	SAB <sub>1</sub>	SBA <sub>1</sub>	A <sub>0</sub> thru A <sub>7</sub>	B <sub>0</sub> thru B <sub>7</sub>	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	/	/	X	X		Input	Store A and B Data
X	H	/	H or L	X	X	Input	Not Specified	State A, Hold B
H	H	/	/	X	X	Input	Output	Store A in Both Registers
L	X	H or L	/	X	X	Not Specified	Input	Hold A, Store B
L	L	/	/	X	X	Output	Input	Store B in Both Registers
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus
L	L	X	H or L	X	H		Input	Store B Data to A Bus
H	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus
H	H	H or L	X	H	X			Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored A Data to B Bus and Stored B Data to A Bus

H = HIGH Voltage Level

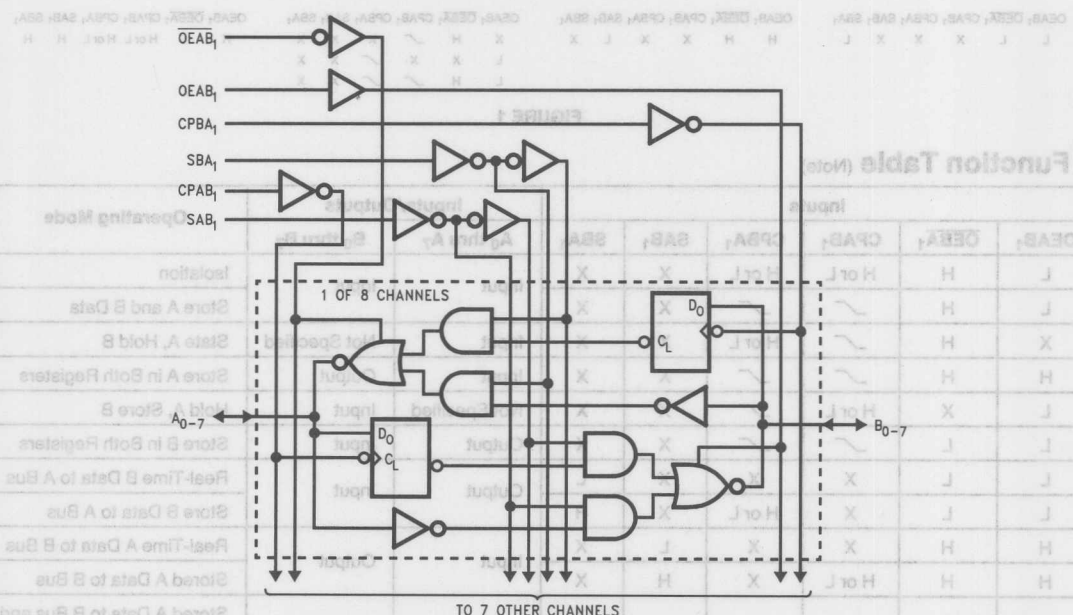
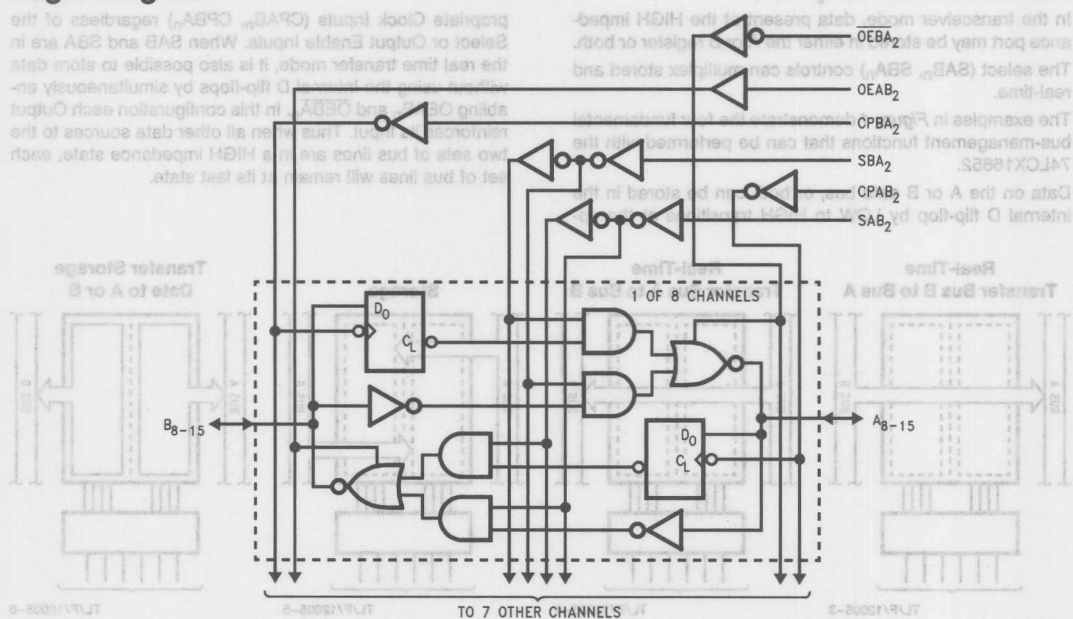
L = LOW Voltage Level

X = Immaterial

/ = LOW to HIGH Clock Transition

**Note:** The data output functions may be enabled or disabled by various signals at OEAB or OEBA inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW to HIGH transition on the clock inputs. This also applies to data I/O (A and B: 8–15) and #2 control pins.

## Logic Diagram



Please note that these diagrams are provided only for the understanding of logic operations and should not be used to estimate propagation delays.

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Input Voltage ( $V_I$ )	-0.5V to +7.0V
Output Voltage ( $V_O$ )	-0.5V to +7.0V
Outputs Tri-Stated	-0.5V to +7.0V
Outputs Active (Note 2)	-0.5V to $V_{CC} + 0.5V$
DC Input Diode Current ( $I_{IK}$ ) $V_I < 0$	-50 mA
DC Output Diode Current ( $I_{OK}$ )	
$V_O < 0$	-50 mA
$V_O > V_{CC}$	+50 mA
DC Output Source/Sink Current ( $I_{OH}/I_{OL}$ )	$\pm 50$ mA
DC $V_{CC}$ or Ground Current per Supply Pin ( $I_{CC}$ or $I_{GND}$ )	$\pm 100$ mA
Storage Temperature Range ( $T_{STG}$ )	-65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operation Conditions" table will define the conditions for actual device operation.

Note 2:  $I_O$  Absolute Maximum Rating must be observed.

**Recommended Operating Conditions**

Supply Voltage	
Operating	2.0V to 3.6V
Data Retention Only	1.5V to 3.6V
Input Voltage ( $V_I$ )	0V to 5.5V
Output Voltage ( $V_O$ )	
Output in Active State	0V to $V_{CC}$
Output in "OFF" State	0V to 5.5V
Output Current $I_{OH}/I_{OL}$	
$V_{CC} = 3.0V$ to $3.6V$	$\pm 24$ mA
$V_{CC} = 2.7V$ to $3.0V$	$\pm 12$ mA
Free Air Operating Temperature ( $T_A$ )	-40°C to +85°C
Minimum Input Edge Rate ( $\Delta V/\Delta t$ )	
$V_{IN} = 0.8V$ to $2.0V$ , $V_{CC} = 3.0V$	10 ns/V

**DC Electrical Characteristics**

Symbol	Parameter	$V_{CC}$ (V)	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		Units	Conditions
			Min	Max		
$V_{IH}$	High Level Input Voltage	2.7-3.6	2.0		V	$V_{OUT} \leq 0.1V$ or $\geq V_{CC} - 0.1V$
$V_{IL}$	Low Level Input Voltage	2.7-3.6		0.8		
$V_{OH}$	High Level Output Voltage	2.7-3.6 2.7 3.0 3.0	$V_{CC} - 0.2$ 2.2 2.4 2.2		V	$I_{OH} = -100 \mu\text{A}$ $I_{OH} = -12 \text{ mA}$ $I_{OH} = -18 \text{ mA}$ $I_{OH} = -24 \text{ mA}$
$V_{OL}$	Low Level Output Voltage	2.7-3.6 2.7 3.0		0.2 0.4 0.55	V	$I_{OL} = 100 \mu\text{A}$ $I_{OL} = 12 \text{ mA}$ $I_{OL} = 24 \text{ mA}$
$I_I$	Input Leakage Current	2.7-3.6		$\pm 5.0$	$\mu\text{A}$	$0 \leq V_I \leq 5.5V$
$I_{OZ}$	TRI-STATE I/O Leakage	2.7-3.6		$\pm 5.0$	$\mu\text{A}$	$0 \leq V_O \leq 5.5V$ $V_I = V_{IH}$ or $V_{IL}$
$I_{OFF}$	Power Off Leakage Current	0		100	$\mu\text{A}$	$V_I$ or $V_O = 5.5V$
$I_{CC}$	Quiescent Supply Current	2.7-3.6		20 $\pm 20$	$\mu\text{A}$	$V_I = V_{CC}$ or GND $3.6 \leq (V_I, V_O) \leq 5.5V$
$\Delta I_{CC}$	Increase in $I_{CC}$ per Input	2.7-3.6		500	$\mu\text{A}$	$V_{IH} = V_{CC} - 0.6V$

# AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = -40°C to +85°C, C <sub>L</sub> = 50 pF		Units
			Min	Max (Note 2)	
t <sub>PHL</sub>	Propagation Delay	2.7	1.5	6.6	ns
t <sub>PLH</sub>	Bus to Bus	3.0–3.6	1.5	6.0	ns
t <sub>PHL</sub>	Propagation Delay	2.7	1.5	8.3	ns
t <sub>PLH</sub>	Clock to Bus	3.0–3.6	1.5	7.5	ns
t <sub>PHL</sub>	Propagation Delay	2.7	1.5	8.3	ns
t <sub>PLH</sub>	SAB or SBA to A <sub>n</sub> or B <sub>n</sub>	3.0–3.6	1.5	7.5	ns
t <sub>PZH</sub>	Output Enable Time	2.7	1.5	8.3	ns
t <sub>PZL</sub>	OEBA to A <sub>n</sub> or B <sub>n</sub>	3.0–3.6	1.5	7.5	ns
t <sub>PHZ</sub>	Output Disable Time	2.7	1.5	8.3	ns
t <sub>PLZ</sub>	OEBA to A <sub>n</sub> or B <sub>n</sub>	3.0–3.6	1.5	7.5	ns
t <sub>PZH</sub>	Output Enable Time	2.7	1.5	8.3	ns
t <sub>PZL</sub>	OEAB to A <sub>n</sub> or B <sub>n</sub>	3.0–3.6	1.5	7.5	ns
t <sub>PHZ</sub>	Output Disable Time	2.7	1.5	8.3	ns
t <sub>PLZ</sub>	OEAB to A <sub>n</sub> or B <sub>n</sub>	3.0–3.6	1.5	7.5	ns
t <sub>s</sub>	Setup Time	2.7	2.5	2.5	ns
t <sub>H</sub>	Hold Time	2.7	1.5	1.5	ns
t <sub>w</sub>	Pulse Width	2.7	4.0	4.0	ns
t <sub>OSHL</sub>	Output to Output Skew	3.0			ns
t <sub>OSLH</sub>	(Note 1)			1.0	ns

**Note 1:** Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t<sub>OSHL</sub>) or LOW to HIGH (t<sub>OSLH</sub>). Parameter guaranteed by design.

**Note 2:** The maximum AC limits are design targets. Actual performance will be specified upon completion of characterization.

## Dynamic Switching Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	Typical	Units	Conditions
V <sub>OLP</sub>	Quiet Output Dynamic Peak V <sub>OL</sub>	3.3	0.8	V	C <sub>L</sub> = 50 pF, V <sub>IH</sub> = 3.3V, V <sub>IL</sub> = 0V
V <sub>OLV</sub>	Quiet Output Dynamic Valley V <sub>OL</sub>	3.3	0.8	V	C <sub>L</sub> = 50 pF, V <sub>IH</sub> = 3.3V, V <sub>IL</sub> = 0V

## Capacitance

Symbol	Parameter	Typical	Units	Conditions
C <sub>IN</sub>	Input Capacitance	7	pF	V <sub>CC</sub> = Open V <sub>I</sub> = 0V or V <sub>CC</sub>
C <sub>I/O</sub>	Input/Output Capacitance	8	pF	V <sub>CC</sub> = 3.3V V <sub>I</sub> = 0V or V <sub>CC</sub>
C <sub>PD</sub>	Power Dissipation Capacitance	32	pF	V <sub>CC</sub> = 3.3V V <sub>I</sub> = 0V or V <sub>CC</sub> F = 10 MHz



## Section 6 Contents

8-3	..... LVX Translator Family Features
8-4	..... 74LVX3245 8-Bit Dual Supply Translating Transceiver with TRI-STATE Outputs
8-9	..... 74LVX3245 8-Bit Dual Supply Translating Transceiver with TRI-STATE Outputs
	..... 74LVX3245 8-Bit Dual Supply Configurable Voltage Interface Transceiver with TRI-STATE
8-16	..... Outputs for 3V System
	..... 74LVX3245 8-Bit Dual Supply Configurable Voltage Interface Transceiver with TRI-STATE
8-21	..... Outputs

## Section 6

### LVX Translator Family



## Section 6 Contents

LVX Translator Family Features .....	6-3
74LVX3245 8-Bit Dual Supply Translating Transceiver with TRI-STATE Outputs .....	6-4
74LVX4245 8-Bit Dual Supply Translating Transceiver with TRI-STATE Outputs .....	6-9
74LVXC3245 8-Bit Dual Supply Configurable Voltage Interface Transceiver with TRI-STATE Outputs for 3V System .....	6-15
74LVXC4245 8-Bit Dual Supply Configurable Voltage Interface Transceiver with TRI-STATE Outputs .....	6-21

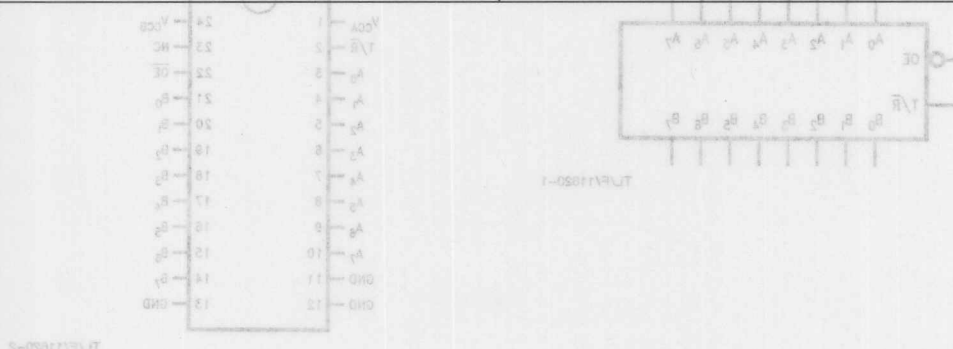
Section 6

LVX Translator Family

## LVX Translator Family

### Low Voltage Dual Supply CMOS Translating Transceivers

Features	Advantages
Advanced 0.8 $\mu\text{m}$ CMOS process	Propagation delays as fast as 7 ns maximum
Bi-directional interface between 3V and 5V system	Works as bus transceiver in 3V/5V mixed systems and also works like a 74 series 245 in the single supply system
$\pm 24$ mA drive current	Balanced drive, guaranteed incident wave switching into 50 $\Omega$ transmission line
Extended $V_{CC}$ range from 2.7V to 3.6V, compatible with JEDEC Std. No. 8-1B	Fully characterized for unregulated battery operation
Low standby current (50 $\mu\text{A}$ ) maximum	Saves power, extends battery life
Patented Quiet Series noise reduction circuitry	Guaranteed simultaneous switching noise level and dynamic threshold performance
Flexible $V_{CCB}$ operating range in Configurable Transceiver (LVXC)	Fits both 3V and 5V PCMCIA cards
B ports and $V_{CCB}$ allowed to float with Configurable Transceiver (LVXC)	Allows plug and remove PCMCIA cards freely
SOIC and QSOP packaging	Saves board space and weight



Pin Names	Description
OE	Output Enable Input
TR	Transceiver Input
A0-A7	Side A Inputs or TRI-STATE Outputs
B0-B7	Side B Inputs or TRI-STATE Outputs

Order Number	SOIC JEDEC	QSOP
74LVX245WM	74LVX245WM	74LVX245QSC
74LVX245MX	74LVX245MX	74LVX245SCX
See NS Package Number	MSB	MOB



## 74LVX3245

### 8-Bit Dual Supply Translating Transceiver with TRI-STATE® Outputs

#### General Description

The LVX3245 is a dual-supply, 8-bit translating transceiver that is designed to interface between a 3V bus and a 5V bus in a mixed 3V/5V supply environment. The Transmit/Receive (T/R) input determines the direction of data flow. Transmit (active-HIGH) enables data from A ports to B ports; Receive (active-LOW) enables data from B ports to A ports. The Output Enable input, when HIGH, disables both A and B ports by placing them in a HIGH Z condition. The A port interfaces with the 3V bus; the B port interfaces with the 5V bus.

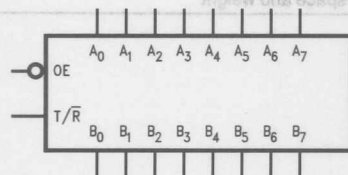
The LVX3245 is suitable for mixed voltage applications such as notebook computers using 3.3V CPU and 5V peripheral components.

#### Features

- Bidirectional interface between 3V and 5V buses
- Inputs compatible with TTL level
- 3V data flow at A port and 5V data flow at B port
- Outputs source/sink 24 mA
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Available in SOIC and QSOP packages
- Implements proprietary EMI reduction circuitry
- Functionally compatible with the 74 series 245

**Ordering Code:** See Section 1.1

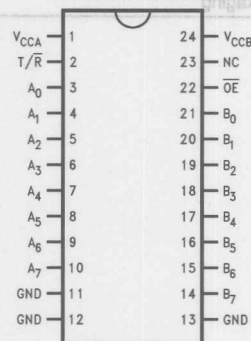
#### Logic Symbol



TL/F/11620-1

#### Connection Diagram

##### Pin Assignment for SOIC and QSOP



TL/F/11620-2

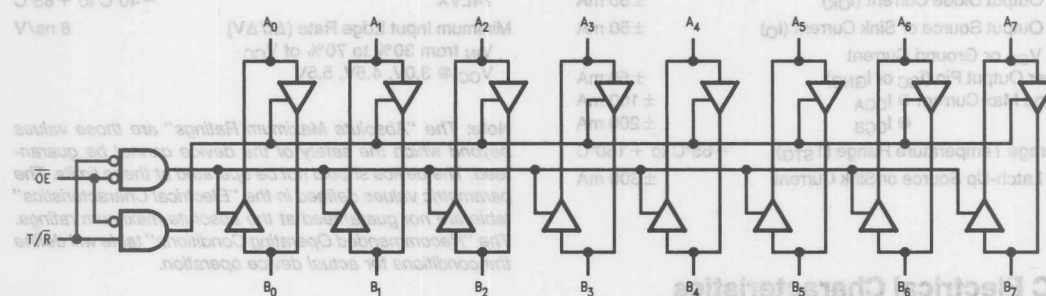
Pin Names	Description
$\overline{OE}$	Output Enable Input
T/R	Transmit/Receive Input
A <sub>0</sub> -A <sub>7</sub>	Side A Inputs or TRI-STATE Outputs
B <sub>0</sub> -B <sub>7</sub>	Side B Inputs or TRI-STATE Outputs

	SOIC JEDEC	QSOP
Order Number	74LVX3245WM 74LVX3245WMX	74LVX3245QSC 74LVX3245QSCX
See NS Package Number	M24B	MQA24

## Truth Table

Inputs		Outputs
$\overline{OE}$	T/R	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	HIGH-Z State

## Logic Diagram



4-0201-7/F/11620									
Symbol	Parameter	V <sub>CCA</sub> (V)	V <sub>CCB</sub> (V)	T <sub>A</sub> = +25°C		T <sub>A</sub> = -40°C to +85°C	Units	Conditions	
				Typ		Guaranteed Limits			
V <sub>IH</sub>	Minimum High Level Input Voltage	A(n), T/R	2.0	2.0	2.0	2.0	V	V <sub>OUT</sub> ≤ 0.1V or V <sub>CC</sub> - 0.1V	
V <sub>IHB</sub>		B(n)	2.0	2.0	2.0	2.0			
V <sub>IL</sub>	Maximum Low Level Input Voltage	A(n), T/R	0.8	0.8	0.8	0.8	V	V <sub>OUT</sub> ≤ 0.1V or V <sub>CC</sub> - 0.1V	
V <sub>ILB</sub>		B(n)	0.8	0.8	0.8	0.8			
V <sub>OH</sub>	Minimum High Level Output Voltage		2.0	2.0	2.0	2.0	V	I <sub>OH</sub> = -100 μA to -24 mA	
V <sub>OH</sub>			2.0	2.0	2.0	2.0			
V <sub>OL</sub>	Maximum Low Level Output Voltage		0.4	0.4	0.4	0.4	V	I <sub>OL</sub> = 100 μA to 24 mA	
V <sub>OLB</sub>			0.4	0.4	0.4	0.4			
I <sub>in</sub>	Maximum Input Leakage Current @ $\overline{OE}$ , T/R		2.0			±0.1	μA	V <sub>I</sub> = V <sub>CCB</sub> , GND	
I <sub>OL</sub>	Maximum TRI-STATE Output Leakage @ A(n)		2.0			±0.2	μA	V <sub>I</sub> = V <sub>IL</sub> , V <sub>IH</sub> = V <sub>CCA</sub> , $\overline{OE}$ = V <sub>CCA</sub> , V <sub>O</sub> = V <sub>CCB</sub> , GND	

please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CCA}$ , $V_{CCB}$ )	-0.5V to +7.0V
DC Input Voltage ( $V_I$ ) @ $\overline{OE}$ , T/ $\overline{R}$	-0.5V to $V_{CCB}$ + 0.5V
DC Input/Output Voltage ( $V_{I/O}$ )	
@ A(n)	-0.5V to $V_{CCA}$ + 0.5V
@ B(n)	-0.5V to $V_{CCB}$ + 0.5V
DC Input Diode Current ( $I_{IN}$ ) @ $\overline{OE}$ , T/ $\overline{R}$	$\pm 20$ mA
DC Output Diode Current ( $I_{OK}$ )	$\pm 50$ mA
DC Output Source or Sink Current ( $I_O$ )	$\pm 50$ mA
DC $V_{CC}$ or Ground Current	
per Output Pin ( $I_{CC}$ or $I_{GND}$ )	$\pm 50$ mA
and Max Current @ $I_{CCA}$	$\pm 100$ mA
@ $I_{CCB}$	$\pm 200$ mA
Storage Temperature Range ( $T_{STG}$ )	-65°C to +150°C
DC Latch-Up Source or Sink Current	$\pm 300$ mA

#### Supply Voltage

$V_{CCA}$	2.7V to 3.6V
$V_{CCB}$	4.5V to 5.5V
Input Voltage ( $V_I$ ) @ $\overline{OE}$ , T/ $\overline{R}$	0V to $V_{CCB}$
Input/Output Voltage ( $V_{I/O}$ )	
@ A(n)	0V to $V_{CCA}$
@ B(n)	0V to $V_{CCB}$

#### Free Air Operating Temperature ( $T_A$ )

74LVX	-40°C to +85°C
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#### Minimum Input Edge Rate ( $\Delta t/\Delta V$ )

$V_{IN}$ from 30% to 70% of $V_{CC}$	8 ns/V
--------------------------------------	--------

$V_{CC}$  @ 3.0V, 4.5V, 5.5V

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## DC Electrical Characteristics

Symbol	Parameter		V <sub>CCA</sub> (V)	V <sub>CCB</sub> (V)	74LVX3245		74LVX3245		Units	Conditions					
					T <sub>A</sub> = +25°C		T <sub>A</sub> = −40°C to +85°C								
					Type	Guaranteed Limits									
V <sub>IHA</sub>	Minimum High Level Input Voltage	A(n), T/ $\overline{R}$ , $\overline{OE}$	3.6 2.7	5.0 5.0		2.0 2.0	2.0 2.0	V	V <sub>OUT</sub> ≤ 0.1V or ≥ V <sub>CC</sub> − 0.1V						
V <sub>IHB</sub>		B(n)	3.3 3.3	4.5 5.5		2.0 2.0	2.0 2.0								
V <sub>ILA</sub>	Maximum Low Level Input Voltage	A(n), T/ $\overline{R}$ , $\overline{OE}$	3.6 2.7	5.0 5.0		0.8 0.8	0.8 0.8	V	V <sub>OUT</sub> ≤ 0.1V or ≥ V <sub>CC</sub> − 0.1V						
V <sub>ILB</sub>		B(n)	3.3 3.3	4.5 5.5		0.8 0.8	0.8 0.8								
V <sub>OHA</sub>	Minimum High Level Output Voltage		3.0 3.0 2.7 2.7	4.5 4.5 4.5 4.5	2.99 2.65 2.5 2.3	2.9 2.35 2.3 2.1	2.9 2.25 2.2 2.0	V	I <sub>OUT</sub> = −100 μA I <sub>OH</sub> = −24 mA I <sub>OH</sub> = −12 mA I <sub>OH</sub> = −24 mA						
V <sub>OHB</sub>			3.0 3.0	4.5 4.5	4.5 4.25	4.4 3.86	4.4 3.76			V	I <sub>OUT</sub> = −100 μA I <sub>OH</sub> = −24 mA				
			V <sub>OLA</sub>	Maximum Low Level Output Voltage		3.0 3.0 2.7 2.7	4.5 4.5 4.5 4.5					0.002 0.21 0.11 0.22	0.1 0.36 0.36 0.42	V	I <sub>OUT</sub> = 100 μA I <sub>OL</sub> = 24 mA I <sub>OL</sub> = 12 mA I <sub>OL</sub> = 24 mA
						V <sub>OLB</sub>	3.0 3.0					4.5 4.5	0.002 0.18		
I <sub>IN</sub>	Maximum Input Leakage Current @ $\overline{OE}$ , T/ $\overline{R}$		3.6	5.5		±0.1	±1.0	μA	V <sub>I</sub> = V <sub>CCB</sub> , GND						
I <sub>OZA</sub>	Maximum TRI-STATE Output Leakage @ A(n)		3.6	5.5		±0.5	±5.0	μA	V <sub>I</sub> = V <sub>IL</sub> , V <sub>IH</sub> $\overline{OE}$ = V <sub>CCA</sub> V <sub>O</sub> = V <sub>CCA</sub> , GND						

Symbol	Parameter		V <sub>CCA</sub> (V)	V <sub>CCB</sub> (V)	T <sub>A</sub> = +25°C		Units	Conditions
					Typ	Guaranteed Limits		
I <sub>OZB</sub>	Maximum TRI-STATE Output Leakage @ B(n)		3.6	5.5		±0.5    ±5.0	μA	V <sub>I</sub> = V <sub>IL</sub> , V <sub>IH</sub> OE = V <sub>CCA</sub> V <sub>O</sub> = V <sub>CCB</sub> , GND
ΔI <sub>CC</sub>	Maximum I <sub>CC</sub> /Input @ B(n)		3.6	5.5	1.0	1.35    1.5	mA	V <sub>I</sub> = V <sub>CCB</sub> - 2.1V
	A(n), T/ $\bar{R}$ , OE		3.6	5.5		0.35    0.5	mA	V <sub>I</sub> = V <sub>CCA</sub> - 0.6V
I <sub>CCA</sub>	Quiescent V <sub>CCA</sub> Supply Current		3.6	5.5		5    50	μA	A(n) = V <sub>CCA</sub> or GND B(n) = V <sub>CCB</sub> or GND, OE = GND, T/ $\bar{R}$ = GND
I <sub>CCB</sub>	Quiescent V <sub>CCB</sub> Supply Current		3.6	5.5		8    80	μA	A(n) = V <sub>CCA</sub> or GND B(n) = V <sub>CCB</sub> or GND, OE = GND, T/ $\bar{R}$ = V <sub>CCA</sub>
V <sub>OLPA</sub> V <sub>OLPB</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>		3.3 3.3	5.0 5.0		0.8 1.5	V	(Notes 1, 2)
V <sub>OLVA</sub> V <sub>OLVB</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>		3.3 3.3	5.0 5.0		-0.8 -1.2	V	(Notes 1, 2)
V <sub>IHDA</sub> V <sub>IHDB</sub>	Minimum High Level Dynamic Input Voltage		3.3 3.3	5.0 5.0		2.0 2.0	V	(Notes 1, 3)
V <sub>ILDA</sub> V <sub>ILDB</sub>	Maximum Low Level Dynamic Input Voltage		3.3 3.3	5.0 5.0		0.8 0.8	V	(Notes 1, 3)

†Maximum test duration 2.0 ms, one output loaded at a time.

**Note 1:** Worst case package.

**Note 2:** Max number of outputs defined as (n). Data inputs are driven 0V to V<sub>CC</sub> level; one output at GND.

**Note 3:** Max number of Data Inputs (n) switching. (n-1) inputs switching 0V to V<sub>CC</sub> level. Input-under-test switching: V<sub>CC</sub> level to threshold (V<sub>IH</sub>), 0V to threshold (V<sub>IL</sub>), f = 1 MHz.

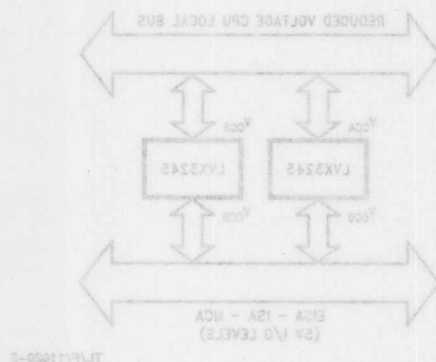
Capacitance	Input Capacitance	Input/Output Capacitance	Power Dissipation	
			A → B	B → A
C <sub>IN</sub>	4.5 pF			
C <sub>IO</sub>		15 pF		
C <sub>PD</sub>			50 pF	40 pF

C<sub>PD</sub> is measured at 10 MHz

## 8-Bit Dual Supply Translating Transceiver

The LVX3245 is a dual supply device capable of bidirectional signal translation. This level shifting ability provides an efficient interface between low voltage CPU local bus with memory and a standard bus defined by 5V I/O levels. The device control inputs can be controlled by either the low voltage CPU and core logic or a bus translator with 5V I/O levels.

Manufactured on a sub-micron CMOS process, the LVX3245 is ideal for mixed voltage applications such as notebook computers using 3.3V CPU's and 5V peripheral devices.



# AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameters	74LVX3245			74LVX3245		74LVX3245		Units
		$T_A = +25^{\circ}\text{C}$ $C_L = 50\text{ pF}$ $**V_{CCA} = 3.3\text{V}$ $*V_{CCB} = 5.0\text{V}$			$T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $C_L = 50\text{ pF}$ $**V_{CCA} = 3.3\text{V}$ $*V_{CCB} = 5.0\text{V}$		$T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $C_L = 50\text{ pF}$ $V_{CCA} = 2.7\text{V}$ $*V_{CCB} = 5.0\text{V}$		
		Min	Typ	Max	Min	Max	Min	Max	
$t_{PHL}$	Propagation Delay A to B	1.0	5.4	8.0	1.0	8.5	1.0	9.0	ns
$t_{PLH}$	Propagation Delay B to A	1.0	5.6	7.5	1.0	8.0	1.0	8.5	ns
$t_{PHL}$	Propagation Delay B to A	1.0	5.1	7.5	1.0	8.0	1.0	8.5	ns
$t_{PLH}$	Propagation Delay A to B	1.0	5.7	7.5	1.0	8.0	1.0	8.5	ns
$t_{PZL}$	Output Enable Time $\overline{OE}$ to B	1.0	4.8	8.0	1.0	8.5	1.0	9.0	ns
$t_{PZH}$	Output Enable Time $\overline{OE}$ to A	1.0	6.3	8.5	1.0	9.0	1.0	9.5	ns
$t_{PZL}$	Output Enable Time $\overline{OE}$ to B	1.0	6.3	8.5	1.0	9.0	1.0	9.5	ns
$t_{PZH}$	Output Enable Time $\overline{OE}$ to A	1.0	6.8	9.0	1.0	9.5	1.0	10.0	ns
$t_{PHZ}$	Output Disable Time $\overline{OE}$ to B	1.0	5.3	7.5	1.0	8.0	1.0	8.5	ns
$t_{PLZ}$	Output Disable Time $\overline{OE}$ to A	1.0	4.2	7.0	1.0	7.5	1.0	8.0	ns
$t_{PHZ}$	Output Disable Time $\overline{OE}$ to B	1.0	5.3	8.0	1.0	8.5	1.0	9.0	ns
$t_{PLZ}$	Output Disable Time $\overline{OE}$ to A	1.0	3.7	6.5	1.0	7.0	1.0	7.5	ns
$t_{OSHL}$	Output to Output Skew***		1.0	1.5		1.5		1.5	ns
$t_{OSLH}$	Data to Output								ns

\*Voltage Range 5.0V is 5.0V  $\pm 0.5\text{V}$ .

\*\*Voltage Range 3.3V is 3.3V  $\pm 0.3\text{V}$ .

\*\*\*Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW ( $t_{OSHL}$ ) or LOW to HIGH ( $t_{OSLH}$ ). Parameter guaranteed by design.

## Capacitance

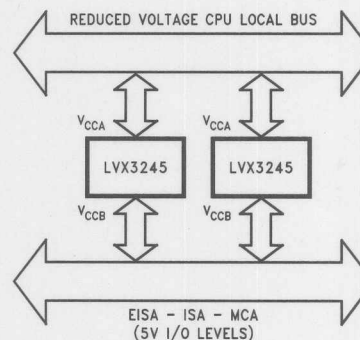
Symbol	Parameter	Typ	Units	Conditions
$C_{IN}$	Input Capacitance	4.5	pF	$V_{CC} = \text{Open}$
$C_{I/O}$	Input/Output Capacitance	15	pF	$V_{CCA} = 3.3\text{V}$ $V_{CCB} = 5.0\text{V}$
$C_{PD}$	Power Dissipation Capacitance	A $\rightarrow$ B	55	pF $V_{CCB} = 5.0\text{V}$ $V_{CCA} = 3.3\text{V}$
		B $\rightarrow$ A	40	

$C_{PD}$  is measured at 10 MHz

## 8-Bit Dual Supply Translating Transceiver

The LVX3245 is a dual supply device capable of bidirectional signal translation. This level shifting ability provides an efficient interface between low voltage CPU local bus with memory and a standard bus defined by 5V I/O levels. The device control inputs can be controlled by either the low voltage CPU and core logic or a bus arbitrator with 5V I/O levels.

Manufactured on a sub-micron CMOS process, the LVX3245 is ideal for mixed voltage applications such as notebook computers using 3.3V CPU's and 5V peripheral devices.



TL/F/11620-3



# 74LVX4245

## 8-Bit Dual Supply Translating Transceiver with TRI-STATE® Outputs

### General Description

The LVX4245 is a dual-supply, 8-bit translating transceiver that is designed to interface between a 5V bus and a 3V bus in a mixed 3V/5V supply environment. The Transmit/Receive (T/R) input determines the direction of data flow. Transmit (active-HIGH) enables data from A ports to B ports; Receive (active-LOW) enables data from B ports to A ports. The Output Enable input, when HIGH, disables both A and B ports by placing them in a HIGH Z condition. The A port interfaces with the 5V bus; the B port interfaces with the 3V bus.

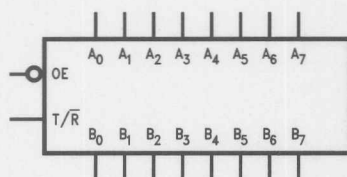
The LVX4245 is suitable for mixed voltage applications such as laptop computers using 3.3V CPU's and 5V LCD displays.

### Features

- Bidirectional interface between 5V and 3V buses
- Control inputs compatible with TTL level
- 5V data flow at A port and 3V data flow at B port
- Outputs source/sink 24 mA at 5V bus; 12 mA at 3V bus
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Available in SOIC and QSOP packages
- Implements patented Quiet Series EMI reduction circuitry
- Functionally compatible with the 74 series 245

**Ordering Code:** See Section 11

### Logic Symbol

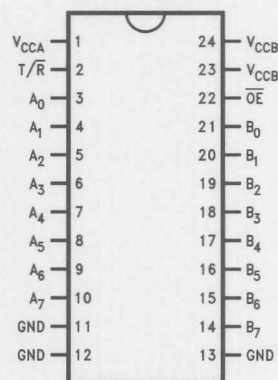


TL/F/11540-1

Pin Names	Description
$\overline{OE}$	Output Enable Input
T/R	Transmit/Receive Input
A <sub>0</sub> –A <sub>7</sub>	Side A Inputs or TRI-STATE Outputs
B <sub>0</sub> –B <sub>7</sub>	Side B Inputs or TRI-STATE Outputs

### Connection Diagram

Pin Assignment for SOIC and QSOP



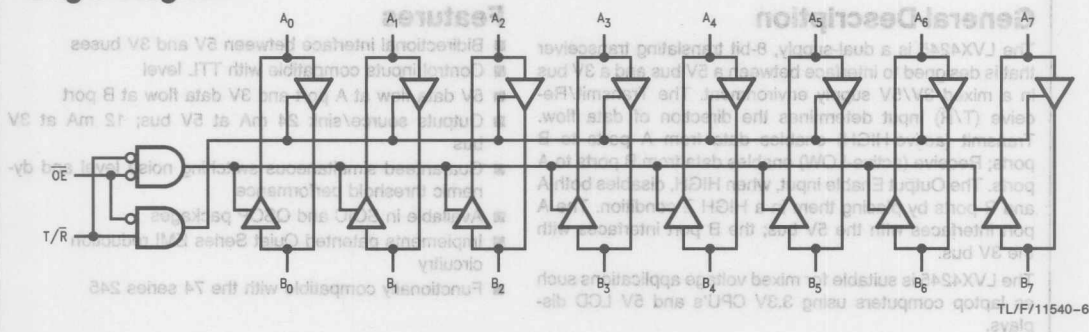
TL/F/11540-2

	SOIC JEDEC	QSOP
Order Number	74LVX4245WM 74LVX4245WMX	74LVX4245QSC 74LVX4245QSCX
See NS Package Number	M24B	MQA24

## Truth Table

Inputs		Outputs
$\overline{OE}$	T/ $\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	HIGH-Z State

## Logic Diagram

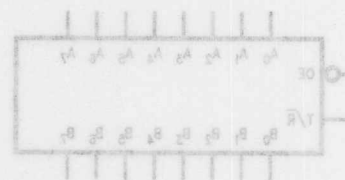


TL/F/11540-6

## Connection Diagram



TL/F/11540-3



TL/F/11540-4

Pin Names	Description
$\overline{OE}$	Output Enable Input
T/ $\overline{R}$	Transmit/Receive Input
A0-A7	Side A Inputs or TRI-STATE Outputs
B0-B7	Side B Inputs or TRI-STATE Outputs

Order Number	See NS Package Number	
	MS-B	QSOIP
74LVX4245WM	74LVX4245WMC	74LVX4245WMC
74LVX4245WMC	74LVX4245WMC	74LVX4245WMC

**Absolute Maximum Ratings** (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CCA}$ , $V_{CCB}$ )	-0.5V to +7.0V
DC Input Voltage ( $V_I$ ) @ $\overline{OE}$ , T/ $\overline{R}$	-0.5V to $V_{CCA}$ + 0.5V
DC Input/Output Voltage ( $V_{I/O}$ ) @ A(n) @ B(n)	-0.5V to $V_{CCA}$ + 0.5V -0.5V to $V_{CCB}$ + 0.5V
DC Input Diode Current ( $I_{IN}$ ) @ $\overline{OE}$ , T/ $\overline{R}$	±20 mA
DC Output Diode Current ( $I_{OK}$ )	±50 mA
DC Output Source or Sink Current ( $I_O$ )	±50 mA
DC $V_{CC}$ or Ground Current per Output Pin ( $I_{CC}$ or $I_{GND}$ ) and Max Current @ $I_{CCA}$ @ $I_{CCB}$	±50 mA ±200 mA ±100 mA
Storage Temperature Range ( $T_{STG}$ )	-65°C to +150°C
DC Latch-Up Source or Sink Current	±300 mA

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Recommended Operating Conditions**

Supply Voltage $V_{CCA}$ $V_{CCB}$	4.5V to 5.5V 2.7V to 3.6V
Input Voltage ( $V_I$ ) @ $\overline{OE}$ , T/ $\overline{R}$	0V to $V_{CCA}$
Input/Output Voltage ( $V_{I/O}$ ) @ A(n) @ B(n)	0V to $V_{CCA}$ 0V to $V_{CCB}$
Free Air Operating Temperature ( $T_A$ )	-40°C to +85°C
Minimum Input Edge Rate ( $\Delta t/\Delta V$ ) $V_{IN}$ from 30% to 70% of $V_{CC}$ $V_{CC}$ @ 3.0V, 4.5V, 5.5V	8 ns/V

**DC Electrical Characteristics**

Symbol	Parameter		V <sub>CCA</sub> (V)	V <sub>CCB</sub> (V)	74LVX4245		(74LVX4245)		Units	Conditions		
					T <sub>A</sub> + 25°C						T <sub>A</sub> = - 40°C to + 85°C	
					Typ		Guaranteed Limits					
V <sub>IHA</sub>	Minimum High Level Input Voltage	A(n), T/ $\overline{R}$ , $\overline{OE}$	5.5 4.5	3.3 3.3	2.0 2.0	2.0 2.0	V	V <sub>OUT</sub> ≤ 0.1V or ≥ V <sub>CC</sub> - 0.1V				
V <sub>IHB</sub>		B(n)	5.0 5.0	3.6 2.7	2.0 2.0	2.0 2.0						
V <sub>ILA</sub>	Maximum Low Level Input Voltage	A(n), T/ $\overline{R}$ , $\overline{OE}$	5.5 4.5	3.3 3.3	0.8 0.8	0.8 0.8	V	V <sub>OUT</sub> ≤ 0.1V or ≥ V <sub>CC</sub> - 0.1V				
V <sub>ILB</sub>		B(n)	5.0 5.0	2.7 3.6	0.8 0.8	0.8 0.8						
V <sub>OHA</sub>	Minimum High Level Output Voltage		4.5 4.5	3.0 3.0	4.5 4.25	4.4 3.86	4.4 3.76	V	I <sub>OUT</sub> = - 100 μA I <sub>OH</sub> = - 24 mA			
V <sub>OHB</sub>			4.5 4.5	3.0 3.0	2.99 2.8	2.9 2.4	2.9 2.4	V	I <sub>OUT</sub> = - 100 μA I <sub>OH</sub> = - 12 mA I <sub>OL</sub> = - 8 mA			
			4.5	2.7	2.5	2.4	2.4					
V <sub>OLA</sub>	Maximum Low Level Output Voltage		4.5 4.5	3.0 3.0	0.002 0.18	0.1 0.36	0.1 0.44	V	I <sub>OUT</sub> = 100 μA I <sub>OL</sub> = 24 mA			
V <sub>OLB</sub>			4.5 4.5	3.0 3.0	0.002 0.1	0.1 0.31	0.1 0.4	V	I <sub>OUT</sub> = 100 μA I <sub>OL</sub> = 12 mA I <sub>OL</sub> = 8 mA			
			4.5	2.7	0.1	0.31	0.4					
I <sub>IN</sub>	Maximum Input Leakage Current @ $\overline{OE}$ , T/ $\overline{R}$		5.5	3.6	±0.1	±1.0	μA	V <sub>I</sub> = V <sub>CCA</sub> , GND				
I <sub>OZA</sub>	Maximum TRI-STATE Output Leakage @ A(n)		5.5	3.6	±0.5	±5.0	μA	V <sub>I</sub> = V <sub>IL</sub> , V <sub>IH</sub> $\overline{OE}$ = V <sub>CCA</sub> V <sub>O</sub> = V <sub>CCA</sub> , GND				

## DC Electrical Characteristics (Continued)

Symbol	Parameter	V <sub>CCA</sub> (V)	V <sub>CCB</sub> (V)	74LVX4245		Units	Conditions	
				T <sub>A</sub> = +25°C				T <sub>A</sub> = -40°C to +85°C
				Typ	Guaranteed Limits			
I <sub>OZB</sub>	Maximum TRI-STATE Output Leakage @ B(n)	5.5	3.6		±0.5	±5.0	μA V <sub>I</sub> = V <sub>IL</sub> , V <sub>IH</sub> OE = V <sub>CCA</sub> V <sub>O</sub> = V <sub>CCB</sub> , GND	
ΔI <sub>CC</sub>	Maximum I <sub>CC</sub> /Input @ A(n), T/Ȧ, OE	5.5	3.6	1.0	1.35	1.5	V <sub>I</sub> = V <sub>CCA</sub> - 2.1V	
	Input @ B(n)	5.5	3.6		0.35	0.5	V <sub>I</sub> = V <sub>CCB</sub> - 0.6V	
I <sub>CCA</sub>	Quiescent V <sub>CCA</sub> Supply Current	5.5	3.6		8	80	μA A(n) = V <sub>CCA</sub> or GND B(n) = V <sub>CCB</sub> or GND, OE = GND T/Ȧ = GND	
I <sub>CCB</sub>	Quiescent V <sub>CCB</sub> Supply Current	5.5	3.6		5	50	μA A(n) = V <sub>CCA</sub> or GND B(n) = V <sub>CCB</sub> or GND, OE = GND T/Ȧ = V <sub>CCA</sub>	
V <sub>OLPA</sub> V <sub>OLPB</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	5.0 5.0	3.3 3.3		1.5 0.8		V (Notes 1, 2)	
V <sub>OLVA</sub> V <sub>OLVB</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	5.0 5.0	3.3 3.3		-1.2 -0.8		V (Notes 1, 2)	
V <sub>IHDA</sub> V <sub>IHDB</sub>	Minimum High Level Dynamic Input Voltage	5.0 5.0	3.3 3.3		2.0 2.0		V (Notes 1, 3)	
V <sub>ILDA</sub> V <sub>ILDB</sub>	Maximum Low Level Dynamic Input Voltage	5.0 5.0	3.3 3.3		0.8 0.8		V (Notes 1, 3)	

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: Worst case package.

Note 2: Max number of outputs defined as (n). Data inputs are driven 0V to V<sub>CC</sub> level; one output at GND.Note 3: Max number of Data Inputs (n) switching. (n - 1) inputs switching 0V to V<sub>CC</sub> level. Input-under-test switching: V<sub>CC</sub> level to threshold (V<sub>IHD</sub>), 0V to threshold (V<sub>ILD</sub>), f = 1 MHz.

V <sub>IH</sub>	V	5.0	5.0	5.0	5.0	5.0	High Level Input Voltage	V <sub>IH</sub>
		5.0	5.0	5.0	5.0	5.0	Input Voltage	
V <sub>IL</sub>	V	0.8	0.8	0.8	0.8	0.8	Maximum Low Level Input Voltage	V <sub>IL</sub>
		0.8	0.8	0.8	0.8	0.8	Input Voltage	
V <sub>OH</sub>	V	4.4	4.4	4.4	4.4	4.4	Minimum High Level Output Voltage	V <sub>OH</sub>
		4.4	4.4	4.4	4.4	4.4	Output Voltage	
V <sub>OL</sub>	V	0.2	0.2	0.2	0.2	0.2	Maximum Low Level Output Voltage	V <sub>OL</sub>
		0.2	0.2	0.2	0.2	0.2	Output Voltage	
I <sub>IL</sub>	A <sub>n</sub>	±1.0	±1.0	±1.0	±1.0	±1.0	Maximum Input Leakage Current @ OE, T/R	I <sub>IL</sub>
		±1.0	±1.0	±1.0	±1.0	±1.0	Input Leakage	
I <sub>OZ</sub>	A <sub>n</sub>	±5.0	±5.0	±5.0	±5.0	±5.0	Maximum TRI-STATE Output Leakage @ A(n)	I <sub>OZ</sub>
		±5.0	±5.0	±5.0	±5.0	±5.0	Output Leakage	

**AC Electrical Characteristics:** See Section 2 for Test Methodology

Symbol	Parameters	74LVX4245			74LVX4245		74LVX4245		Units
		$T_A = +25^{\circ}\text{C}$ $C_L = 50\text{ pF}$ $V_{CCA} = 5\text{V}$ $V_{CCB} = 3.3\text{V}$			$T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $C_L = 50\text{ pF}$ $V_{CCA} = 5\text{V}$ $V_{CCB} = 3.3\text{V}$		$T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $C_L = 50\text{ pF}$ $V_{CCA} = 5\text{V}$ $V_{CCB} = 2.7\text{V}$		
		Min	Typ	Max	Min	Max	Min	Max	
$t_{PHL}$	Propagation Delay A to B	1.0	5.1	8.5	1.0	9.0	1.0	10.0	ns
$t_{PLH}$		1.0	5.3	8.5	1.0	9.0	1.0	10.0	
$t_{PHL}$	Propagation Delay B to A	1.0	5.4	8.5	1.0	9.0	1.0	10.0	ns
$t_{PLH}$		1.0	5.5	8.5	1.0	9.0	1.0	10.0	
$t_{PZL}$	Output Enable Time $\overline{OE}$ to B	1.0	6.5	10.0	1.0	10.5	1.0	11.5	ns
$t_{PZH}$		1.0	6.7	10.0	1.0	10.5	1.0	11.5	
$t_{PZL}$	Output Enable Time $\overline{OE}$ to A	1.0	5.2	9.0	1.0	9.5	1.0	10.0	ns
$t_{PZH}$		1.0	5.8	9.0	1.0	9.5	1.0	10.0	
$t_{PHZ}$	Output Disable Time $\overline{OE}$ to B	1.0	6.0	9.5	1.0	10.0	1.0	10.0	ns
$t_{PLZ}$		1.0	3.3	6.5	1.0	7.0	1.0	7.5	
$t_{PHZ}$	Output Disable Time $\overline{OE}$ to A	1.0	3.9	7.0	1.0	7.5	1.0	7.5	ns
$t_{PLZ}$		1.0	2.9	6.5	1.0	7.0	1.0	7.5	
$t_{OSHL}$	Output to Output Skew***		1.0	1.5		1.5		1.5	ns
$t_{OSLH}$	Data to Output								

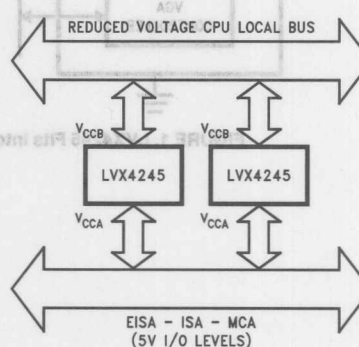
\*Voltage Range 5.0V is 5.0V  $\pm 0.5\text{V}$ .\*\*Voltage Range 3.3V is 3.3V  $\pm 0.3\text{V}$ .\*\*\*Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW ( $t_{OSHL}$ ) or LOW to HIGH ( $t_{OSLH}$ ). Parameter guaranteed by design.**Capacitance**

Symbol	Parameter	Typ	Units	Conditions
$C_{IN}$	Input Capacitance	4.5	pF	$V_{CC} = \text{Open}$
$C_{I/O}$	Input/Output Capacitance	15	pF	$V_{CCA} = 5.0\text{V}$ $V_{CCB} = 3.3\text{V}$
$C_{PD}$	Power Dissipation Capacitance	B $\rightarrow$ A	55	pF
		A $\rightarrow$ B	40	pF

 $C_{PD}$  is measured at 10 MHz**8-Bit Dual Supply Translating Transceiver**

The LVX4245 is a dual supply device capable of bidirectional signal translation. This level shifting ability provides an efficient interface between low voltage CPU local bus with memory and a standard bus defined by 5V I/O levels. The device control inputs can be controlled by either the low voltage CPU and core logic or a bus arbitrator with 5V I/O levels.

Manufactured on a sub-micron CMOS process, the LVX4245 is ideal for mixed voltage applications such as notebook computers using 3.3V CPU's and 5V peripheral devices.



TL/F/11540-3

applied VCC. If an I/O pin of 3V ICs is driven by 5V ICs, the P-Channel transistor in 3V ICs will conduct causing current flow from I/O bus to the 3V power supply. The resulting high current flow can cause destruction of 3V ICs through latch-up effects. To prevent this problem, a current limiting resistor is used typically under direct connection of 3V ICs and 5V ICs, but it causes speed degradation.

In a better solution, the LVX4245 configures two different output levels to handle the dual supply interface issues. The "A" port is a dedicated 5V port to interface 5V ICs. The "B" port is a dedicated port to interface 3V ICs. Figure 1 shows how LVX4245 fits into a system with 3V subsystem and 5V subsystem.

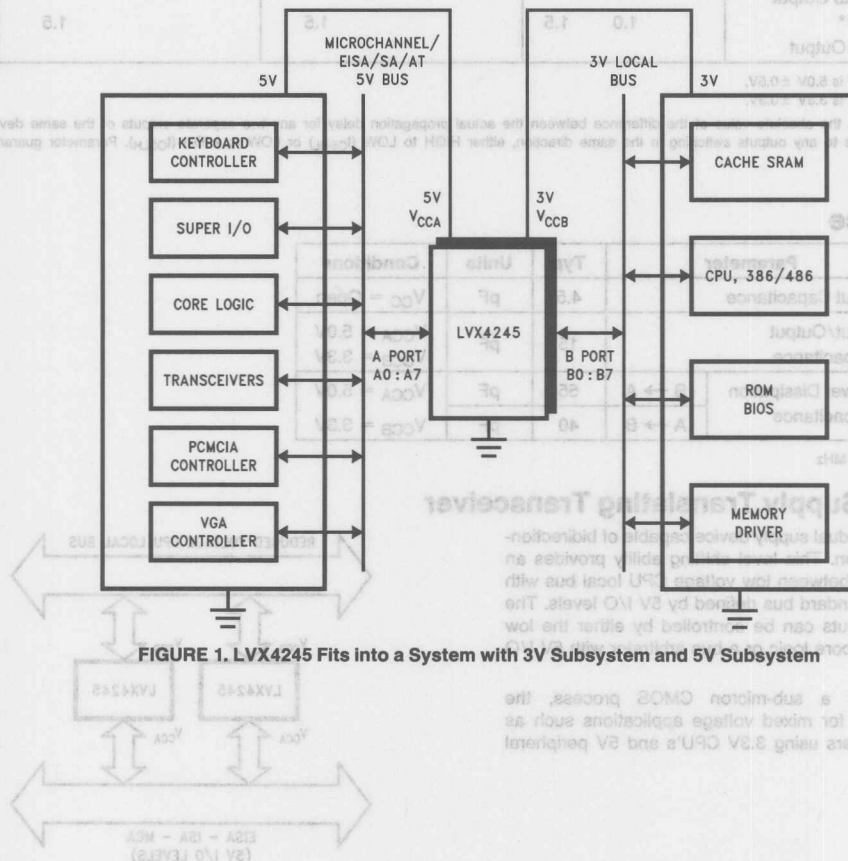


FIGURE 1. LVX4245 Fits into a System with 3V Subsystem and 5V Subsystem

select either bidirectional or unidirectional modes. Since the center 20 pins are also pin compatible to 74 series 245, as shown in Figure 2, the designer could use this device in either a 3V system or a 5V system without any further work to re-layout the board.

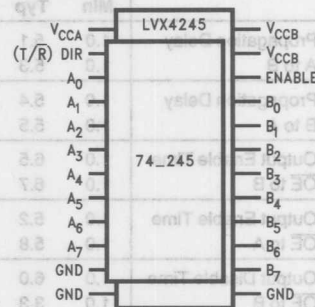


FIGURE 2. LVX4245 Pin Arrangement is Compatible to 20-Pin 74 Series 245

## 74LVXC3245

# 8-Bit Dual Supply Configurable Voltage Interface Transceiver with TRI-STATE® Outputs for 3V System

### General Description

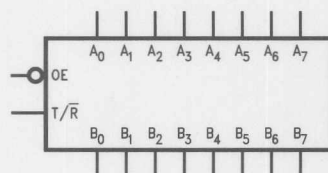
The LVXC3245 is a 24-pin dual-supply, 8-bit configurable voltage interface transceiver suited for PCMCIA and other real time configurable I/O applications. The  $V_{CCA}$  pin accepts a 3V supply level. The A port is a dedicated 3V port. The  $V_{CCB}$  pin accepts a 3V-to-5V supply level. The B port is configured to track the  $V_{CCB}$  supply level respectively. A 5V level on the  $V_{CC}$  pin will configure the I/O pins at a 5V level and a 3V  $V_{CC}$  will configure the I/O pins at a 3V level. The A port should interface with a 3V host system and the B port to the card slots. This device will allow the  $V_{CCB}$  voltage source pin and I/O pins on the B port to float when  $\overline{OE}$  is HIGH. This feature is necessary to buffer data to and from a PCMCIA socket that permits PCMCIA cards to be inserted and removed during normal operation.

### Features

- Bidirectional interface between 3V and 3V-to-5V buses
- Control inputs compatible with TTL level
- Outputs source/sink up to 24 mA
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Available in SOIC and QSOP packages
- Implements patented Quiet Series EMI reduction circuitry
- Flexible  $V_{CCB}$  operating range
- Allows B port and  $V_{CCB}$  to float simultaneously when  $\overline{OE}$  is HIGH
- Functionally compatible with the 74 series 245

**Ordering Code:** See Section 11

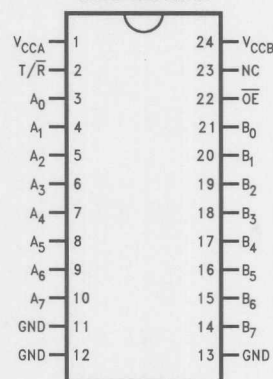
### Logic Symbol



TL/F/12008-1

### Connection Diagram

Pin Assignment for SOIC and QSOP



TL/F/12008-2

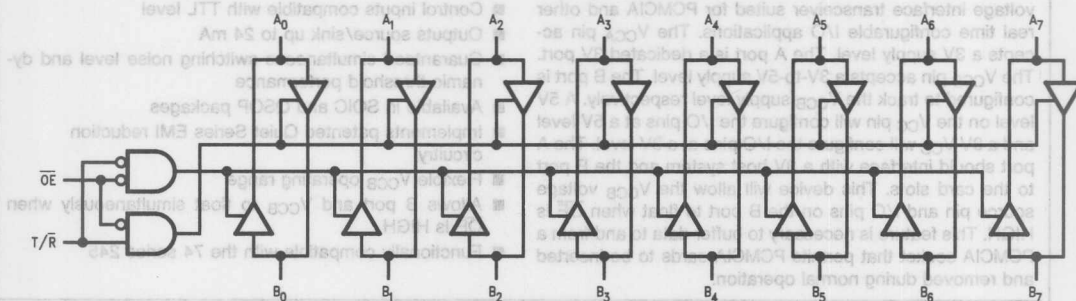
Pin Names	Description
$\overline{OE}$	Output Enable Input
T/ $\overline{R}$	Transmit/Receive Input
A <sub>0</sub> –A <sub>7</sub>	Side A Inputs or TRI-STATE Outputs
B <sub>0</sub> –B <sub>7</sub>	Side B Inputs or TRI-STATE Outputs

	SOIC JEDEC	QSOP
Order Number	74LVXC3245WM 74LVXC3245WMX	74LVXC3245QSC 74LVXC3245QSCX
See NS Package Number	M24B	MQA24

# Truth Table

Inputs		Outputs
OE	T/R	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	HIGH-Z State

## Logic Diagram



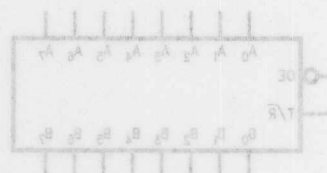
TL/F/12008-4

## Connection Diagram



TL/F/12008-5

## Logic Symbol



TL/F/12008-1

Pin Name	Description
OE	Output Enable Input
T/R	Transmit/Receive Input
A <sub>0</sub> -A <sub>7</sub>	Side A Inputs or TRI-STATE Outputs
B <sub>0</sub> -B <sub>7</sub>	Side B Inputs or TRI-STATE Outputs

Order Number	SOIC JEDEC	QSOIP
	74LVXC3245WM	74LVXC3245SC
See NS Package Number	M24B	M24A
	74LVXC3245MX	74LVXC3245CX

**Absolute Maximum Ratings** (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CCA}, V_{CCB}$ )	-0.5V to +7.0V
DC Input Voltage ( $V_I$ ) @ $\overline{OE}$ , T/ $\overline{R}$	-0.5V to $V_{CCA} + 0.5V$
DC Input/Output Voltage ( $V_{I/O}$ ) @ $A_n$ @ $B_n$	-0.5V to $V_{CCA} + 0.5V$ -0.5V to $V_{CCB} + 0.5V$
DC Input Diode Curr. ( $I_{IK}$ ) @ $\overline{OE}$ , T/ $\overline{R}$	$\pm 20$ mA
DC Output Diode Current ( $I_{OK}$ )	$\pm 50$ mA
DC Output Source or Sink Current ( $I_O$ )	$\pm 50$ mA
DC $V_{CC}$ or Ground Current per Output Pin ( $I_{CC}$ or $I_{GND}$ ) and Max Current	$\pm 50$ mA $\pm 200$ mA
Storage Temperature Range ( $T_{STG}$ )	-65°C to +150°C
DC Latch-Up Source or Sink Current	$\pm 300$ mA

**Recommended Operating Conditions**

Supply Voltage $V_{CCA}$	2.7V to 3.6V ( $V_{CCA} \leq V_{CCB}$ )
$V_{CCB}$	3.0V to 5.5V
Input Voltage ( $V_I$ ) @ $\overline{OE}$ , T/ $\overline{R}$	0V to $V_{CCA}$
Input Output Voltage ( $V_{I/O}$ ) @ $A_n$ @ $B_n$	0V to $V_{CCA}$ 0V to $V_{CCB}$
Free Air Operating Temperature ( $T_A$ )	-40°C to +85°C
Minimum Input Edge Rate ( $\Delta V/\Delta t$ ) $V_{IN}$ from 30% to 70% of $V_{CC}$ $V_{CC}$ @ 3.0V, 4.5V, 5.5V	8 ns/V

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**DC Electrical Characteristics**

Symbol	Parameter		V <sub>CCA</sub> (V)	V <sub>CCB</sub> (V)	74LVXC3245		74LVXC3245		Units	Conditions
					T <sub>A</sub> = 25°C		T <sub>A</sub> = -40°C to +85°C			
					Typ	Guaranteed Limits				
V <sub>IHA</sub>	Minimum High Level Input Voltage	A <sub>n</sub>	2.7	3.0		2.0	2.0	V	V <sub>OUT</sub> ≤ 0.1V or ≥ V <sub>CC</sub> - 0.1V	
		OE	3.0	3.6		2.0	2.0			
		T/ $\overline{R}$	3.6	5.5		2.0	2.0			
V <sub>IHB</sub>		B <sub>n</sub>	2.7	3.0		2.0	2.0	V	V <sub>OUT</sub> ≤ 0.1V or ≥ V <sub>CC</sub> - 0.1V	
			3.0	3.6		2.0	2.0			
			3.6	5.5		3.85	3.85			
V <sub>ILA</sub>	Maximum Low Level Input Voltage	A <sub>n</sub>	2.7	3.0		0.8	0.8	V	V <sub>OUT</sub> ≤ 0.1V or ≥ V <sub>CC</sub> - 0.1V	
		OE	3.0	3.6		0.8	0.8			
		T/ $\overline{R}$	3.6	5.5		0.8	0.8			
V <sub>ILB</sub>		B <sub>n</sub>	2.7	3.0		0.8	0.8	V	V <sub>OUT</sub> ≤ 0.1V or ≥ V <sub>CC</sub> - 0.1V	
			3.0	3.6		0.8	0.8			
			3.6	5.5		1.65	1.65			
V <sub>OHA</sub>	Minimum High Level Output Voltage		3.0	3.0	2.99	2.9	2.9	V	I <sub>OUT</sub> = -100 μA I <sub>OH</sub> = -12 mA I <sub>OH</sub> = -24 mA I <sub>OH</sub> = -12 mA I <sub>OH</sub> = -24 mA	
			3.0	3.0	2.85	2.56	2.46			
			3.0	3.0	2.65	2.35	2.25			
			2.7	3.0	2.5	2.3	2.2			
			2.7	4.5	2.3	2.1	2.0			
V <sub>OHB</sub>			3.0	3.0	2.99	2.9	2.9	V	I <sub>OUT</sub> = -100 μA I <sub>OH</sub> = -12 mA I <sub>OH</sub> = -24 mA I <sub>OH</sub> = -12 mA I <sub>OH</sub> = -24 mA	
			3.0	3.0	2.85	2.56	2.46			
			3.0	3.0	2.65	2.35	2.25			
			3.0	3.0	2.65	2.35	2.25			
			3.0	4.5	4.25	3.86	3.76			
V <sub>OLA</sub>	Maximum Low Level Output Voltage		3.0	3.0	0.002	0.1	0.1	V	I <sub>OUT</sub> = 100 μA I <sub>OL</sub> = 24 mA I <sub>OL</sub> = 12 mA I <sub>OL</sub> = 24 mA	
			3.0	3.0	0.21	0.36	0.44			
			2.7	3.0	0.11	0.36	0.44			
			2.7	4.5	0.22	0.42	0.5			
V <sub>OLB</sub>			3.0	3.0	0.002	0.1	0.1	V	I <sub>OUT</sub> = 100 μA I <sub>OL</sub> = 24 mA I <sub>OL</sub> = 24 mA	
			3.0	3.0	0.21	0.36	0.44			
			3.0	4.5	0.18	0.36	0.44			

## DC Electrical Characteristics (Continued)

Symbol	Parameter	V <sub>CCA</sub> (V)	V <sub>CCB</sub> (V)	74LVXC3245		74LVXC3245		Units	Conditions
				T <sub>A</sub> = +25°C		T <sub>A</sub> = -40°C to +85°C			
				Typ	Guaranteed Limits				
I <sub>IN</sub>	Maximum Input Leakage Current @ OE, T/Ṛ	3.6 3.6	3.6 5.5		±0.1 ±0.1	±1.0 ±1.0	μA	V <sub>I</sub> = V <sub>CCA</sub> , GND	
I <sub>OZA</sub>	Maximum TRI-STATE Output Leakage @ A <sub>n</sub>	3.6 3.6	3.6 5.5		±0.5 ±0.5	±5.0 ±5.0	μA	V <sub>I</sub> = V <sub>IL</sub> , V <sub>IH</sub> , OE = V <sub>CCA</sub> , V <sub>O</sub> = V <sub>CCA</sub> , GND	
I <sub>OZB</sub>	Maximum TRI-STATE Output Leakage @ B <sub>n</sub>	3.6 3.6	3.6 5.5		±0.5 ±0.5	±5.0 ±5.0	μA	V <sub>I</sub> = V <sub>IL</sub> , V <sub>IH</sub> , OE = V <sub>CCA</sub> , V <sub>O</sub> = V <sub>CCB</sub> , GND	
ΔI <sub>CC</sub>	Maximum I <sub>CC</sub> /Input	B <sub>n</sub>	3.6	5.5	1.0	1.35	1.5	mA	V <sub>I</sub> = V <sub>CCB</sub> -2.1V
		All Inputs	3.6	3.6		0.35	0.5		V <sub>I</sub> = V <sub>CC</sub> -0.6V
I <sub>CCA1</sub>	Quiescent V <sub>CCA</sub> Supply Current as B Port Floats		3.6	Open		5	50	μA	A <sub>n</sub> = V <sub>CCA</sub> or GND B <sub>n</sub> = Open, OE = V <sub>CCA</sub> , T/Ṛ = V <sub>CCA</sub> , V <sub>CCB</sub> = Open
I <sub>CCA2</sub>	Quiescent V <sub>CCA</sub> Supply Current		3.6 3.6	3.6 5.5		5 5	50 50	μA	A <sub>n</sub> = V <sub>CCA</sub> or GND, B <sub>n</sub> = V <sub>CCB</sub> or GND, OE = GND, T/Ṛ = GND
I <sub>CCB</sub>	Quiescent V <sub>CCB</sub> Supply Current		3.6 3.6	3.6 5.5		5 8	50 80	μA	A <sub>n</sub> = V <sub>CCA</sub> or GND, B <sub>n</sub> = V <sub>CCB</sub> or GND, OE = GND, T/Ṛ = V <sub>CCA</sub>
V <sub>OLPA</sub>	Quiet Output		3.3 3.3	3.3 5.0		0.8 0.8		V	(Notes 1, 2)
V <sub>OLPB</sub>	V <sub>OL</sub>		3.3 3.3	3.3 5.0		0.8 1.5		V	(Notes 1, 2)
V <sub>OLVA</sub>	Quiet Output		3.3 3.3	3.3 5.0		-0.8 -0.8		V	(Notes 1, 2)
V <sub>OLVB</sub>	V <sub>OL</sub>		3.3 3.3	3.3 5.0		-0.8 -1.2		V	(Notes 1, 2)
V <sub>IHDA</sub>	Minimum High Level Dynamic		3.3 3.3	3.3 5.0		2.0 2.0		V	(Notes 1, 3)
V <sub>IHDB</sub>	Input Voltage		3.3 3.3	3.3 5.0		2.0 3.5		V	(Notes 1, 3)
V <sub>ILDA</sub>	Maximum Low Level Dynamic		3.3 3.3	3.3 5.0		0.8 0.8		V	(Notes 1, 3)
V <sub>ILDB</sub>	Input Voltage		3.3 3.3	3.3 5.0		0.8 1.5		V	(Notes 1, 3)
<b>Note 1:</b> Worst case package.									
<b>Note 2:</b> Max number of outputs defined as (n). Data inputs are driven 0V to V <sub>CC</sub> level; one output at GND.									
<b>Note 3:</b> Max number of Data Inputs (n) switching. (n-1) inputs switching 0V to V <sub>CC</sub> level. Input-under-test switching: V <sub>CC</sub> level to threshold (V <sub>IHD</sub> ), 0V to threshold (V <sub>ILD</sub> ). f = 1 MHz.									

**AC Electrical Characteristics:** See Section 2 for Test Methodology

Symbol	Parameter	74LVXC3245			74LVXC3245		74LVXC3245			74LVXC3245		Units
		T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF V <sub>CCA</sub> = 2.7V–3.6V V <sub>CCB</sub> = 4.5V–5.5V			T <sub>A</sub> = –40°C to +85°C C <sub>L</sub> = 50 pF V <sub>CCA</sub> = 2.7V–3.6V V <sub>CCB</sub> = 4.5V–5.5V		T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF V <sub>CCA</sub> = 2.7V–3.6V V <sub>CCB</sub> = 3.0V–3.6V			T <sub>A</sub> = –40°C to +85°C C <sub>L</sub> = 50 pF V <sub>CCA</sub> = 2.7V–3.6V V <sub>CCB</sub> = 3.0V–3.6V		
		Min	Typ (Note 1)	Max	Min	Max	Min	Typ (Note 2)	Max	Min	Max	
t <sub>PHL</sub>	Propagation Delay	1.0	4.8	8.0	1.0	8.5	1.0	5.5	8.5	1.0	9.0	ns
t <sub>PLH</sub>	A to B	1.0	3.9	6.5	1.0	7.0	1.0	5.2	8.0	1.0	8.5	
t <sub>PHL</sub>	Propagation Delay	1.0	3.8	6.5	1.0	7.0	1.0	4.4	7.0	1.0	7.5	ns
t <sub>PLH</sub>	B to A	1.0	4.3	7.5	1.0	8.0	1.0	5.1	7.5	1.0	8.0	
t <sub>PZL</sub>	Output Enable Time	1.0	4.7	8.0	1.0	8.5	1.0	6.0	9.0	1.0	9.5	ns
t <sub>PZH</sub>	OE to B	1.0	4.8	8.5	1.0	9.0	1.0	6.1	9.5	1.0	10.0	
t <sub>PZL</sub>	Output Enable Time	1.0	5.9	9.5	1.0	10.0	1.0	6.4	10.0	1.0	10.5	ns
t <sub>PZH</sub>	OE to A	1.0	5.4	9.0	1.0	9.5	1.0	5.8	9.0	1.0	9.5	
t <sub>PHZ</sub>	Output Disable Time	1.0	4.0	8.0	1.0	8.5	1.0	6.3	9.5	1.0	10.0	ns
t <sub>PLZ</sub>	OE to B	1.0	3.8	7.5	1.0	8.0	1.0	4.5	8.0	1.0	8.5	
t <sub>PHZ</sub>	Output Disable Time	1.0	4.6	9.5	1.0	10.0	1.0	5.2	9.5	1.0	10.0	ns
t <sub>PLZ</sub>	OE to A	1.0	3.1	6.5	1.0	7.0	1.0	3.4	6.5	1.0	7.0	
t <sub>OSSL</sub>	Output to Output											ns
t <sub>OSLH</sub>	Skew* Data to Output		1.0	1.5		1.5		1.0	1.5		1.5	

Note 1: Typical values at V<sub>CCA</sub> = 3.3V, V<sub>CCB</sub> = 5.0V @ 25°C.

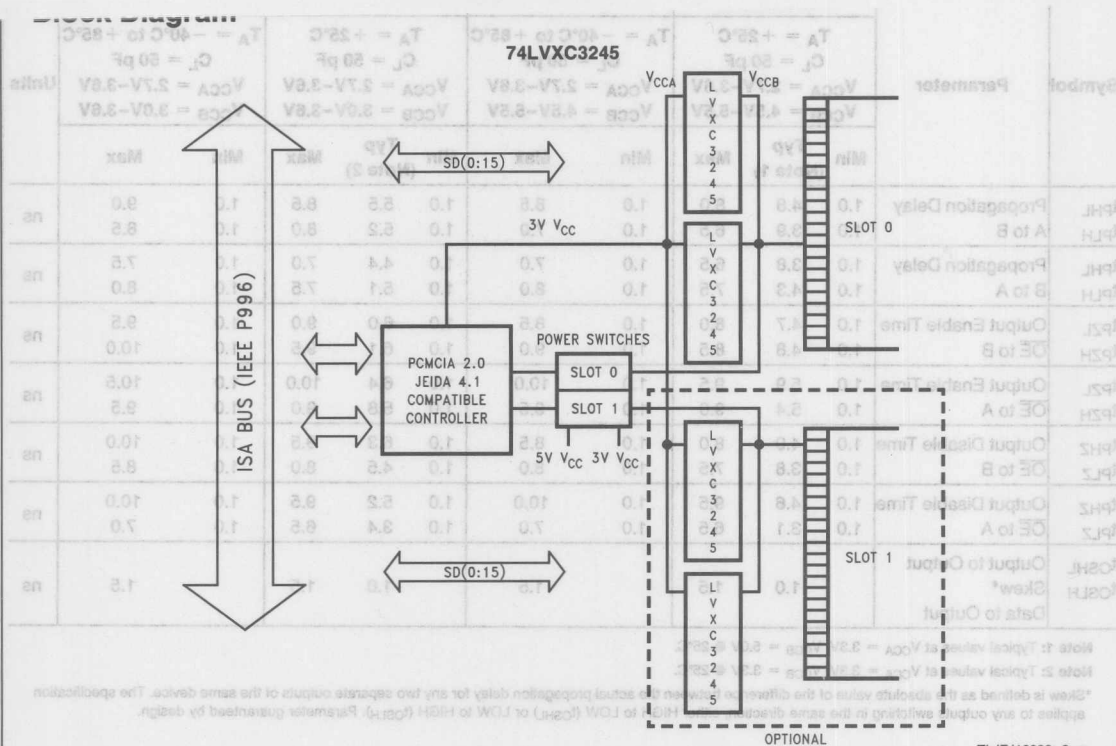
Note 2: Typical values at V<sub>CCA</sub> = 3.3V, V<sub>CCB</sub> = 3.3V @ 25°C.

\*Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t<sub>OSSL</sub>) or LOW to HIGH (t<sub>OSLH</sub>). Parameter guaranteed by design.

**Capacitance**

Symbol	Parameter	Typ	Units	Conditions	
C <sub>IN</sub>	Input Capacitance	4.5	pF	V <sub>CC</sub> = Open	
C <sub>I/O</sub>	Input/Output Capacitance	10	pF	V <sub>CCA</sub> = 3.3V V <sub>CCB</sub> = 5.0V	
C <sub>PD</sub>	Power Dissipation Capacitance	A → B	50	pF	V <sub>CCB</sub> = 5.0V
		B → A	40	pF	V <sub>CCA</sub> = 3.3V

C<sub>PD</sub> is measured at 10 MHz.



The LVXC3245 is a 24-pin dual supply device well suited for PCMCIA configurable I/O applications. Ideal for low power notebook designs, the LVXC3245 consumes less than 1 mW of quiescent power in all modes of operation. The LVXC3245 meets all PCMCIA I/O voltage requirements at 5V and 3.3V operation. By tying  $V_{CCB}$  of the LVXC3245 to the card voltage supply, the PCMCIA card will always experience rail to rail output swings, maximizing the reliability of the interface.

The  $V_{CCA}$  pin on the LVXC3245 must always be tied to a 3V power supply. This voltage connection provides internal references needed to account for variations in  $V_{CCB}$ . When connected as in the figure above, the LVXC3245 meets all the voltage and current requirements of the ISA bus standard (IEEE P996).

## 74LVXC4245

### 8-Bit Dual Supply Configurable Voltage Interface Transceiver with TRI-STATE® Outputs

#### General Description

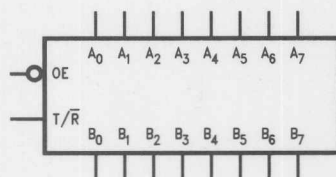
The LVXC4245 is a 24-pin dual-supply, 8-bit configurable voltage interface transceiver suited for PCMCIA and other real time configurable I/O applications. The  $V_{CCA}$  pin accepts a 5V supply level. The "A" port is a dedicated 5V port. The  $V_{CCB}$  pin accepts a 3V-to-5V supply level. The "B" port is configured to track the  $V_{CCB}$  supply level respectively. A 5V level on the  $V_{CC}$  pin will configure the I/O pins at a 5V level and a 3V  $V_{CC}$  will configure the I/O pins at a 3V level. This device will allow the  $V_{CCB}$  voltage source pin and I/O pins on the "B" port to float when  $\overline{OE}$  is HIGH. This feature is necessary to buffer data to and from a PCMCIA socket that permits PCMCIA cards to be inserted and removed during normal operation.

#### Features

- Bidirectional interface between 5V and 3V-to-5V buses
- Control inputs compatible with TTL level
- Outputs source/sink up to 24 mA
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Available in SOIC and QSOP packages
- Implements patented Quiet Series EMI reduction circuitry
- Flexible  $V_{CCB}$  operating range
- Allows B port and  $V_{CCB}$  to float simultaneously when  $\overline{OE}$  is HIGH
- Functionally compatible with the 74 series 245

**Ordering Code:** See Section 11

#### Logic Symbol

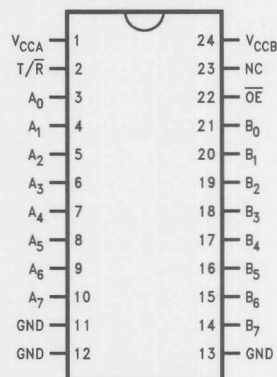


TL/F/12009-1

Pin Names	Description
$\overline{OE}$	Output Enable Input
$T/\overline{R}$	Transmit/Receive Input
$A_0$ - $A_7$	Side A Inputs or TRI-STATE Outputs
$B_0$ - $B_7$	Side B Inputs or TRI-STATE Outputs

#### Connection Diagram

Pin Assignment  
for SOIC and QSOP



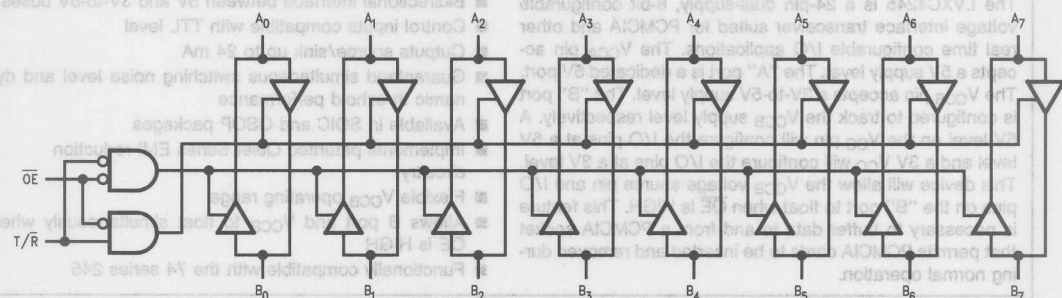
TL/F/12009-2

	SOIC JEDEC	QSOP
Order Number	74LVXC4245WM 74LVXC4245WMX	74LVXC4245QSC 74LVXC4245QSCX
See NS Package Number	M24B	MQA24

# Truth Table

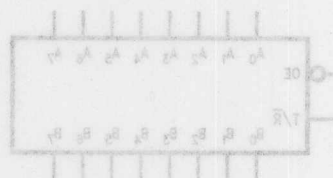
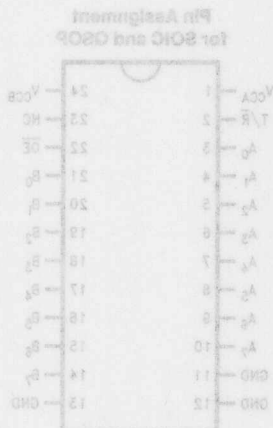
Inputs		Outputs
$\overline{OE}$	$T/\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	HIGH-Z State

# Logic Diagram



TL/F/12009-4

# Connection Diagram



TL/F/12009-1

Pin Names	Description
$\overline{OE}$	Output Enable Input
$T/\overline{R}$	Transmit/Receive Input
$A_0-A_7$	Side A Inputs or TRI-STATE Outputs
$B_0-B_7$	Side B Inputs or TRI-STATE Outputs

Order Number	SOIC JEDEC	QSO
7ALVXC4245WM	7ALVXC4245WMX	7ALVXC4245QSC
7ALVXC4245WMX	7ALVXC4245QSCX	MOA24

**Absolute Maximum Ratings** (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CCA}, V_{CCB}$ )	-0.5V to +7.0V
DC Input Voltage ( $V_I$ ) @ $\overline{OE}$ , T/ $\overline{R}$	-0.5V to $V_{CCA} + 0.5V$
DC Input/Output Voltage ( $V_{I/O}$ )	
@ $A_n$	-0.5V to $V_{CCA} + 0.5V$
@ $B_n$	-0.5V to $V_{CCB} + 0.5V$
DC Input Diode Current ( $I_{IK}$ ) @ $\overline{OE}$ , T/ $\overline{R}$	$\pm 20$ mA
DC Output Diode Current ( $I_{OK}$ )	$\pm 50$ mA
DC Output Source or Sink Current ( $I_O$ )	$\pm 50$ mA
DC $V_{CC}$ or Ground Current	
Per Output Pin ( $I_{CC}$ or $I_{GND}$ )	$\pm 50$ mA
and Max Current	$\pm 200$ mA
Storage Temperature Range ( $T_{STG}$ )	-65°C to +150°C
DC Latch-Up Source or Sink Current	$\pm 300$ mA

**Recommended Operating Conditions**

Supply Voltage	$V_{CCA}$	4.5V to 5.5V
	$V_{CCB}$	2.7V to 5.5V
Input Voltage ( $V_I$ ) @ $\overline{OE}$ , T/ $\overline{R}$		0V to $V_{CCA}$
Input/Output Voltage ( $V_{I/O}$ )		
@ $A_n$		0V to $V_{CCA}$
@ $B_n$		0V to $V_{CCB}$
Free Air Operating Temperature ( $T_A$ )		-40°C to +85°C
Minimum Input Edge Rate ( $\Delta V/\Delta t$ )		8 ns/V
	$V_{IN}$ from 30% to 70% of $V_{CC}$	
	$V_{CC}$ @ 3V, 4.5V, 5.5V	

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**DC Electrical Characteristics**

Symbol	Parameter		$V_{CCA}$ (V)	$V_{CCB}$ (V)	74LVXC4245		Units	Conditions
					$T_A = +25^\circ\text{C}$	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		
					Typ	Guaranteed Limits		
$V_{IHA}$	Minimum High Level Input Voltage	$A_n$	4.5	2.7	2.0	2.0	V	$V_{OUT} \leq 0.1V$ or $\geq V_{CC} - 0.1V$
		$\overline{OE}$	4.5	3.6	2.0	2.0		
		T/ $\overline{R}$	5.5	5.5	2.0	2.0		
$V_{IHB}$		$B_n$	4.5	2.7	2.0	2.0	V	
			4.5	3.6	2.0	2.0		
			4.5	5.5	3.85	3.85		
$V_{ILA}$	Maximum Low Level Input Voltage	$A_n$	4.5	2.7	0.8	0.8	V	$V_{OUT} \leq 0.1V$ or $\geq V_{CC} - 0.1V$
		$\overline{OE}$	4.5	3.6	0.8	0.8		
		T/ $\overline{R}$	5.5	5.5	0.8	0.8		
$V_{ILB}$		$B_n$	4.5	2.7	0.8	0.8	V	
			4.5	3.6	0.8	0.8		
			4.5	5.5	1.65	1.65		
$V_{OHA}$	Minimum High Level Output Voltage		4.5	3.0	4.49	4.4	V	$I_{OUT} = -100 \mu A$ $I_{OH} = -24 \text{ mA}$
			4.5	3.0	4.25	3.86		
$V_{OHB}$			4.5	3.0	2.99	2.9	V	$I_{OUT} = -100 \mu A$ $I_{OH} = -12 \text{ mA}$ $I_{OH} = -24 \text{ mA}$ $I_{OH} = -12 \text{ mA}$ $I_{OH} = -24 \text{ mA}$ $I_{OH} = -24 \text{ mA}$
			4.5	3.0	2.85	2.56		
			4.5	3.0	2.65	2.35		
			4.5	2.7	2.5	2.3		
			4.5	2.7	2.3	2.1		
$V_{OLA}$	Maximum Low Level Output Voltage		4.5	3.0	0.002	0.1	V	$I_{OUT} = 100 \mu A$ $I_{OL} = 24 \text{ mA}$
			4.5	3.0	0.21	0.36		
$V_{OLB}$			4.5	3.0	0.002	0.1	V	$I_{OUT} = 100 \mu A$ $I_{OL} = 24 \text{ mA}$ $I_{OL} = 12 \text{ mA}$ $I_{OL} = 24 \text{ mA}$ $I_{OL} = 24 \text{ mA}$
			4.5	3.0	0.21	0.36		
			4.5	2.7	0.11	0.36		
			4.5	2.7	0.22	0.42		
			4.5	4.5	0.18	0.36		

## DC Electrical Characteristics (Continued)

		74LVXC4245						Units	Conditions	
Symbol	Parameter	V <sub>CCA</sub> (V)	V <sub>CCB</sub> (V)	T <sub>A</sub> = +25°C		T <sub>A</sub> = -40°C to +85°C				
				Typ	Guaranteed Limits					
I <sub>IN</sub>	Maximum Input Leakage Current @ OE, T/R	5.5 5.5	3.6 5.5	±0.1 ±0.1	±1.0 ±1.0		μA	V <sub>I</sub> = V <sub>CCA</sub> , GND		
I <sub>OZA</sub>	Maximum TRI-STATE Output Leakage @ A <sub>n</sub>	5.5 5.5	3.6 5.5	±0.5 ±0.5	±5.0 ±5.0		μA	V <sub>I</sub> = V <sub>IL</sub> , V <sub>IH</sub> , OE = V <sub>CCA</sub> V <sub>O</sub> = V <sub>CCA</sub> , GND		
I <sub>OZB</sub>	Maximum TRI-STATE Output Leakage @ B <sub>n</sub>	5.5 5.5	3.6 5.5	±0.5 ±0.5	±5.0 ±5.0		μA	V <sub>I</sub> = V <sub>IL</sub> , V <sub>IH</sub> , OE = V <sub>CCA</sub> V <sub>O</sub> = V <sub>CCB</sub> , GND		
ΔI <sub>CC</sub>	Maximum I <sub>CC</sub> /Input	All Inputs	5.5	5.5	1.0	1.35	1.5	mA	V <sub>I</sub> = V <sub>CC</sub> - 2.1V	
		B <sub>n</sub>	5.5	3.6	0.35		0.5	mA	V <sub>I</sub> = V <sub>CCB</sub> - 0.6V	
I <sub>CCA1</sub>	Quiescent V <sub>CCA</sub> Supply Current as B Port Floats	5.5	Open	8		80		μA	A <sub>n</sub> = V <sub>CCA</sub> or GND B <sub>n</sub> = Open, OE = V <sub>CCA</sub> T/R = V <sub>CCA</sub> , V <sub>CCB</sub> = Open	
I <sub>CCA2</sub>	Quiescent V <sub>CCA</sub> Supply Current	5.5	3.6	8		80		μA	A <sub>n</sub> = V <sub>CCA</sub> or GND B <sub>n</sub> = V <sub>CCB</sub> or GND OE = GND, T/R = GND	
		5.5	5.5	8		80				
I <sub>CCB</sub>	Quiescent V <sub>CCB</sub> Supply Current	5.5	3.6	5		50		μA	A <sub>n</sub> = V <sub>CCA</sub> or GND B <sub>n</sub> = V <sub>CCB</sub> or GND OE = GND, T/R = V <sub>CCA</sub>	
		5.5	5.5	8		80				
V <sub>OLPA</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	5.0 5.0	3.3 5.0	1.5 1.5				V	(Notes 1 and 2)	
V <sub>OLPB</sub>		5.0 5.0	3.3 5.0	0.8 1.5				V	(Notes 1 and 2)	
V <sub>OLVA</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	5.0 5.0	3.3 5.0	-1.2 -1.2				V	(Notes 1 and 2)	
V <sub>OLVB</sub>		5.0 5.0	3.3 5.0	-0.8 -1.2				V	(Notes 1 and 2)	
V <sub>IHDA</sub>	Minimum High Level Dynamic Input Voltage	5.0 5.0	3.3 5.0	2.0 2.0				V	(Notes 1 and 3)	
V <sub>IHDB</sub>		5.0 5.0	3.3 5.0	2.0 3.5				V	(Notes 1 and 3)	
V <sub>ILDA</sub>	Maximum Low Level Dynamic Input Voltage	5.0 5.0	3.3 5.0	0.8 0.8				V	(Notes 1 and 3)	
V <sub>ILDB</sub>		5.0 5.0	3.3 5.0	0.8 1.5				V	(Notes 1 and 3)	
<b>Note 1:</b> Worst case package.										
<b>Note 2:</b> Max number of outputs defined as (n). Data inputs are driven 0V to V <sub>CC</sub> level; one output at GND.										
<b>Note 3:</b> Max number of Data Inputs (n) switching. (n - 1) inputs switching 0V to V <sub>CC</sub> level. Input-under-test switching: V <sub>CC</sub> level to threshold (V <sub>IH</sub> ), 0V to threshold (V <sub>IL</sub> ), f = 1 MHz.										
V		1.0	1.0	0.002	0.0	0.0	Maximum Low Level Output Voltage			
		1.0	1.0	0.002	0.0	0.0				
V		1.0	1.0	0.002	0.0	0.0				
		1.0	1.0	0.002	0.0	0.0				
		1.0	1.0	0.002	0.0	0.0				
		1.0	1.0	0.002	0.0	0.0				
		1.0	1.0	0.002	0.0	0.0				
		1.0	1.0	0.002	0.0	0.0				

**AC Electrical Characteristics:** See Section 2 for Test Methodology

Symbol	Parameter	74LVXC4245						74LVXC4245						Units
		$C_L = 50 \text{ pF}$ $V_{CCA} = 4.5\text{V to } 5.5\text{V}$ $V_{CCB} = 4.5\text{V to } 5.5\text{V}$						$C_L = 50 \text{ pF}$ $V_{CCA} = 4.5\text{V to } 5.5\text{V}$ $V_{CCB} = 2.7\text{V to } 3.6\text{V}$						
		$T_A = +25^\circ\text{C}$			$T_A = -40^\circ\text{C to } +85^\circ\text{C}$			$T_A = +25^\circ\text{C}$			$T_A = -40^\circ\text{C to } +85^\circ\text{C}$			
		Min	Typ (Note 1)	Max	Min	Max	Min	Typ (Note 2)	Max	Min	Max	Min	Max	
$t_{PHL}$	Propagation Delay A to B	1.0	4.9	6.5	1.0	7.0	1.0	5.5	7.5	1.0	8.0	1.0	8.0	ns
$t_{PLH}$	Delay A to B	1.0	4.0	5.5	1.0	6.0	1.0	5.0	7.0	1.0	7.5	1.0	7.5	
$t_{PHL}$	Propagation Delay B to A	1.0	4.7	6.5	1.0	7.0	1.0	5.6	7.5	1.0	8.0	1.0	8.0	ns
$t_{PLH}$	Delay B to A	1.0	3.9	5.0	1.0	5.5	1.0	4.3	6.0	1.0	6.5	1.0	6.5	
$t_{PZL}$	Output Enable Time $\overline{OE}$ to B	1.0	5.6	7.5	1.0	8.0	1.0	6.7	9.0	1.0	10.0	1.0	10.0	ns
$t_{PZH}$	Time $\overline{OE}$ to B	1.0	5.7	7.5	1.0	8.0	1.0	6.9	9.5	1.0	10.0	1.0	10.0	
$t_{PZL}$	Output Enable Time $\overline{OE}$ to A	1.0	7.4	9.0	1.0	10.0	1.0	8.0	10.0	1.0	11.0	1.0	11.0	ns
$t_{PZH}$	Time $\overline{OE}$ to A	1.0	6.1	7.5	1.0	8.5	1.0	6.3	8.0	1.0	8.5	1.0	8.5	
$t_{PHZ}$	Output Disable Time $\overline{OE}$ to B	1.0	4.8	7.0	1.0	7.5	1.0	6.0	9.0	1.0	9.5	1.0	9.5	ns
$t_{PLZ}$	Time $\overline{OE}$ to B	1.0	3.8	5.5	1.0	6.0	1.0	4.2	6.5	1.0	7.0	1.0	7.0	
$t_{PHZ}$	Output Disable Time $\overline{OE}$ to A	1.0	3.4	5.5	1.0	6.0	1.0	3.4	5.5	1.0	6.0	1.0	6.0	ns
$t_{PLZ}$	Time $\overline{OE}$ to A	1.0	2.9	4.5	1.0	5.0	1.0	2.9	5.0	1.0	5.5	1.0	5.5	
$t_{OSHL}$ $t_{OSLH}$	Output to Output Skew (Note 3) Data to Output		1.0	1.5		1.5		1.0	1.5				1.5	ns

**Note 1:** Typical values at  $V_{CCA} = 5\text{V}$ ,  $V_{CCB} = 5\text{V}$  @25°C.

**Note 2:** Typical values at  $V_{CCA} = 5\text{V}$ ,  $V_{CCB} = 3.3\text{V}$  @25°C.

**Note 3:** Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW ( $t_{OSHL}$ ) or LOW to HIGH ( $t_{OSLH}$ ). Parameter guaranteed by design.

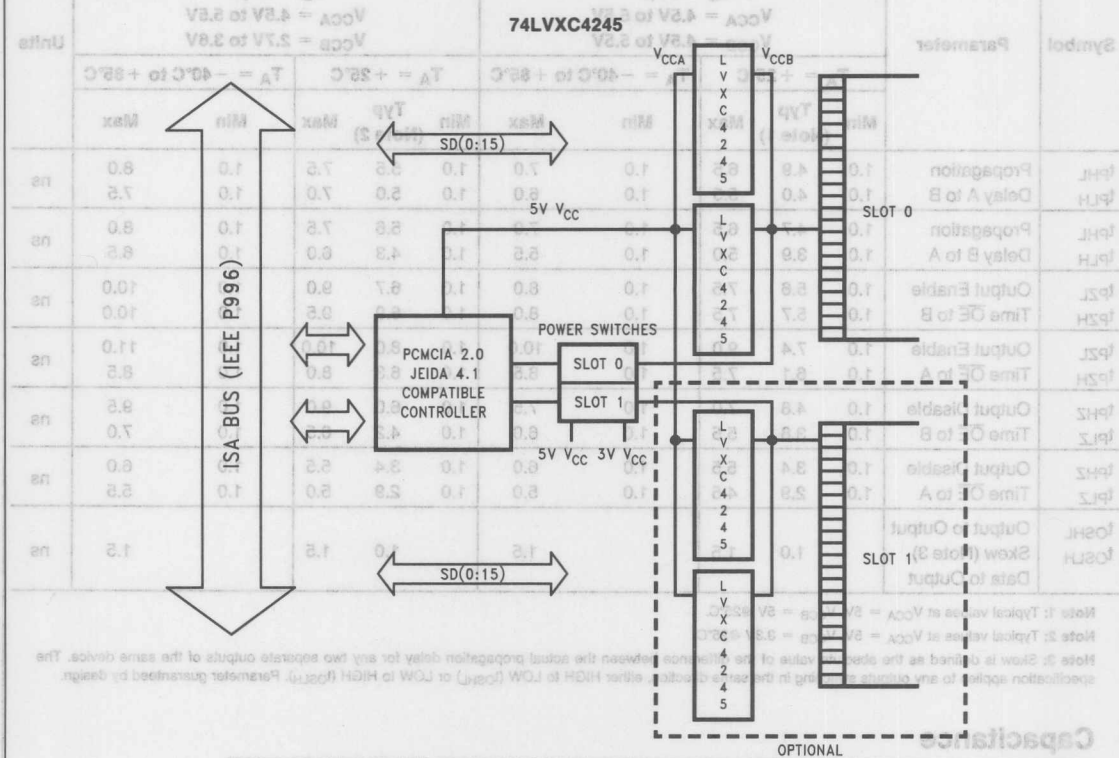
**Capacitance**

Symbol	Parameter	Typ	Units	Conditions	
C <sub>IN</sub>	Input Capacitance	4.5	pF	V <sub>CC</sub> = Open	
C <sub>I/O</sub>	Input/Output Capacitance	10	pF	V <sub>CCA</sub> = 5V, V <sub>CCB</sub> = 3.3V	
C <sub>PD</sub>	Power Dissipation Capacitance	A → B	45	pF	V <sub>CCA</sub> = 5V
		B → A	50	pF	V <sub>CCB</sub> = 3.3V

**Note:**  $C_{PD}$  is measured at 10 MHz.

## Configurable I/O Application for PCMCIA Cards

## Block Diagram



The LVXC4245 is a 24-pin dual supply device well suited for PCMCIA configurable I/O applications. Ideal for low power notebook designs, the LVXC4245 consumes less than 1 mW of quiescent power in all modes of operation. The LVXC4245 meets all PCMCIA I/O voltage requirements at 5V and 3.3V operation. By tying VCCB of the LVXC4245 to the card voltage supply, the PCMCIA card will always experience rail to rail output swings, maximizing the reliability of the interface.

The VCCA pin on the LVXC4245 must always be tied to a 5V power supply. This voltage connection provides internal references needed to account for variations in VCCB. When connected as in the block diagram above, the LVXC4245 meets all the voltage and current requirements of the ISA bus standard (IEEE P996).



## Section 7 Contents

7-3	..... LVX Bus Switch Family Features
7-4	..... 74LVX383 10-Bit Low Power Bus-Exchange Switch
7-7	..... 74LVX384 10-Bit Low Power Bus Switch

## Section 7 LVX Bus Switch Family



## Section 7 Contents

LVX Bus Switch Family Features .....	7-3
74LVX3L383 10-Bit Low Power Bus-Exchange Switch .....	7-4
74LVX3L384 10-Bit Low Power Bus Switch .....	7-7

Section 7  
LVX Bus Switch Family



## LVX Bus Switch Family Low Voltage CMOS Bus Switches

LVX Bus Switch Family

Features	Advantages
State-of-the-Art sub-micron BiCMOS process	Good ESD and Latchup immunity
Quick and easy 5V to 3V translation	Allows 3.3V components to interface with 5V signals
Near zero propagation delays; 250 ps typical	Facilitates high-performance bus connections and exchanges
Ultra low standby current ( $I_{CC}$ 3 $\mu$ A max over temp)	Saves power, extends battery life. Ideal for portable applications
Low on resistance ( $R_{on}$ ) and low input capacitance ( $C_i$ )	Minimizes bus loading
SOIC and QSOP	Saves board space and weight
Alternate source available	Product standardization. Ensured product supply

Connection Diagram

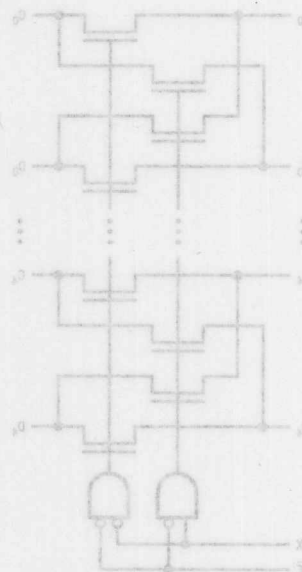


Pin Name	Description
BE	Bus Switch Enable
BX	Bus Exchange
A <sub>0</sub> -A <sub>3</sub> , B <sub>0</sub> -B <sub>3</sub>	Buses A, B
C <sub>0</sub> -C <sub>3</sub> , D <sub>0</sub> -D <sub>3</sub>	Buses C, D

Order Number	SOIC JEDEC	QSOP JEDEC
74LVX1383WM	74LVX1383WG	74LVX1383WG
74LVX1383MX	74LVX1383MX	74LVX1383MX
MOA24		

Preliminary Data: National Semiconductor reserves the right to make changes at any time without notice.

Logic Diagram



Truth Table

BE	BX	A <sub>0</sub> -A <sub>3</sub>	B <sub>0</sub> -B <sub>3</sub>	Function
H	X	High-Z State	High-Z State	Disconnect
L	L	C <sub>0</sub> -C <sub>3</sub>	D <sub>0</sub> -D <sub>3</sub>	Connect
L	H	D <sub>0</sub> -D <sub>3</sub>	C <sub>0</sub> -C <sub>3</sub>	Exchange

# 74LVX3L383

## 10-Bit Low Power Bus-Exchange Switch

### General Description

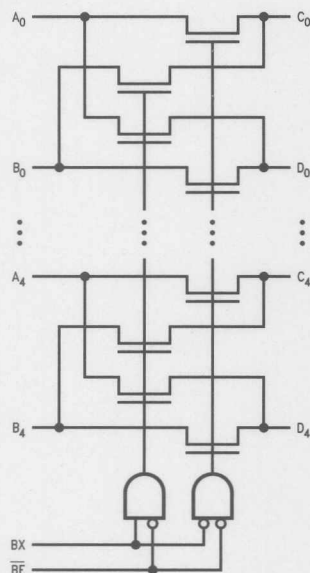
The LVX3L383 provides two sets of high-speed CMOS TTL-compatible bus switches. The low on resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise. The device operates as a 10-bit bus switch or a 5-bit bus exchanger. The bus exchange (BX) signal provides nibble swapping of the AB and CD pairs of signals. This exchange configuration allows byte swapping of buses in systems. It can also be used as a quad 2-to-1 multiplexer and to create low delay barrel shifters. The bus enable ( $\overline{BE}$ ) signal turns the switches on.

### Features

- 5 $\Omega$  switch connection between two ports
- Zero propagation delay
- Ultra low power with 0.2  $\mu$ A typical  $I_{CC}$
- Zero ground bounce in flow-through mode
- Control inputs compatible with TTL level
- Available in SOIC and QSOP (SSOP, 0.15" body width) packages

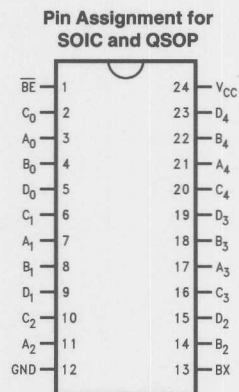
**Ordering Code:** See Section 11

### Logic Diagram



TL/F/11652-1

### Connection Diagram



TL/F/11652-2

Pin Names	Description
$\overline{BE}$	Bus Switch Enable
BX	Bus Exchange
$A_0-A_4, B_0-B_4$	Buses A, B
$C_0-C_4, D_0-D_4$	Buses C, D

### Truth Table

$\overline{BE}$	BX	$A_0-A_4$	$B_0-B_4$	Function
H	X	High-Z State	High-Z State	Disconnect
L	L	$C_0-C_4$	$D_0-D_4$	Connect
L	H	$D_0-D_4$	$C_0-C_4$	Exchange

	SOIC JEDEC	SSOP JEDEC
Order Number	74LVX3L383WM 74LVX3L383WMX	74LVX3L383QSC 74LVX3L383QSCX
See NS Package Number	M24B	MQA24

Preliminary Data: National Semiconductor reserves the right to make changes at any time without notice.

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Switch Voltage ( $V_S$ )	-0.5V to +7.0V
DC Input Voltage ( $V_I$ ) (Note 2)	-0.5V to +7.0V
DC Input Diode Current ( $I_{IN}$ ) with $V_I < 0$	-20 mA
DC Output ( $I_O$ ) Sink Current	120 mA
Storage Temperature Range ( $T_{STG}$ )	-65°C to +150°C
Power Dissipation	0.5W

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

Supply Voltage ( $V_{CC}$ )	4.0V to 5.5V
Free Air Operating Temperature ( $T_A$ )	-40°C to +85°C

## DC Electrical Characteristics

Symbol	Parameter	V <sub>CC</sub> (V)	74LVX3L383			Units	Conditions
			T <sub>A</sub> = −40°C to +85°C				
			Min	Typ (Note 3)	Max		
V <sub>IK</sub>	Maximum Clamp Diode Voltage	4.5			−1.2	V	I <sub>IN</sub> = −18 mA
V <sub>IH</sub>	Minimum High Level Input Voltage	4.0–5.5	2.0			V	
V <sub>IL</sub>	Maximum Low Level Input Voltage	4.0–5.5			0.8		
I <sub>IN</sub>	Maximum Input Leakage Current	0 5.5		10 ±1		μA	0 ≤ V <sub>IN</sub> ≤ 5.5V
I <sub>OZ</sub>	Maximum TRI-STATE® I/O Leakage	5.5			±1	μA	0 ≤ A, B ≤ V <sub>CC</sub>
I <sub>OS</sub>	Short Circuit Current	4.5	100			mA	V <sub>I</sub> (A), V <sub>I</sub> (B) = 0V, V <sub>I</sub> (B), V <sub>I</sub> (A) = 4.5V
R <sub>ON</sub>	Switch On Resistance (Note 1)	4.5	5	7		Ω	V <sub>I</sub> = 0V, I <sub>ON</sub> = 30 mA
			10	15		Ω	V <sub>I</sub> = 2.4V, I <sub>ON</sub> = 15 mA
I <sub>CC</sub>	Maximum Quiescent Supply Current	5.5	0.2	3.0		μA	V <sub>I</sub> = V <sub>CC</sub> , GND I <sub>O</sub> = 0
ΔI <sub>CC</sub>	Increase in I <sub>CC</sub> per Input (Note 2)	5.5		2.5		mA	V <sub>IN</sub> = 3.4V, I <sub>O</sub> = 0 Per Control Input

Note 1: Measured by voltage drop between A and B pin at indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B) pins.

Note 2: Per TTL driven input ( $V_{IN} = 3.4\text{V}$ , control inputs only). A and B pins do not contribute to  $I_{CC}$ .

Note 3: All typical values are at  $V_{CC} = 5.0\text{V}$ ,  $T_A = 25^\circ\text{C}$ .

**AC Electrical Characteristics:** See Section 2 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	74LVX3L383		Units
			Min	Typ (Note 2)	
T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF					
t <sub>PLH</sub> t <sub>PHL</sub>	Data Propagation Delay A <sub>n</sub> to B <sub>n</sub> or B <sub>n</sub> to A <sub>n</sub> (Note 1)	4.5		0.25	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Switch Exchange Time BX to A <sub>n</sub> or B <sub>n</sub>	4.5	1.5	6.5	ns
t <sub>PZL</sub> t <sub>PZH</sub>	Switch Enable Time BE to A <sub>n</sub> , B <sub>n</sub>	4.5	1.5	6.5	ns
t <sub>PLZ</sub> t <sub>PHZ</sub>	Switch Disenable Time BE to A <sub>n</sub> , B <sub>n</sub>	4.5	1.5	5.5	ns

**Note 1:** This parameter is guaranteed by design but not tested. The bus switch contributes no propagation delay other than the RC delay of the On resistance of the switch and the load capacitance. The time constant for the switch and alone is of the order of 0.25 ns for 50 pF load. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.

**Note 2:** All typical values are at V<sub>CC</sub> = 5.0V, T<sub>A</sub> = 25°C.

**Capacitance (Note)**

Symbol	Parameter	Typ	Max	Units	Conditions
C <sub>IN</sub>	Control Input Capacitance	4		pF	V <sub>CC</sub> = 5.0V
C <sub>I/O</sub> (ON)	Input/Output Capacitance	8		pF	V <sub>CC</sub> = 5.0V
C <sub>I/O</sub> (OFF)	Input/Output Capacitance	6		pF	V <sub>CC</sub> = 5.0V

**Note:** Capacitance is characterized but not tested.

V <sub>IL</sub>	V	0.8	4.0-5.5	2.0	Maximum Low Level Input Voltage
					Minimum High Level Input Voltage
V <sub>IH</sub>	V	2.0	4.0-5.5	2.0	Maximum High Level Input Voltage
					Minimum Low Level Input Voltage
I <sub>IL</sub>	A <sub>IL</sub>	±1	0	0	Maximum Input Leakage Current
					Maximum Input Leakage Current
I <sub>OL</sub>	A <sub>OL</sub>	±1	0	0	Maximum Output Leakage Current
					Maximum Output Leakage Current
I <sub>OS</sub>	mA	100	0	0	Short Circuit Current
					Short Circuit Current
R <sub>ON</sub>	Ω	10	10	10	Switch On Resistance (Note 1)
					Switch On Resistance (Note 1)
I <sub>CC</sub>	A <sub>CC</sub>	0.0	0.0	0.0	Maximum Quiescent Supply Current
					Maximum Quiescent Supply Current
ΔI <sub>CC</sub>	mA	2.5	2.5	2.5	Increase in I <sub>CC</sub> per Input (Note 2)
					Increase in I <sub>CC</sub> per Input (Note 2)

**Note 1:** Measured by voltage drop between A and B pins at indicated current through the switch. On resistance is determined by the lower of the voltages on the two pins (A or B).

**Note 2:** Per TTL driven input (V<sub>IL</sub> = 3.4V, control inputs only). A and B pins do not contribute to I<sub>CC</sub>.

**Note 3:** All typical values are at V<sub>CC</sub> = 5.0V, T<sub>A</sub> = 25°C.



# 74LVX3L384

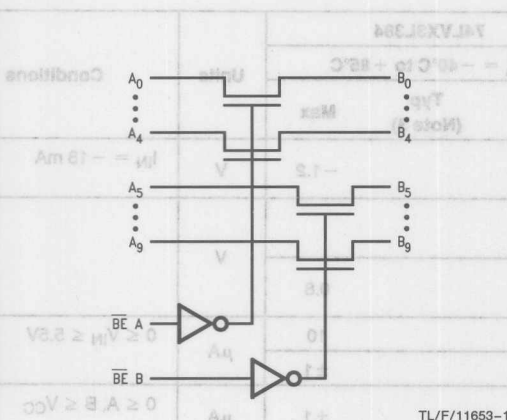
## 10-Bit Low Power Bus Switch

### General Description

The LVX3L384 provides 10 bits of high-speed CMOS TTL-compatible bus switches. The low on resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise. The device is organized as two 5-bit switches with separate bus enable ( $\overline{BE}$ ) signals. When  $\overline{BE}$  is low, the switch is on and port A is connected to port B. When  $\overline{BE}$  is high, the switch is open and a high-impedance state exists between the two ports.

**Ordering Code:** See Section 11

### Logic Diagram



### Truth Table

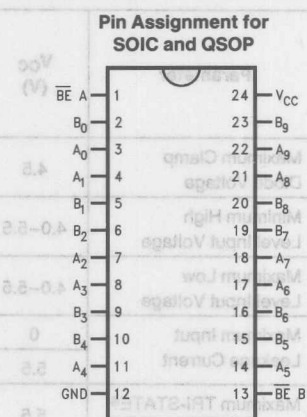
$\overline{BE} A$	$\overline{BE} B$	$B_0-B_4$	$B_5-B_9$	Function
L	L	$A_0-A_4$	$A_5-A_9$	Connect
L	H	$A_0-A_4$	HIGH-Z State	Connect
H	L	HIGH-Z State	$A_5-A_9$	Connect
H	H	HIGH-Z State	HIGH-Z State	Disconnect

### PRELIMINARY

### Features

- 5  $\Omega$  switch connection between two ports
- Zero propagation delay
- Ultra low power with 0.2  $\mu A$  typical  $I_{CC}$
- Zero ground bounce in flow-through mode
- Control inputs compatible with TTL level
- Available in SOIC and QSOP (SSOP 0.15" Body width)

### Connection Diagram



Pin Names	Description
$\overline{BE} A, \overline{BE} B$	Bus Switch Enable
$A_0-A_9$	Bus A
$B_0-B_9$	Bus B

	SOIC JEDEC	SSOP JEDEC
Order Number	74LVX3L384WM 74LVX3L384WMX	74LVX3L384QSC 74LVX3L384QSCX
See NS Package Number	M24B	MQA24

Preliminary Data: National Semiconductor reserves the right to make changes at any time without notice.

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Switch Voltage ( $V_S$ )	-0.5 to +7.0V
DC Input Input Voltage ( $V_I$ ) (Note 2)	-0.5 to +7.0V
DC Input Diode Current with ( $V_I < 0$ )	-20 mA
DC Output ( $I_O$ ) Sink Current	120 mA
Storage Temperature Range ( $T_{STG}$ )	-65°C to +150°C
Power Dissipation	0.5W

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

**Recommended Operating Conditions**

Supply Voltage ( $V_{CC}$ )	4.0V to 5.5V
Free Air Operating Temperature ( $T_A$ )	-40°C to +85°C

**DC Electrical Characteristics**

Symbol	Parameter	V <sub>CC</sub> (V)	74LVX3L384			Units	Conditions
			T <sub>A</sub> = −40°C to +85°C				
			Min	Typ (Note 3)	Max		
V <sub>IK</sub>	Maximum Clamp Diode Voltage	4.5			−1.2	V	I <sub>IN</sub> = −18 mA
V <sub>IH</sub>	Minimum High Level Input Voltage	4.0–5.5	2.0			V	
V <sub>IL</sub>	Maximum Low Level Input Voltage	4.0–5.5			0.8		
I <sub>IN</sub>	Maximum Input Leakage Current	0			10	μA	0 ≤ V <sub>IN</sub> ≤ 5.5V
		5.5			±1		
I <sub>OZ</sub>	Maximum TRI-STATE® I/O Leakage	5.5			±1	μA	0 ≤ A, B ≤ V <sub>CC</sub>
I <sub>OS</sub>	Short Circuit Current	4.5	100			mA	V <sub>I</sub> (A), V <sub>I</sub> (B) = 0V, V <sub>I</sub> (B), V <sub>I</sub> (A) = 4.5V
R <sub>ON</sub>	Switch On Resistance (Note 1)	4.5		5	7	Ω	V <sub>I</sub> = 0V, I <sub>ON</sub> = 30 mA
				10	15	Ω	V <sub>I</sub> = 2.4V, I <sub>ON</sub> = 15 mA
I <sub>CC</sub>	Maximum Quiescent Supply Current	5.5		0.2	3.0	μA	V <sub>I</sub> = V <sub>CC</sub> , GND I <sub>O</sub> = 0
ΔI <sub>CC</sub>	Increase in I <sub>CC</sub> per Input (Note 2)	5.5			2.5	mA	V <sub>IN</sub> = 3.4V, I <sub>O</sub> = 0 Per Control Input

Note 1: Measured by voltage drop between A and B pin at indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B) pins.

Note 2: Per TTL driven input ( $V_{IN} = 3.4\text{V}$ , control inputs only). A and B pins do not contribute to  $I_{CC}$ .

Note 3: All typical values are at  $V_{CC} = 5.0\text{V}$ ,  $T_A = 25^\circ\text{C}$ .

**AC Electrical Characteristics:** See Section 2 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	74LVX3L384			Units
			T <sub>A</sub> = −40°C to +85°C C <sub>L</sub> = 50 pF			
			Min	Typ (Note 2)	Max	
T <sub>PLH</sub> T <sub>PHL</sub>	Data Propagation Delay An to Bn or Bn to An (Note 1)	4.5			0.25	ns
T <sub>PZL</sub> T <sub>PZH</sub>	Switch Enable Time BE <sub>A</sub> , BE <sub>B</sub> to An, Bn	4.5	1.5		6.5	ns
T <sub>PLZ</sub> T <sub>PHZ</sub>	Switch Disable Time BE <sub>A</sub> , BE <sub>B</sub> to An, Bn	4.5	1.5		5.5	ns

**Note 1:** This parameter is guaranteed by design but not tested. The bus switch contributes no propagation delay other than the RC delay of the On resistance of the switch and the load capacitance. The time constant for the switch and alone is of the order of 0.25 ns for 50 pF load. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.

**Note 2:** All typical values are at V<sub>CC</sub> = 5.0V, T<sub>A</sub> = 25°C.

**Capacitance** (Note)

Symbol	Parameter	Typ	Max	Units	Conditions
C <sub>IN</sub>	Control Input Capacitance	4		pF	V <sub>CC</sub> = 5.0V
C <sub>I/O</sub> (ON)	Input/Output Capacitance	8		pF	V <sub>CC</sub> = 5.0V
C <sub>I/O</sub> (OFF)	Input/Output Capacitance	6		pF	V <sub>CC</sub> = 5.0V

**Note:** Capacitance is characterized but not tested.

		(V)	$C_L = 50\text{ pF}$	
			Min	Max
$T_{PLH}$ $T_{PHL}$	Data Propagation Delay An to Bn or Bn to An (Note 1)	4.5		0.25
$T_{PLZ}$ $T_{PHZ}$	Switch Enable Time $BE_A, BE_B$ to An, Bn	4.5	1.5	8.5
$T_{PZS}$ $T_{PHS}$	Switch Disable Time $BE_A, BE_B$ to An, Bn	4.5	1.5	8.5

Note 1: The parameter is guaranteed by design but not tested. The bus switch contributes no propagation delay other than the RC delay of the ON resistance of the switch and the load capacitance. The time constant for the switch and load is of the order of 0.25 ns for 50 pF load. Since this time constant is much smaller than the half-bit time of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.

Note 2: All typical values are at  $V_{CC} = 5.0\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

### Capacitance (Note)

Symbol	Parameter	Typ	Max	Units	Conditions
$C_{IN}$	Control Input Capacitance	4		pF	$V_{CC} = 5.0\text{ V}$
$C_{IO}(\text{ON})$	Input/Output Capacitance	8		pF	$V_{CC} = 5.0\text{ V}$
$C_{IO}(\text{OFF})$	Input/Output Capacitance	8		pF	$V_{CC} = 5.0\text{ V}$

Note: Capacitance is characterized but not tested.



Section 8 Contents

8-8	LVX Family Features
8-4	74LVX00 Low Voltage Quad 2-Input NAND Gate
8-7	74LVX02 Low Voltage Quad 2-Input NOR Gate
8-10	74LVX04 Low Voltage Hex Inverter
8-13	74LVX08 Low Voltage Quad 2-Input AND Gate
8-16	74LVX14 Low Voltage Hex Inverter with Schmitt Trigger Input
8-19	74LVX32 Low Voltage Quad 2-Input OR Gate
8-22	74LVX74 Low Voltage Dual D-Type Positive Edge-Triggered Flip-Flop
8-26	74LVX86 Low Voltage Quad 2-Input Exclusive-OR Gate
8-29	74LVX155 Low Voltage Quad Buffer with TRI-STATE Outputs
8-32	74LVX138 Low Voltage 1-Input Multiplexer
8-36	74LVX157 Low Voltage Quad 2-Input Multiplexer
8-40	74LVX174 Low Voltage Hex D Flip-Flop with Master Reset
8-43	74LVX240 Low Voltage Octal Buffer/Line Driver with TRI-STATE Outputs
8-46	74LVX244 Low Voltage Octal Buffer/Line Driver with TRI-STATE Outputs
8-49	74LVX245 Low Voltage Octal Bidirectional Transceiver
8-52	74LVX273 Low Voltage Octal D Flip-Flop
8-56	74LVX373 Low Voltage Octal Transparent Latch with TRI-STATE Outputs
8-61	74LVX374 Low Voltage Octal D Flip-Flop with TRI-STATE Outputs
8-65	74LVX573 Low Voltage Octal Latch with TRI-STATE Outputs

Section 8  
LVX Family



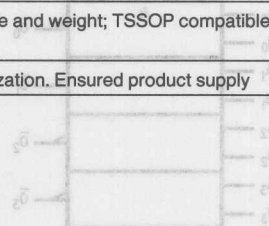
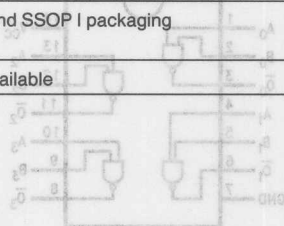
## Section 8 Contents

LVX Family Features .....	8-3
74LVX00 Low Voltage Quad 2-Input NAND Gate .....	8-4
74LVX02 Low Voltage Quad 2-Input NOR Gate .....	8-7
74LVX04 Low Voltage Hex Inverter .....	8-10
74LVX08 Low Voltage Quad 2-Input AND Gate .....	8-13
74LVX14 Low Voltage Hex Inverter with Schmitt Trigger Input .....	8-16
74LVX32 Low Voltage Quad 2-Input OR Gate .....	8-19
74LVX74 Low Voltage Dual D-Type Positive Edge-Triggered Flip-Flop .....	8-22
74LVX86 Low Voltage Quad 2-Input Exclusive-OR Gate .....	8-26
74LVX125 Low Voltage Quad Buffer with TRI-STATE Outputs .....	8-29
74LVX138 Low Voltage 1-of-8 Decoder/Demultiplexer .....	8-32
74LVX157 Low Voltage Quad 2-Input Multiplexer .....	8-36
74LVX174 Low Voltage Hex D Flip-Flop with Master Reset .....	8-40
74LVX240 Low Voltage Octal Buffer/Line Driver with TRI-STATE Outputs .....	8-43
74LVX244 Low Voltage Octal Buffer/Line Driver with TRI-STATE Outputs .....	8-46
74LVX245 Low Voltage Octal Bidirectional Transceiver .....	8-49
74LVX273 Low Voltage Octal D Flip-Flop .....	8-52
74LVX373 Low Voltage Octal Transparent Latch with TRI-STATE Outputs .....	8-56
74LVX374 Low Voltage Octal D Flip-Flop with TRI-STATE Outputs .....	8-61
74LVX573 Low Voltage Octal Latch with TRI-STATE Outputs .....	8-65



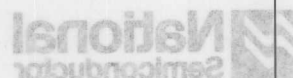
## LVX Family Low Voltage CMOS Logic (with 5V tolerant inputs)

Features	Advantages
Extended $V_{CC}$ range from 2.7V to 3.6V, compatible with JEDEC Std. No. 8-1B	Fully characterized for unregulated battery operation
0.8 $\mu\text{m}$ CMOS process	High performance with propagation delays as fast as 7.0 ns max for octals
No Input-diode clamp to $V_{CC}$	Interfaces directly to industry standard buses and 5V systems at inputs
Low standby current ( $I_{CC}$ 40 $\mu\text{A}$ max for octal over temp)	Saves power, extends battery life
$\pm 4$ mA drive current	Balanced drive
SOIC, EIAJ-SOIC and SSOP I packaging	Saves board space and weight; TSSOP compatible with PCMCIA standards
Alternate source available	Product standardization. Ensured product supply



Pin Names	Description
$A_n, B_n$	Inputs
$Y_n$	Outputs

Order Number	SOIC JEDEC	SOIC EIAJ	SSOP TYPE I
74LVX00M	74LVX00M	74LVX00M	74LVX00M
74LVX00MX	74LVX00MX	74LVX00MX	74LVX00MX
See NS Package Number	M14A	M14D	M2C14



## 74LVX00

### Low Voltage Quad 2-Input NAND Gate

#### General Description

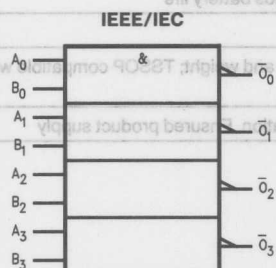
The LVX00 contains four 2-input NAND gates. The inputs tolerate voltages up to 7V allowing the interface of 5V systems to 3V systems.

#### Features

- Input voltage level translation from 5V to 3V
- Ideal for low power/low noise 3.3V applications
- Available in SOIC JEDEC, SOIC EIAJ and SSOP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance

**Ordering Code:** See Section 11

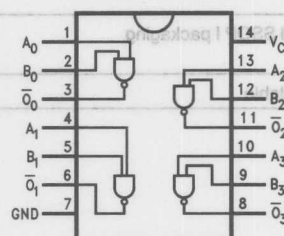
#### Logic Symbol



TL/F/11551-3

#### Connection Diagram

##### Pin Assignment for SOIC and SSOP



TL/F/11551-2

Pin Names	Description
$A_n, B_n$	Inputs
$\bar{O}_n$	Outputs

	SOIC JEDEC	SOIC EIAJ	SSOP TYPE I
Order Number	74LVX00M 74LVX00MX	74LVX00SJ 74LVX00SJX	74LVX00MSCX
See NS Package Number	M14A	M14D	MSC14

**Absolute Maximum Ratings** (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Input Diode Current ( $I_{IK}$ ) $V_I = -0.5V$	-20 mA
DC Input Voltage ( $V_I$ )	-0.5V to 7V
DC Output Diode Current ( $I_{OK}$ ) $V_O = -0.5V$	-20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage ( $V_O$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Source or Sink Current ( $I_O$ )	$\pm 25$ mA

DC $V_{CC}$ or Ground Current ( $I_{CC}$ or $I_{GND}$ )	$\pm 50$ mA
Storage Temperature ( $T_{STG}$ )	-65°C to +150°C
Power Dissipation	180 mW

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Recommended Operating Conditions**

Supply Voltage ( $V_{CC}$ )	2.0V to 3.6V
Input Voltage ( $V_I$ )	0V to 5.5V
Output Voltage ( $V_O$ )	0V to $V_{CC}$
Operating Temperature ( $T_A$ )	-40°C to +85°C
Input Rise and Fall Time ( $\Delta V/\Delta t$ )	0 ns/V to 100 ns/V

**DC Electrical Characteristics**

Symbol	Parameter	V <sub>CC</sub>	74LVX00			74LVX00		Units	Conditions	
			T <sub>A</sub> = +25°C			T <sub>A</sub> = −40°C to +85°C				
			Min	Typ	Max	Min	Max			
V <sub>IH</sub>	High Level Input Voltage	2.0	1.5			1.5		V		
		3.0	2.0			2.0				
		3.6	2.4			2.4				
V <sub>IL</sub>	Low Level Input Voltage	2.0			0.5		0.5	V		
		3.0			0.8		0.8			
		3.6			0.8		0.8			
V <sub>OH</sub>	High Level Output Voltage	2.0	1.9	2.0		1.9		V	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub>	I <sub>OH</sub> = −50 μA I <sub>OH</sub> = −50 μA I <sub>OH</sub> = −4 mA
		3.0	2.9	3.0		2.9				
		3.0	2.58			2.48				
V <sub>OL</sub>	Low Level Output Voltage	2.0		0.0	0.1		0.1	V	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub>	I <sub>OL</sub> = 50 μA I <sub>OL</sub> = 50 μA I <sub>OL</sub> = 4 mA
		3.0		0.0	0.1		0.1			
		3.0			0.36		0.44			
I <sub>IN</sub>	Input Leakage Current	3.6			±0.1		±1.0	μA	V <sub>IN</sub> = 5.5V or GND	
I <sub>CC</sub>	Quiescent Supply Current	3.6			2.0		20.0	μA	V <sub>IN</sub> = V <sub>CC</sub> or GND	

**Noise Characteristics:** See Section 2 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	74LVX00		Units	C <sub>L</sub> (pF)
			T <sub>A</sub> = 25°C			
			Typ	Limit		
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	3.3	0.3	0.5	V	50
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	3.3	−0.3	−0.5	V	50
V <sub>IHD</sub>	Minimum High Level Dynamic Input Voltage	3.3		2.0	V	50
V <sub>ILD</sub>	Maximum Low Level Dynamic Input Voltage	3.3		0.8	V	50

**Note:** (Input  $t_r = t_f = 3$  ns)

**AC Electrical Characteristics:** See Section 2 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	74LVX00			74LVX00			Units	C <sub>L</sub> (pF)
			T <sub>A</sub> = +25°C			T <sub>A</sub> = −40°C to +85°C				
			Min	Typ	Max	Min	Max			
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay Time	2.7	5.4	10.1		1.0	12.5			15
			7.9	13.6		1.0	16.0			50
		3.3 ± 0.3	4.1	6.2		1.0	7.5	ns		15
			6.6	9.7		1.0	11.0			50
t <sub>OSLH</sub> , t <sub>OSSL</sub>	Output to Output Skew (Note 1)	2.7			1.5			1.5	ns	50

**Note 1:** Parameter guaranteed by design  $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$ ,  $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$

## Capacitance

Symbol	Parameter	74LVX00			74LVX00		Units	
		T <sub>A</sub> = +25°C			T <sub>A</sub> = -40°C to +85°C			
		Min	Typ	Max	Min	Max		
C <sub>IN</sub>	Input Capacitance		4	10		8.0	10	pF
C <sub>PD</sub>	Power Dissipation Capacitance (Note 1)		19			8.0		pF

**Note 1:** C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:  $I_{CC(opr)} = \frac{C_{PD} \times V_{CC} \times f_{IN} + I_{CC}}{4}$  (per Gate)

**Note 1:**  $C_{PD}$  is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:  $I_{CC(opr.)} = \frac{C_{PD} \times V_{CC} \times f_{IN} + I_{CC}}{4 \text{ (per Gate)}}$



**74LVX02**

## Low Voltage Quad 2-Input NOR Gate

### General Description

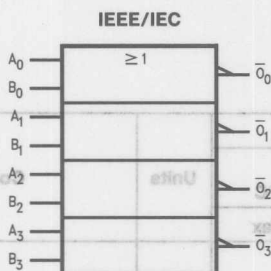
The LVX02 contains four 2-input NOR gates. The inputs tolerate voltages up to 7V allowing the interface of 5V systems to 3V systems.

### Features

- Input voltage level translation from 5V to 3V
- Ideal for low power/low noise 3.3V applications
- Available in SOIC JEDEC, SOIC EIAJ, and SSOP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance

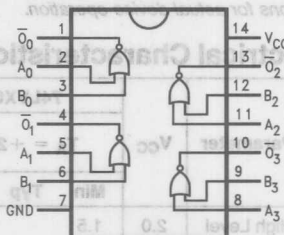
**Ordering Code:** See Section 11

### Logic Symbol



### Connection Diagram

Pin Assignment  
for SOIC and SSOP



Symbol		TL/F/11600-1		TL/F/11600-2		TL/F/11600-1	
High Level Input Voltage	3.0	3.0	3.0	3.0	3.0	3.0	3.0
Low Level Input Voltage	0.8	0.8	0.8	0.8	0.8	0.8	0.8
High Level Output Voltage	2.0	2.0	2.0	2.0	2.0	2.0	2.0
Low Level Output Voltage	0.8	0.8	0.8	0.8	0.8	0.8	0.8
Input Leakage Current	±0.1	±0.1	±0.1	±0.1	±0.1	±0.1	±0.1
Quiescent Supply Current	3.8	3.8	3.8	3.8	3.8	3.8	3.8

Pin Names	Description
A <sub>n</sub> , B <sub>n</sub>	Inputs
O <sub>n</sub>	Outputs

	SOIC JEDEC	SOIC EIAJ	SSOP TYPE I
Order Number	74LVX02M 74LVX02MX	74LVX02SJ 74LVX02SJX	74LVX02MSCX
See NS Package Number	M14A	M14D	MSC14

**Absolute Maximum Ratings** (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )  $-0.5V$  to  $+7.0V$

DC Input Diode Current ( $I_{IK}$ )  $-20$  mA  
 $V_I = -0.5V$

DC Input Voltage ( $V_I$ )  $-0.5V$  to  $7V$

DC Output Diode Current ( $I_{OK}$ )  $-20$  mA  
 $V_O = -0.5V$   
 $V_O = V_{CC} + 0.5V$

DC Output Voltage ( $V_O$ )  $-0.5V$  to  $V_{CC} + 0.5V$

DC Output Source or Sink Current ( $I_O$ )  $\pm 25$  mA

DC  $V_{CC}$  or Ground Current ( $I_{CC}$  or  $I_{GND}$ )  $\pm 50$  mA

Storage Temperature ( $T_{STG}$ )  $-65^\circ C$  to  $+150^\circ C$

Power Dissipation  $180$  mW

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Recommended Operating Conditions**

Supply Voltage ( $V_{CC}$ )  $2.0V$  to  $3.6V$

Input Voltage ( $V_I$ )  $0V$  to  $5.5V$

Output Voltage ( $V_O$ )  $0V$  to  $V_{CC}$

Operating Temperature ( $T_A$ )  $-40^\circ C$  to  $+85^\circ C$

Input Rise and Fall Time ( $\Delta t_r/\Delta t_f$ )  $0$  ns/V to  $100$  ns/V

**DC Electrical Characteristics**

Symbol	Parameter	V <sub>CC</sub>	74LVX02			74LVX02		Units	Conditions	
			T <sub>A</sub> = +25°C			T <sub>A</sub> = −40°C to +85°C				
			Min	Typ	Max	Min	Max			
V <sub>IH</sub>	High Level Input Voltage	2.0	1.5			1.5		V		
		3.0	2.0			2.0				
		3.6	2.4			2.4				
V <sub>IL</sub>	Low Level Input Voltage	2.0			0.5		0.5	V		
		3.0			0.8		0.8			
		3.6			0.8		0.8			
V <sub>OH</sub>	High Level Output Voltage	2.0	1.9	2.0		1.9		V	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OH</sub> = −50 μA I <sub>OH</sub> = −50 μA I <sub>OH</sub> = −4 mA	
		3.0	2.9	3.0		2.9				
		3.0	2.58			2.48				
V <sub>OL</sub>	Low Level Output Voltage	2.0		0.0	0.1		0.1	V	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OL</sub> = 50 μA I <sub>OL</sub> = 50 μA I <sub>OL</sub> = 4 mA	
		3.0		0.0	0.1		0.1			
		3.0			0.36		0.44			
I <sub>IN</sub>	Input Leakage Current	3.6			±0.1		±1.0	μA	V <sub>IN</sub> = 5.5V or GND	
I <sub>CC</sub>	Quiescent Supply Current	3.6			2.0		20.0	μA	V <sub>IN</sub> = V <sub>CC</sub> or GND	

Order Number	74LVX02M	74LVX02J	74LVX02C
See NS Package Number	M14A	M14D	M14A
	74LVX02MX	74LVX02JX	74LVX02CX
	74LVX02M	74LVX02J	74LVX02C

**Noise Characteristics:** See Section 2 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	74LVX02		Units	Conditions C <sub>L</sub> (pF)
			T <sub>A</sub> = 25°C			
			Typ	Limit		
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	3.3	0.3	0.5	V	50
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	3.3	−0.3	−0.5	V	50
V <sub>IHD</sub>	Minimum High Level Dynamic Input Voltage	3.3		2.0	V	50
V <sub>ILD</sub>	Maximum Low Level Dynamic Input Voltage	3.3		0.8	V	50

Note: (Input t<sub>r</sub> = t<sub>f</sub> = 3 ns)

**AC Electrical Characteristics:** See Section 2 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	74LVX02			74LVX02		Units	C <sub>L</sub> (pF)
			T <sub>A</sub> = +25°C			T <sub>A</sub> = −40°C to +85°C			
			Min	Typ	Max	Min	Max		
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay Time	2.7		5.9	10.7	1.0	13.5	ns	15
				8.4	14.2	1.0	17.0		50
		3.3 ± 0.3		4.5	6.6	1.0	8.0		15
				7.0	10.1	1.0	11.5		50
t <sub>OSLH</sub> , t <sub>OSHL</sub>	Output to Output Skew (Note 1)	2.7			1.5		1.5	ns	50

Note 1: Parameter guaranteed by design. t<sub>OSLH</sub> = |t<sub>PLHm</sub> - t<sub>PLHl</sub>|, t<sub>OSHL</sub> = |t<sub>PHLm</sub> - t<sub>PHLl</sub>|

**Capacitance**

Symbol	Parameter	74LVX02			74LVX02		Units
		T <sub>A</sub> = +25°C			T <sub>A</sub> = −40°C to +85°C		
		Min	Typ	Max	Min	Max	
C <sub>IN</sub>	Input Capacitance		4	10		10	pF
C <sub>PD</sub>	Power Dissipation Capacitance (Note 1)		15				pF

Note 1: C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:  $I_{CC(opr)} = \frac{C_{PD} \times V_{CC} \times f_{IN} + I_{CC}}{4}$  (per Gate)

Order Number	74LVX02M	74LVX02L	74LVX02S
See NS Package Number	M14D	M14D	M14D
	74LVX02MX	74LVX02LX	74LVX02SX
	M14D	M14D	M14D



## 74LVX04

### Low Voltage Hex Inverter

#### General Description

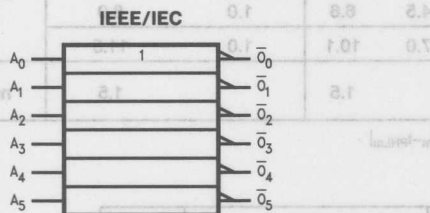
The LVX04 contains six inverters. The inputs tolerate voltages up to 7V allowing the interface of 5V systems to 3V systems.

#### Features

- Input voltage level translation from 5V to 3V
- Ideal for low power/low noise 3.3V applications
- Available in SOIC JEDEC, SOIC EIAJ and SSOP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance

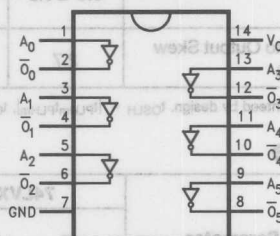
**Ordering Code:** See Section 11

#### Logic Symbol



#### Connection Diagram

Pin Assignment  
for SOIC and SSOP



Pin Names	Description
$A_n$	Inputs
$O_n$	Outputs

	SOIC JEDEC	SOIC EIAJ	SSOP TYPE I
Order Number	74LVX04M 74LVX04MX	74LVX04SJ 74LVX04SJX	74LVX04MSCX
See NS Package Number	M14A	M14D	MSC14

# Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )  $-0.5V$  to  $+7.0V$

DC Input Diode Current ( $I_{IK}$ )  
 $V_I = -0.5V$   $-20$  mA

DC Input Voltage ( $V_I$ )  $-0.5V$  to  $7V$

DC Output Diode Current ( $I_{OK}$ )  
 $V_O = -0.5V$   $-20$  mA  
 $V_O = V_{CC} + 0.5V$   $+20$  mA

DC Output Voltage ( $V_O$ )  $-0.5V$  to  $V_{CC} + 0.5V$

DC Output Source or Sink Current ( $I_O$ )  $\pm 25$  mA

DC  $V_{CC}$  or Ground Current ( $I_{CC}$  or  $I_{GND}$ )  $\pm 50$  mA

Storage Temperature ( $T_{STG}$ )  $-65^\circ C$  to  $+150^\circ C$

Power Dissipation  $180$  mW

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

# Recommended Operating Conditions

Supply Voltage ( $V_{CC}$ )  $2.0V$  to  $3.6V$

Input Voltage ( $V_I$ )  $0V$  to  $5.5V$

Output Voltage ( $V_O$ )  $0V$  to  $V_{CC}$

Operating Temperature ( $T_A$ )  $-40^\circ C$  to  $+85^\circ C$

Input Rise and Fall Time ( $\Delta t/\Delta v$ )  $0$  ns/V to  $100$  ns/V

# DC Electrical Characteristics

Symbol	Parameter	V <sub>CC</sub>	74LVX04			74LVX04		Units	Conditions
			T <sub>A</sub> = +25°C			T <sub>A</sub> = −40°C to +85°C			
			Min	Typ	Max	Min	Max		
V <sub>IH</sub>	High Level Input Voltage	2.0	1.5		1.5		V		
		3.0	2.0		2.0				
		3.6	2.4		2.4				
V <sub>IL</sub>	Low Level Input Voltage	2.0		0.5		0.5	V		
		3.0		0.8		0.8			
		3.6		0.8		0.8			
V <sub>OH</sub>	High Level Output Voltage	2.0	1.9	2.0	1.9		V	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OH</sub> = −50 μA I <sub>OH</sub> = −50 μA I <sub>OH</sub> = −4 mA	
		3.0	2.9	3.0	2.9				
		3.0	2.58		2.48				
V <sub>OL</sub>	Low Level Output Voltage	2.0		0.0	0.1	0.1	V	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OL</sub> = 50 μA I <sub>OL</sub> = 50 μA I <sub>OL</sub> = 4 mA	
		3.0		0.0	0.1	0.1			
		3.0		0.36	0.44	0.44			
I <sub>IN</sub>	Input Leakage Current	3.6		±0.1		±1.0	μA	V <sub>IN</sub> = 5.5V or GND	
I <sub>CC</sub>	Quiescent Supply Current	3.6		2.0		20.0	μA	V <sub>IN</sub> = V <sub>CC</sub> or GND	

# **Noise Characteristics:** See Section 2 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	74LVX04		Units	C <sub>L</sub> (pF)
			T <sub>A</sub> = 25°C			
			Typ	Limit		
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	3.3	0.3	0.5	V	50
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	3.3	−0.3	−0.5	V	50
V <sub>IHD</sub>	Minimum High Level Dynamic Input Voltage	3.3		2.0	V	50
V <sub>ILD</sub>	Maximum Low Level Dynamic Input Voltage	3.3		0.8	V	50

Note: (Input t<sub>r</sub> = t<sub>f</sub> = 3 ns)

# **AC Electrical Characteristics:** See Section 2 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	74LVX04			74LVX04		Units	C <sub>L</sub> (pF)
			T <sub>A</sub> = +25°C			T <sub>A</sub> = −40°C to +85°C			
			Min	Typ	Max	Min	Max		
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay Time	2.7	5.4	10.1	1.0	12.5	ns	15	
			7.9	13.6	1.0	16.0		50	
		3.3 ± 0.3	4.1	6.2	1.0	7.5	15		
			6.6	9.7	1.0	11.0	50		
t <sub>OSLH</sub> , t <sub>OSHL</sub>	Output to Output Skew (Note 1)	2.7	1.5			1.5	ns	50	

Note 1: Parameter guaranteed by design. t<sub>OSLH</sub> = |t<sub>PLHm</sub> - t<sub>PLHn</sub>|, t<sub>OSHL</sub> = |t<sub>PHLm</sub> - t<sub>PHLn</sub>|.

# **Capacitance**

Symbol	Parameter	74LVX04			74LVX04		Units
		T <sub>A</sub> = +25°C			T <sub>A</sub> = −40°C to +85°C		
		Min	Typ	Max	Min	Max	
C <sub>IN</sub>	Input Capacitance		4	10		10	pF
C <sub>PD</sub>	Power Dissipation Capacitance (Note 1)		18				pF

Note 1: C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:  $I_{CC(opr)} = \frac{C_{PD} \times V_{CC} \times f_{IN} + I_{CC}}{6 \text{ (per Gate)}}$

		V <sub>IN</sub> = 5.5V or GND	A <sub>IN</sub>	±1.0					
		V <sub>IN</sub> = V <sub>CC</sub> or GND	A <sub>IN</sub>	20.0		2.0			



## 74LVX08

### Low Voltage Quad 2-Input AND Gate

#### General Description

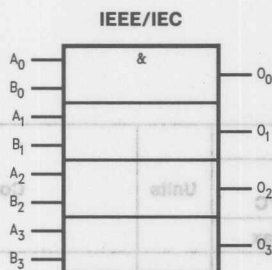
The LVX08 contains four 2-input AND gates. The inputs tolerate voltages up to 7V allowing the interface of 5V systems to 3V systems.

#### Features

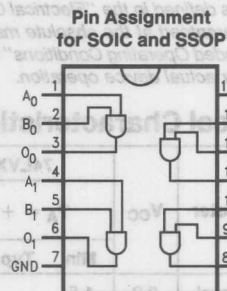
- Input voltage level translation from 5V to 3V
- Ideal for low power/low noise 3.3V applications
- Available in SOIC JEDEC, SOIC EIAJ, and SSOP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance

**Ordering Code:** See Section 11

#### Logic Symbol



#### Connection Diagram



Pin Names	Description
A <sub>n</sub> , B <sub>n</sub>	Inputs
O <sub>n</sub>	Outputs

	SOIC JEDEC	SOIC EIAJ	SSOP TYPE I
Order Number	74LVX08M 74LVX08MX	74LVX08SJ 74LVX08SJX	74LVX08MSCX
See NS Package Number	M14A	M14D	MSC14

**Absolute Maximum Ratings** (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Input Diode Current ( $I_{IK}$ )	-20 mA
$V_I = -0.5V$	-0.5V to 7V
DC Input Voltage ( $V_I$ )	-0.5V to 7V
DC Output Diode Current ( $I_{OK}$ )	-20 mA
$V_O = -0.5V$	+20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage ( $V_O$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Source or Sink Current ( $I_O$ )	$\pm 25$ mA
DC $V_{CC}$ or Ground Current ( $I_{CC}$ or $I_{GND}$ )	$\pm 50$ mA
Storage Temperature ( $T_{STG}$ )	-65°C to +150°C
Power Dissipation	180 mW
Lead Temperature ( $T_L$ ) (Soldering, 10 sec.)	240°C

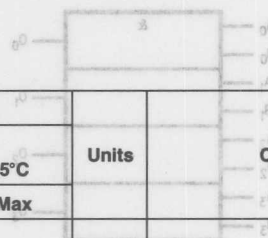
Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**DC Electrical Characteristics**

Symbol	Parameter	V <sub>CC</sub>	74LVX08			74LVX08		Units	Conditions	
			T <sub>A</sub> = +25°C			T <sub>A</sub> = −40°C to +85°C				
			Min	Typ	Max	Min	Max			
V <sub>IH</sub>	High Level Input Voltage	2.0	1.5			1.5		V		
		3.0	2.0			2.0				
		3.6	2.4			2.4				
V <sub>IL</sub>	Low Level Input Voltage	2.0			0.5		0.5	V		
		3.0			0.8		0.8			
		3.6			0.8		0.8			
V <sub>OH</sub>	High Level Output Voltage	2.0	1.9	2.0		1.9		V	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub>	I <sub>OH</sub> = −50 μA I <sub>OH</sub> = −50 μA I <sub>OH</sub> = −4 mA
		3.0	2.9	3.0		2.9				
		3.0	2.58			2.48				
V <sub>OL</sub>	Low Level Output Voltage	2.0		0.0	0.1		0.1	V	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub>	I <sub>OL</sub> = 50 μA I <sub>OL</sub> = 50 μA I <sub>OL</sub> = 4 mA
		3.0		0.1	0.1		0.1			
		3.0			0.36		0.44			
I <sub>IN</sub>	Input Leakage Current	3.6			±0.1		±1.0	μA	V <sub>IN</sub> = 5.5V or GND	
I <sub>CC</sub>	Quiescent Supply Current	3.6			2.0		20.0	μA	V <sub>IN</sub> = V <sub>CC</sub> or GND	

**Recommended Operating Conditions**

Supply Voltage ( $V_{CC}$ )	2.0V to 3.6V
Input Voltage ( $V_I$ )	0V to 5.5V
Output Voltage ( $V_O$ )	0V to $V_{CC}$
Operating Temperature ( $T_A$ )	-40°C to +85°C
Input Rise and Fall Time ( $\Delta t_r/\Delta t_f$ )	0 ns/V to 100 ns/V



**Noise Characteristics:** See Section 2 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	74LVX08		Units	C <sub>L</sub> (pF)
			T <sub>A</sub> = 25°C			
			Typ	Limit		
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	3.3	0.3	0.5	V	50
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	3.3	−0.3	−0.5	V	50
V <sub>IHD</sub>	Minimum High Level Dynamic Input Voltage	3.3		2.0	V	50
V <sub>ILD</sub>	Maximum Low Level Dynamic Input Voltage	3.3		0.8	V	50

Note: (Input t<sub>r</sub> = t<sub>f</sub> = 3 ns)

**AC Electrical Characteristics:** See Section 2 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	74LVX08			74LVX08		Units	C <sub>L</sub> (pF)
			T <sub>A</sub> = +25°C			T <sub>A</sub> = −40°C to +85°C			
			Min	Typ	Max	Min	Max		
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay Time	2.7		6.3	11.4	1.0	13.5	ns	15
				8.8	14.9	1.0	17.0		50
		3.3 ± 0.3		4.8	7.1	1.0	8.5		15
				7.3	10.6	1.0	12.0		50
t <sub>OSLH</sub> , t <sub>OSHL</sub>	Output to Output Skew (Note 1)	2.7			1.5		1.5	ns	50

Note 1: Parameter guaranteed by design. t<sub>OSLH</sub> = |t<sub>PLHm</sub> - t<sub>PLHn</sub>|, t<sub>OSHL</sub> = |t<sub>PHLm</sub> - t<sub>PHLn</sub>|

**Capacitance**

Symbol	Parameter	74LVX08			74LVX08		Units
		T <sub>A</sub> = +25°C			T <sub>A</sub> = −40°C to +85°C		
		Min	Typ	Max	Min	Max	
C <sub>IN</sub>	Input Capacitance		4	10		10	pF
C <sub>PD</sub>	Power Dissipation Capacitance (Note 1)		18				pF

Note 1: C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:  $I_{CC(opr)} = \frac{C_{PD} \times V_{CC} \times f_{IN} + I_{CC}}{4}$  (per Gate)

Pin Names	
Inputs	I <sub>1</sub> , I <sub>2</sub>
Outputs	O <sub>1</sub> , O <sub>2</sub>

Output	Input
0	A
H	L
L	H

Order Number	74LVX14MM	74LVX14MX	74LVX14SX
See NS Package Number	M14A	M14D	M14C
	SOIC JEDEC	SOIC EIAJ	SSOP TYPE I

# 74LVX14

## Low Voltage Hex Inverter with Schmitt Trigger Input

### General Description

The LVX14 contains six inverter gates each with a Schmitt trigger input. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. In addition, they have a greater noise margin than conventional inverters.

The LVX14 has hysteresis between the positive-going and negative-going input thresholds (typically 1.0V) which is determined internally by transistor ratios and is essentially insensitive to temperature and supply voltage variations.

The inputs tolerate voltages up to 7V allowing the interface of 5V systems to 3V systems.

### Features

- Input voltage level translation from 5V to 3V
- Ideal for low power/low noise 3.3V applications
- Available in SOIC JEDEC, SOIC EIAJ and SSOP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance

**Ordering Code:** See Section 11

### Logic Symbol

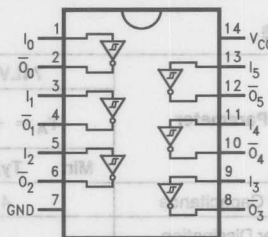
### Connection Diagram

IEEE/IEC



TL/F/11603-2

Pin Assignment  
for SOIC and SSOP



TL/F/11603-1

Pin Names	Description
$I_n$	Inputs
$O_n$	Outputs

### Truth Table

Input	Output
A	$\bar{O}$
L	H
H	L

	SOIC JEDEC	SOIC EIAJ	SSOP TYPE I
Order Number	74LVX14M 74LVX14MX	74LVX14SJ 74LVX14SJX	74LVX14MSCX
See NS Package Number	M14A	M14D	MSC14

**Absolute Maximum Ratings** (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )  $-0.5V$  to  $+7.0V$

DC Input Diode Current ( $I_{IK}$ )  
 $V_I = -0.5V$   $-20$  mA

DC Input Voltage ( $V_I$ )  $-0.5V$  to  $7V$

DC Output Diode Current ( $I_{OK}$ )  
 $V_O = -0.5V$   $-20$  mA  
 $V_O = V_{CC} + 0.5V$   $+20$  mA

DC Output Voltage ( $V_O$ )  $-0.5V$  to  $V_{CC} + 0.5V$

DC Output Source or Sink Current ( $I_O$ )  $\pm 25$  mA

DC  $V_{CC}$  or Ground Current ( $I_{CC}$  or  $I_{GND}$ )  $\pm 50$  mA

Storage Temperature ( $T_{STG}$ )  $-65^\circ C$  to  $+150^\circ C$

Power Dissipation  $180$  mW

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Recommended Operating Conditions**

Supply Voltage ( $V_{CC}$ )  $2.0V$  to  $3.6V$

Input Voltage ( $V_I$ )  $0V$  to  $5.5V$

Output Voltage ( $V_O$ )  $0V$  to  $V_{CC}$

Operating Temperature ( $T_A$ )  $-40^\circ C$  to  $+85^\circ C$

Input Rise and Fall Time ( $\Delta t_r/\Delta t_f$ )  $0$  ns/V to  $100$  ns/V

**DC Electrical Characteristics**

Symbol	Parameter	V <sub>CC</sub>	74LVX14			74LVX14		Units	Conditions	
			T <sub>A</sub> = +25°C			T <sub>A</sub> = −40°C to +85°C				
			Min	Typ	Max	Min	Max			
V <sub>t+</sub>	Positive Threshold	3.0			2.2		2.2	V		
V <sub>t−</sub>	Negative Threshold	3.0	0.9			0.9		V		
V <sub>H</sub>	Hysteresis	3.0	0.3		1.2	0.3	1.2	V		
V <sub>OH</sub>	High Level Output Voltage	2.0	1.9	2.0		1.9		V	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub>	I <sub>OH</sub> = −50 μA
		3.0	2.9	3.0		2.9				I <sub>OH</sub> = −50 μA
		3.0	2.58			2.48				I <sub>OH</sub> = −4 mA
V <sub>OL</sub>	Low Level Output Voltage	2.0		0.0	0.1		0.1	V	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub>	I <sub>OL</sub> = 50 μA
		3.0		0.0	0.1		0.1			I <sub>OL</sub> = 50 μA
		3.0			0.36		0.44			I <sub>OL</sub> = 4 mA
I <sub>IN</sub>	Input Leakage Current	3.6			±0.1		±1.0	μA	V <sub>IN</sub> = 5.5V or GND	
I <sub>CC</sub>	Quiescent Supply Current	3.6			2.0		20	μA	V <sub>IN</sub> = V <sub>CC</sub> or GND	

**Noise Characteristics:** See Section 2 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	74LVX14 T <sub>A</sub> = 25°C		Units	C <sub>L</sub> (pF)
			Typ	Limit		
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	3.3	0.3	0.5	V	50
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	3.3	-0.3	-0.5	V	50
V <sub>IHD</sub>	Minimum High Level Dynamic Input Voltage	3.3		2.0	V	50
V <sub>ILD</sub>	Maximum Low Level Dynamic Input Voltage	3.3		0.8	V	50

Note: Input t<sub>r</sub> = t<sub>f</sub> = 3 ns**AC Electrical Characteristics:** See Section 2 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	74LVX14			74LVX14		Units	C <sub>L</sub> (pF)
			T <sub>A</sub> = +25°C			T <sub>A</sub> = −40°C to +85°C			
			Min	Typ	Max	Min	Max		
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay Time	2.7		8.7	16.3	1.0	19.5	ns	15
				11.2	19.8	1.0	23.0		50
		3.3 ± 0.3		6.8	10.6	1.0	12.5		15
				9.3	14.1	1.0	16.0		50
t <sub>OSLH</sub> , t <sub>OSHL</sub>	Output to Output Skew (Note 1)	2.7			1.5		1.5	ns	50

Note 1: Parameter guaranteed by design. t<sub>OSLH</sub> = |t<sub>PLHm</sub> - t<sub>PLHn</sub>|, t<sub>OSHL</sub> = |t<sub>PHLm</sub> - t<sub>PHLn</sub>|**Capacitance**

Symbol	Parameter	74LVX14			74LVX14		Units
		T <sub>A</sub> = +25°C			T <sub>A</sub> = −40°C to +85°C		
		Min	Typ	Max	Min	Max	
C <sub>IN</sub>	Input Capacitance		4	10		10	pF
C <sub>PD</sub>	Power Dissipation Capacitance (Note 1)		21				pF

Note 1: C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.Average operating current can be obtained by the equation:  $I_{CC(opr)} = \frac{C_{PD} \times V_{CC} \times f_{IN} + I_{CC}}{6 \text{ (per Gate)}}$ 

	V <sub>IN</sub> = 0V to V <sub>CC</sub> or GND	I <sub>CC</sub>	3.0	3.0	3.0	Low Level Output Voltage
	V <sub>IN</sub> = V <sub>CC</sub> or GND	I <sub>CC</sub>	3.0	3.0	3.0	High Level Output Voltage
	V <sub>IN</sub> = 0V to V <sub>CC</sub> or GND	I <sub>CC</sub>	3.0	3.0	3.0	Low Level Input Leakage Current
	V <sub>IN</sub> = V <sub>CC</sub> or GND	I <sub>CC</sub>	3.0	3.0	3.0	High Level Input Leakage Current



## 74LVX32

### Low Voltage Quad 2-Input OR Gate

#### General Description

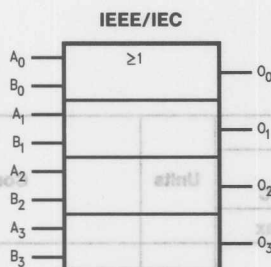
The LVX32 contains four 2-input OR gates. The inputs tolerate voltages up to 7V allowing the interface of 5V systems to 3V systems.

#### Features

- Input voltage level translation from 5V to 3V
- Ideal for low power/low noise 3.3V applications
- Available in SOIC JEDEC, SOIC EIAJ and SSOP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance

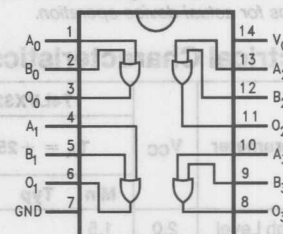
**Ordering Code:** See Section 11

#### Logic Symbol



#### Connection Diagram

##### Pin Assignment for SOIC and SSOP



Pin Names	Description
$A_n, B_n$	Inputs
$O_n$	Outputs

	SOIC JEDEC	SOIC EIAJ	SSOP TYPE I
Order Number	74LVX32M 74LVX32MX	74LVX32SJ 74LVX32SJX	74LVX32MSCX
NS Package Number	M14A	M14D	MSC14

**Absolute Maximum Ratings** (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )  $-0.5V$  to  $+7.0V$

DC Input Diode Current ( $I_{IK}$ )  $-20$  mA  
 $V_I = -0.5V$

DC Input Voltage ( $V_I$ )  $-0.5V$  to  $7V$

DC Output Diode Current ( $I_{OK}$ )  $-20$  mA  
 $V_O = -0.5V$

$V_O = V_{CC} + 0.5V$

DC Output Voltage ( $V_O$ )  $-0.5V$  to  $V_{CC} + 0.5V$

DC Output Source or Sink Current ( $I_O$ )  $\pm 25$  mA

DC  $V_{CC}$  or Ground Current ( $I_{CC}$  or  $I_{GND}$ )  $\pm 50$  mA

Storage Temperature ( $T_{STG}$ )  $-65^\circ C$  to  $+150^\circ C$

Power Dissipation  $180$  mW

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Recommended Operating Conditions**

Supply Voltage ( $V_{CC}$ )  $2.0V$  to  $3.6V$

Input Voltage ( $V_I$ )  $0V$  to  $5.5V$

Output Voltage ( $V_O$ )  $0V$  to  $V_{CC}$

Operating Temperature ( $T_A$ )  $-40^\circ C$  to  $+85^\circ C$

Input Rise and Fall Time ( $\Delta t_r/\Delta t_f$ )  $0$  ns/V to  $100$  ns/V

**DC Electrical Characteristics**

Symbol	Parameter	V <sub>CC</sub>	74LVX32			74LVX32		Units	Conditions			
			T <sub>A</sub> = +25°C			T <sub>A</sub> = −40°C to +85°C						
			Min	Typ	Max	Min	Max					
V <sub>IH</sub>	High Level Input Voltage	2.0 3.0 3.6	1.5 2.0 2.4			1.5 2.0 2.4		V				
V <sub>IL</sub>	Low Level Input Voltage	2.0 3.0 3.6			0.5 0.8 0.8		0.5 0.8 0.8	V				
V <sub>OH</sub>	High Level Output Voltage	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0		1.9 2.9 2.48		V	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub>	I <sub>OH</sub> = −50 μA I <sub>OH</sub> = −50 μA I <sub>OH</sub> = −4 mA		
V <sub>OL</sub>	Low Level Output Voltage	2.0 3.0 3.0		0.0 0.0 0.36	0.1 0.1 0.44		0.1 0.1 0.44	V	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub>	I <sub>OL</sub> = 50 μA I <sub>OL</sub> = 50 μA I <sub>OL</sub> = 4 mA		
I <sub>IN</sub>	Input Leakage Current	3.6			±0.1		±1.0	μA	V <sub>IN</sub> = 5.5V or GND			
I <sub>CC</sub>	Quiescent Supply Current	3.6			2.0		20	μA	V <sub>IN</sub> = V <sub>CC</sub> or GND			

**Noise Characteristics:** See Section 2 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	74LVX32		Units	C <sub>L</sub> (pF)
			T <sub>A</sub> = 25°C			
			Typ	Limit		
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	3.3	0.3	0.5	V	50
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	3.3	−0.3	−0.5	V	50
V <sub>IHD</sub>	Minimum High Level Dynamic Input Voltage	3.3		2.0	V	50
V <sub>ILD</sub>	Maximum Low Level Dynamic Input Voltage	3.3		0.8	V	50

Note: (Input t<sub>r</sub> = t<sub>f</sub> = 3 ns)

**AC Electrical Characteristics:** See Section 2 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	74LVX32			74LVX32		Units	C <sub>L</sub> (pF)
			T <sub>A</sub> = +25°C			T <sub>A</sub> = -40°C to +85°C			
			Min	Typ	Max	Min	Max		
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay Time	2.7		5.8	10.7	1.0	12.5	ns	15
				8.3	14.2	1.0	16.0		50
		3.3 ± 0.3		4.4	6.6	1.0	7.5	ns	15
				6.9	10.1	1.0	11.5		50
t <sub>OSLH</sub> , t <sub>OSHL</sub>	Output to Output Skew (Note 1)	2.7			1.5		1.5	ns	50

Note 1: Parameter guaranteed by design. t<sub>OSLH</sub> = |t<sub>PLHm</sub> - t<sub>PLHn</sub>|, t<sub>OSHL</sub> = |t<sub>PHLm</sub> - t<sub>PHLn</sub>|

**Capacitance**

Symbol	Parameter	74LVX32			74LVX32		Units
		T <sub>A</sub> = +25°C			T <sub>A</sub> = -40°C to +85°C		
		Min	Typ	Max	Min	Max	
C <sub>IN</sub>	Input Capacitance		4	10		10	pF
C <sub>PD</sub>	Power Dissipation Capacitance (Note 1)		14				pF

Note 1: C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:  $I_{CC(opr)} = \frac{C_{PD} \times V_{CC} \times f_{IN} + I_{CC}}{4 \text{ (per Gate)}}$

Pin Name	Description
D <sub>1</sub> , D <sub>2</sub>	Data Inputs
C <sub>P1</sub> , C <sub>P2</sub>	Clock Pulse Inputs
C <sub>D1</sub> , C <sub>D2</sub>	Direct Clear Inputs
S <sub>D1</sub> , S <sub>D2</sub>	Direct Set Inputs
O <sub>1</sub> , O <sub>2</sub>	Outputs

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial  
~ = LOW-to-HIGH Clock Transition  
Q<sub>0</sub> = Previous Q(t) before LOW-to-HIGH Transition of Clock

Order Number	SOIC JEDEC	SOIC BIAJ	280P TYPE I
74LVX32MM	74LVX32MM	74LVX32MM	74LVX32MM
74LVX32MX	74LVX32MX	74LVX32MX	74LVX32MX
Package Number	MM	MM	MM



## 74LVX74

### Low Voltage Dual D-Type Positive Edge-Triggered Flip-Flop

#### General Description

The LVX74 is a dual D-type flip-flop with Asynchronous Clear and Set inputs and complementary ( $Q$ ,  $\bar{Q}$ ) outputs. Information at the input is transferred to the outputs on the positive edge of the clock pulse. After the Clock Pulse input threshold voltage has been passed, the Data input is locked out and information present will not be transferred to the outputs until the next rising edge of the Clock Pulse input.

#### Asynchronous Inputs:

LOW input to  $\bar{S}_D$  (Set) sets  $Q$  to HIGH level

LOW input to  $\bar{C}_D$  (Clear) sets  $Q$  to LOW level

Clear and Set are independent of clock

Simultaneous LOW on  $\bar{C}_D$  and  $\bar{S}_D$  makes both  $Q$  and  $\bar{Q}$

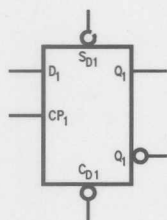
HIGH

#### Features

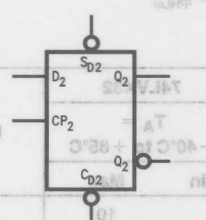
- Input voltage level translation from 5V to 3V
- Ideal for low power/low noise 3.3V applications
- Available in SOIC JEDEC, SOIC EIAJ and SSOP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance

**Ordering Code:** See Section 11

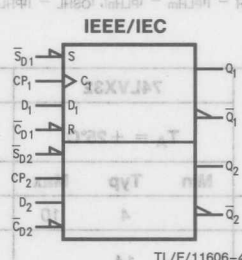
#### Logic Symbols



TL/F/11606-1

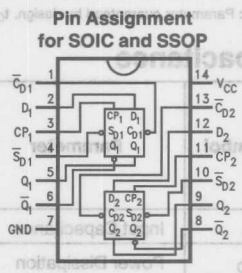


TL/F/11606-2



TL/F/11606-4

#### Connection Diagram



#### Truth Table (Each Half)

Pin Names	Description
$D_1, D_2$	Data Inputs
$CP_1, CP_2$	Clock Pulse Inputs
$\bar{C}_D1, \bar{C}_D2$	Direct Clear Inputs
$\bar{S}_D1, \bar{S}_D2$	Direct Set Inputs
$Q_1, \bar{Q}_1, Q_2, \bar{Q}_2$	Outputs

Inputs			Outputs		
$\bar{S}_D$	$\bar{C}_D$	CP	D	Q	$\bar{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H
H	H	↗	H	H	L
H	H	↘	L	L	H
H	H	L	X	$Q_0$	$\bar{Q}_0$

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

↗ = LOW-to-HIGH Clock Transition

$Q_0(\bar{Q}_0)$  = Previous  $Q(\bar{Q})$  before LOW-to-HIGH Transition of Clock

	SOIC JEDEC	SOIC EIAJ	SSOP TYPE I
Order Number	74LVX74M 74LVX74MX	74LVX74SJ 74LVX74SJX	74LVX74MSCX
See NS Package Number	M14A	M14D	MSC14

**Absolute Maximum Ratings** (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Input Diode Current ( $I_{IK}$ )	-20 mA
$V_I = -0.5V$	-0.5V to 7V
DC Input Voltage ( $V_I$ )	-20 mA
DC Output Diode Current ( $I_{OK}$ )	+20 mA
$V_O = -0.5V$	-0.5V to $V_{CC} + 0.5V$
$V_O = V_{CC} \pm 0.5V$	$\pm 25$ mA
DC Output Voltage ( $V_O$ )	
DC Output Source or Sink Current ( $I_O$ )	

DC $V_{CC}$ or Ground Current ( $I_{CC}$ or $I_{GND}$ )	$\pm 50$ mA
Storage Temperature ( $T_{STG}$ )	-65°C to +150°C
Power Dissipation	180 mW

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**DC Electrical Characteristics**

Symbol	Parameter	V <sub>CC</sub>	74LVX74			74LVX74		Units	Conditions
			T <sub>A</sub> = +25°C			T <sub>A</sub> = -40°C to +85°C			
			Min	Typ	Max	Min	Max		
V <sub>IH</sub>	High Level Input Voltage	2.0	1.5		1.5		V		
		3.0	2.0		2.0				
		3.6	2.4		2.4				
V <sub>IL</sub>	Low Level Input Voltage	2.0		0.5		0.5	V		
		3.0		0.8		0.8			
		3.6		0.8		0.8			
V <sub>OH</sub>	High Level Output Voltage	2.0	1.9	2.0	1.9		V	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OH</sub> = -50 μA I <sub>OH</sub> = -50 μA I <sub>OH</sub> = -4 mA	
		3.0	2.9	3.0	2.9				
		3.0	2.58		2.48				
V <sub>OL</sub>	Low Level Output Voltage	2.0		0.0	0.1	0.1	V	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OL</sub> = 50 μA I <sub>OL</sub> = 50 μA I <sub>OL</sub> = 4 mA	
		3.0		0.0	0.1	0.1			
		3.0		0.36		0.44			
I <sub>IN</sub>	Input Leakage Current	3.6		±0.1		±1.0	μA	V <sub>IN</sub> = 5.5V or GND	
I <sub>CC</sub>	Quiescent Supply Current	3.6		2.0		20.0	μA	V <sub>IN</sub> = V <sub>CC</sub> or GND	

**Recommended Operating Conditions**

Supply Voltage ( $V_{CC}$ )	2.0V to 3.6V
Input Voltage ( $V_I$ )	0V to 5.5V
Output Voltage ( $V_O$ )	0V to $V_{CC}$
Operating Temperature ( $T_A$ )	-40°C to +85°C
Input Rise and Fall Time ( $\Delta t/\Delta v$ )	0 ns/V to 100 ns/V

**Noise Characteristics:** See Section 2 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	74LVX74		Units	C <sub>L</sub> (pF)
			T <sub>A</sub> = 25°C			
			Typ	Limit		
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	3.3	0.3	0.5	V	50
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	3.3	−0.3	−0.5	V	50
V <sub>IHD</sub>	Minimum High Level Dynamic Input Voltage	3.3		2.0	V	50
V <sub>ILD</sub>	Maximum Low Level Dynamic Input Voltage	3.3		0.8	-V	50

Note: Input t<sub>r</sub> = t<sub>f</sub> = 3 ns**AC Electrical Characteristics:** See Section 2 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	74LVX74			74LVX74		Units	C <sub>L</sub> (pF)
			T <sub>A</sub> = +25°C			T <sub>A</sub> = −40°C to +85°C			
			Min	Typ	Max	Min	Max		
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay C <sub>P</sub> <sub>N</sub> to Q <sub>N</sub> or $\overline{Q}_N$	2.7	7.3	15	1.0	18.5	ns	15	
			9.8	18.5	1.0	22		50	
		3.3 ± 0.3	5.7	9.7	1.0	11.5	15		
			8.2	13.2	1.0	15	50		
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay $\overline{C}_D$ <sub>N</sub> to $\overline{S}_D$ <sub>N</sub> to Q <sub>N</sub> or $\overline{Q}_N$	2.7	8.4	15.6	1.0	18.5	ns	15	
			10.9	19.1	1.0	22		50	
		3.3 ± 0.3	6.6	10.1	1.0	12	15		
			9.1	13.6	1.0	15.5	50		
t <sub>W</sub>	C <sub>P</sub> <sub>N</sub> or $\overline{C}_D$ <sub>N</sub> or $\overline{S}_D$ <sub>N</sub> Pulse Width	2.7	8.5		10	ns			
		3.3 ± 0.3	6		7				
t <sub>S</sub>	Setup Time D <sub>N</sub> to C <sub>P</sub> <sub>N</sub>	2.7	8.0		9.5	ns			
		3.3 ± 0.3	5.5		6.5				
t <sub>H</sub>	Hold Time D <sub>N</sub> to C <sub>P</sub> <sub>N</sub>	2.7	0.5		0.5	ns			
		3.3 ± 0.3	0.5		0.5				
t <sub>rec</sub>	Recovery Time $\overline{C}_P$ <sub>N</sub> or $\overline{S}_D$ <sub>N</sub> to C <sub>P</sub> <sub>N</sub>	2.7	6.5		7.5	ns			
		3.3 ± 0.3	5.0		5.0				
f <sub>max</sub>	Maximum Clock Frequency	2.7	55	135	50		15		
			45	60	40	MHz	50		
		3.3 ± 0.3	95	145	80		15		
			60	85	50		50		
t <sub>OSLH</sub> , t <sub>OSHL</sub>	Output to Output Skew (Note 1)	2.7		1.5	1.5	ns	50		

Note 1: Parameter guaranteed by design. t<sub>OSLH</sub> = |t<sub>PLHm</sub> - t<sub>PLHn</sub>|, t<sub>OSHL</sub> = |t<sub>PHLm</sub> - t<sub>PHLl</sub>|

## Capacitance

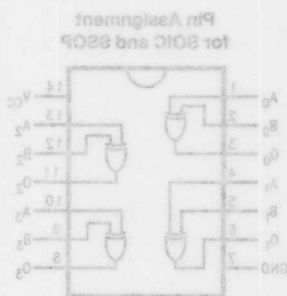
Symbol	Parameter	74LVX74			74LVX74		Units
		T <sub>A</sub> = + 25°C			T <sub>A</sub> = − 40°C to + 85°C		
		Min	Typ	Max	Min	Max	
C <sub>IN</sub>	Input Capacitance		4	10		10	pF
C <sub>PD</sub>	Power Dissipation Capacitance (Note 1)		25				pF

**Note 1:**  $C_{PD}$  is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:  $I_{CC(oper)} = \frac{C_{PD} \times V_{CC} \times f_{IN} + I_{CC}}{2}$  (per F/F)

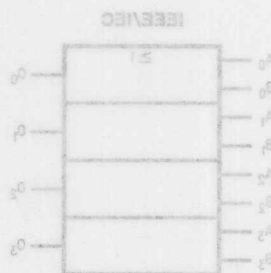
■ Guaranteed simultaneous switching noise level and dynamic threshold performance

### Connection Diagram



TLV111008-1

### Logic Symbol



TLV111008-2

Pin Name	Description
A0-A3	Inputs
B0-B3	Inputs
Q0-Q3	Outputs

Order Number	SOIC JEDEC	SOIC EIAJ	SSOP TYPE I
74LVX86M	74LVX86S1	74LVX86SX	74LVX86MSX
74LVX86MX	74LVX86SX	74LVX86MSX	74LVX86MSX
See NS Package Number	M14A	M14D	M8C14



## 74LVX86

### Low Voltage Quad 2-Input Exclusive-OR Gate

#### General Description

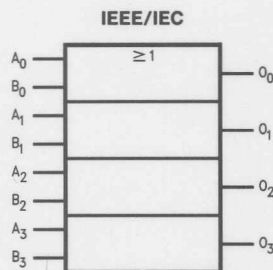
The LVX86 contains four 2-input exclusive-OR gates. The inputs tolerate voltages up to 7V allowing the interface of 5V systems to 3V systems.

#### Features

- Input voltage level translation from 5V to 3V
- Ideal for low power/low noise 3.3V applications
- Available in SOIC JEDEC, SOIC EIAJ and SSOP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance

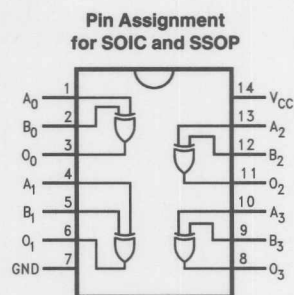
**Ordering Code:** See Section 11

#### Logic Symbol



TL/F/11605-2

#### Connection Diagram



TL/F/11605-1

Pin Names	Description
A <sub>0</sub> -A <sub>3</sub>	Inputs
B <sub>0</sub> -B <sub>3</sub>	Inputs
O <sub>0</sub> -O <sub>3</sub>	Outputs

	SOIC JEDEC	SOIC EIAJ	SSOP TYPE I
Order Number	74LVX86M 74LVX86MX	74LVX86SJ 74LVX86SJX	74LVX86MSCX
See NS Package Number	M14A	M14D	MSC14

**Absolute Maximum Ratings** (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )  $-0.5V$  to  $+7.0V$

DC Input Diode Current ( $I_{IK}$ )  
 $V_I = -0.5V$   $-20$  mA

DC Input Voltage ( $V_I$ )  $-0.5V$  to  $7V$

DC Output Diode Current ( $I_{OK}$ )  
 $V_O = -0.5V$   $-20$  mA  
 $V_O = V_{CC} + 0.5V$   $+20$  mA

DC Output Voltage ( $V_O$ )  $-0.5V$  to  $V_{CC} + 0.5V$

DC Output Source or Sink Current ( $I_O$ )  $\pm 25$  mA

DC  $V_{CC}$  or Ground Current ( $I_{CC}$  or  $I_{GND}$ )  $\pm 50$  mA

Storage Temperature ( $T_{STG}$ )  $-65^\circ C$  to  $+150^\circ C$

Power Dissipation  $180$  mW

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**DC Electrical Characteristics**

Symbol	Parameter	V <sub>CC</sub>	74LVX86			74LVX86		Units	Conditions	
			T <sub>A</sub> = +25°C			T <sub>A</sub> = -40°C to +85°C				
			Min	Typ	Max	Min	Max			
V <sub>IH</sub>	High Level Input Voltage	2.0	1.5			1.5		V		
		3.0	2.0			2.0				
		3.6	2.4			2.4				
V <sub>IL</sub>	Low Level Input Voltage	2.0			0.5		0.5	V		
		3.0			0.8		0.8			
		3.6			0.8		0.8			
V <sub>OH</sub>	High Level Output Voltage	2.0	1.9	2.0		1.9		V	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub>	I <sub>OH</sub> = -50 μA I <sub>OH</sub> = -50 μA I <sub>OH</sub> = -4 mA
		3.0	2.9	3.0		2.9				
		3.0	2.58			2.48				
V <sub>OL</sub>	Low Level Output Voltage	2.0		0.0	0.1		0.1	V	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub>	I <sub>OL</sub> = 50 μA I <sub>OL</sub> = 50 μA I <sub>OL</sub> = 4 mA
		3.0		0.0	0.1		0.1			
		3.0			0.36		0.44			
I <sub>IN</sub>	Input Leakage Current	3.6			±0.1		±1.0	μA	V <sub>IN</sub> = 5.5V or GND	
I <sub>CC</sub>	Quiescent Supply Current	3.6			2.0		20.0	μA	V <sub>IN</sub> = V <sub>CC</sub> or GND	

**Noise Characteristics:** See Section 2 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	74LVX86		Units	C <sub>L</sub> (pF)
			T <sub>A</sub> = 25°C			
			Typ	Limit		
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	3.3	0.3	0.5	V	50
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	3.3	−0.3	−0.5	V	50
V <sub>IHD</sub>	Minimum High Level Dynamic Input Voltage	3.3		2.0	V	50
V <sub>ILD</sub>	Maximum Low Level Dynamic Input Voltage	3.3		0.8	V	50

Note: (Input t<sub>r</sub> = t<sub>f</sub> = 3 ns)**AC Electrical Characteristics:** See Section 2 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	74LVX86			74LVX86		Units	C <sub>L</sub> (pF)
			T <sub>A</sub> = +25°C			T <sub>A</sub> = −40°C to +85°C			
			Min	Typ	Max	Min	Max		
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay Time	2.7		7.5	14.5	1.0	17.5		15
				10.0	18.0	1.0	21.0		50
		3.3 ± 0.3		5.8	9.3	1.0	11.0	ns	15
				8.3	12.8	1.0	14.5		50
t <sub>OSLH</sub> t <sub>OSHL</sub>	Output to Output Skew (Note 1)	2.7			1.5		1.5	ns	50

Note 1: Parameter guaranteed by design. t<sub>OSLH</sub> = |t<sub>PLHm</sub> - t<sub>PLHn</sub>|, t<sub>OSHL</sub> = |t<sub>PHLm</sub> - t<sub>PHLn</sub>|**Capacitance**

Symbol	Parameter	74LVX86			74LVX86		Units
		T <sub>A</sub> = +25°C			T <sub>A</sub> = −40°C to +85°C		
		Min	Typ	Max	Min	Max	
C <sub>IN</sub>	Input Capacitance		4	10		10	pF
C <sub>PD</sub>	Power Dissipation Capacitance (Note 1)		18				pF

Note 1: C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.Average operating current can be obtained by the equation:  $I_{CC(opr)} = \frac{C_{PD} \times V_{CC} \times f_{IN} + I_{CC}}{4 \text{ (per Gate)}}$ 

	V <sub>IN</sub> = 2.5V or GND	A <sub>IN</sub>	0.1 ±		0.1 ±			Input Leakage Current
	V <sub>IN</sub> = V <sub>CC</sub> or GND	A <sub>IN</sub>	0.0		0.0			Quiescent Supply Current



## 74LVX125

# Low-Voltage Quad Buffer with TRI-STATE® Outputs

### General Description

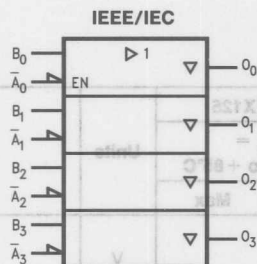
The LVX125 contains four independent non-inverting buffers with TRI-STATE outputs. The inputs tolerate voltages up to 7V allowing the interface of 5V systems to 3V systems.

### Features

- Input voltage level translation from 5V to 3V
- Ideal for low power/low noise 3.3V applications
- Available in SOIC JEDEC, SOIC EIAJ and SSOP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance

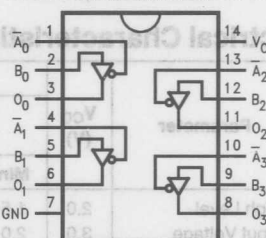
**Ordering Code:** See Section 11

### Logic Symbol



### Connection Diagram

**Pin Assignment for  
SOIC and SSOP**



### Truth Table

Pin Names		Description	
A <sub>n</sub> , B <sub>n</sub>		Inputs	
O <sub>n</sub>		Outputs	
Inputs		Output	
A <sub>n</sub>	B <sub>n</sub>	O <sub>n</sub>	
L	L	L	
L	H	H	
H	X	Z	

H = HIGH Voltage Level  
L = LOW Voltage Level  
Z = High Impedance  
X = Immaterial

	SOIC JEDEC	SOIC EIAJ	SSOP TYPE I
Order Number	74LVX125M 74LVX125MX	74LVX125SJ 74LVX125SJX	74LVX125MSCX
See NS Package Number	M14A	M14D	MSC14

## Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Input Diode Current ( $I_{IK}$ ) $V_I = -0.5V$	+20 mA
DC Input Voltage ( $V_I$ )	-0.5V to +7.0V
DC Output Diode Current ( $I_{OK}$ )	-20 mA
$V_O = 0.5V$	+20 mA
$V_O = V_{CC} + 0.5V$	-0.5V to $V_{CC} + 0.5V$
Output Voltage ( $V_O$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Source/Sink Current ( $I_O$ )	$\pm 25$ mA
DC $V_{CC}$ or Ground Current ( $I_{CC}$ or $I_{GND}$ )	$\pm 50$ mA
Storage Temp. Range ( $T_{STG}$ )	-65°C to +150°C
Power Dissipation	180 mW

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## Recommended Operating Conditions

Supply Voltage ( $V_{CC}$ )	2.0V to 3.6V
Input Voltage ( $V_I$ )	0V to 5.5V
Output Voltage ( $V_O$ )	0V to $V_{CC}$
Operating Temperature ( $T_A$ )	-40°C to +85°C
Input Rise and Fall Time ( $\Delta t/\Delta v$ )	0 ns/V to 100 ns/V

## DC Electrical Characteristics

Symbol	Parameter	V <sub>CC</sub> (V)	74LVX125			74LVX125		Units	Conditions	
			T <sub>A</sub> = 25°C			T <sub>A</sub> = −40°C to +85°C				
			Min	Typ	Max	Min	Max			
V <sub>IH</sub>	High Level Input Voltage	2.0 3.0 3.6	1.5 2.0 2.4			1.5 2.0 2.4		V		
V <sub>IL</sub>	Low Level Input Voltage	2.0 3.0 3.6		0.5 0.8 0.8		0.5 0.8 0.8		V		
V <sub>OH</sub>	High Level Output Voltage	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0		1.9 2.9 2.48		V	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub>	I <sub>OH</sub> = −50 μA I <sub>OH</sub> = −50 μA I <sub>OH</sub> = −4 mA
V <sub>OL</sub>	Low Level Output Voltage	2.0 3.0 3.0		0.0 0.0 0.36		0.1 0.1 0.44		V	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub>	I <sub>OL</sub> = 50 μA I <sub>OL</sub> = 50 μA I <sub>OL</sub> = 4 mA
I <sub>OZ</sub>	TRI-STATE Output Off-State Current	3.6		±0.25		±2.5		μA	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>OUT</sub> = V <sub>CC</sub> or GND	
I <sub>IN</sub>	Input Leakage Current	3.6		±0.1		±1.0		μA	V <sub>IN</sub> = 5.5V or GND	
I <sub>CC</sub>	Quiescent Supply Current	3.6		4.0		40.0		μA	V <sub>IH</sub> = V <sub>CC</sub> or GND	

Order Number	74LVX125M	74LVX125J	74LVX125L
See NS Package Number	M14A	M14D	M14C

**Noise Characteristics:** See Section 2 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	74LVX125		Units	C <sub>L</sub> (pF)
			T <sub>A</sub> = 25°C			
			Typ	Limit		
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	3.3	0.3	0.8	V	50
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	3.3	−0.3	−0.8	V	50
V <sub>IHD</sub>	Minimum High Level Dynamic Input Voltage	3.3		2.0	V	50
V <sub>ILD</sub>	Maximum Low Level Dynamic Input Voltage	3.3		0.8	V	50

Note: Input  $t_r = t_f = 3$  ns.**AC Electrical Characteristics:** See Section 2 Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	74LVX125			74LVX125		Units	Conditions
			T <sub>A</sub> = +25°C			T <sub>A</sub> = −40°C to +85°C			
			Min	Typ	Max	Min	Max		
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay Time Data to Output	2.7		5.8	10.1	1.0	13.5	ns	C <sub>L</sub> = 15 pF
				8.3	13.6	1.0	17.0		C <sub>L</sub> = 50 pF
		3.3 ± 0.3		4.4	6.2	1.0	8.5		C <sub>L</sub> = 15 pF
				6.9	9.7	1.0	12.0		C <sub>L</sub> = 50 pF
t <sub>PZH</sub> , t <sub>PZL</sub>	Output Enable Time	2.7		5.3	9.3	1.0	12.5	ns	C <sub>L</sub> = 15 pF, R <sub>L</sub> = 1 kΩ
				7.8	12.8	1.0	16.0		C <sub>L</sub> = 50 pF, R <sub>L</sub> = 1 kΩ
		3.3 ± 0.3		4.0	5.6	1.0	7.5		C <sub>L</sub> = 15 pF, R <sub>L</sub> = 1 kΩ
				6.5	9.1	1.0	11.0		C <sub>L</sub> = 50 pF, R <sub>L</sub> = 1 kΩ
t <sub>PHZ</sub> , t <sub>PLZ</sub>	Output Disable Time	2.7		10.0	15.7	1.0	19.0	ns	C <sub>L</sub> = 50 pF, R <sub>L</sub> = 1 kΩ
		3.3 ± 0.3		8.3	11.2	1.0	13.0		C <sub>L</sub> = 50 pF, R <sub>L</sub> = 1 kΩ
t <sub>OSSL</sub> , t <sub>OSLH</sub>	Output to Output Skew (Note 1)	2.7			1.5		1.5	ns	C <sub>L</sub> = 50 pF

Note 1: Parameter guaranteed by design.  $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$ ,  $t_{OSSL} = |t_{PHLm} - t_{PHLn}|$ **Capacitance**

Symbol	Parameter	74LVX125			74LVX125		Units
		T <sub>A</sub> = 25°C			T <sub>A</sub> = −40°C to +85°C		
		Min	Typ	Max	Min	Max	
C <sub>IN</sub>	Input Capacitance		4.0	10		10	pF
C <sub>PD</sub>	Power Dissipation Capacitance (Note 1)		14				pF

Note 1: C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumptionwithout load. Average operating current can be obtained by the equation:  $I_{CC(opr)} = \frac{C_{PD} \times V_{CC} \times f_{IN} + I_{CC}}{4}$  (per bit)

Order Number	74LVX125M	74LVX125J	74LVX125P	74LVX125T
See NS Package Number	M18A	M18D	M18C	M18E



## 74LVX138

### Low Voltage 1-of-8 Decoder/Demultiplexer

#### General Description

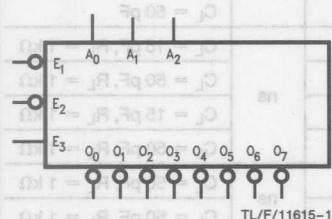
The LVX138 is a high-speed 1-of-8 decoder/demultiplexer. This device is ideally suited for high-speed bipolar memory chip select address decoding. The multiple input enables allow parallel expansion to a 1-of-24 decoder using just three LVX138 devices or a 1-of-32 decoder using four LVX138 devices and one inverter.

#### Features

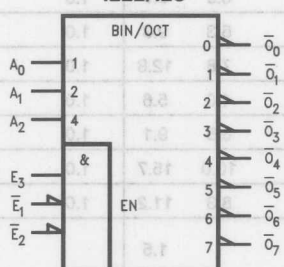
- Input voltage level translation from 5V to 3V
- Ideal for low power/low noise 3.3V applications
- Available in SOIC JEDEC, SOIC EIAJ and SSOP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance

#### Ordering Code: See Section 11

#### Logic Symbols

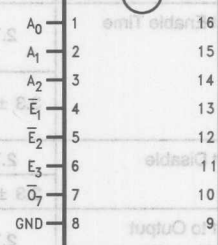


#### IEEE/IEC



#### Connection Diagram

##### Pin Assignment for SOIC and SSOP



Pin Names	Description
A <sub>0</sub> -A <sub>2</sub>	Address Inputs
E <sub>1</sub> -E <sub>2</sub>	Enable Inputs
E <sub>3</sub>	Enable Input
O <sub>0</sub> -O <sub>7</sub>	Outputs

	SOIC JEDEC	SOIC EIAJ	SSOP TYPE I
Order Number	74LVX138M 74LVX138MX	74LVX138SJ 74LVX138SJX	74LVX138MSCX
See NS Package Number	M16A	M16D	MSC16

## Functional Description

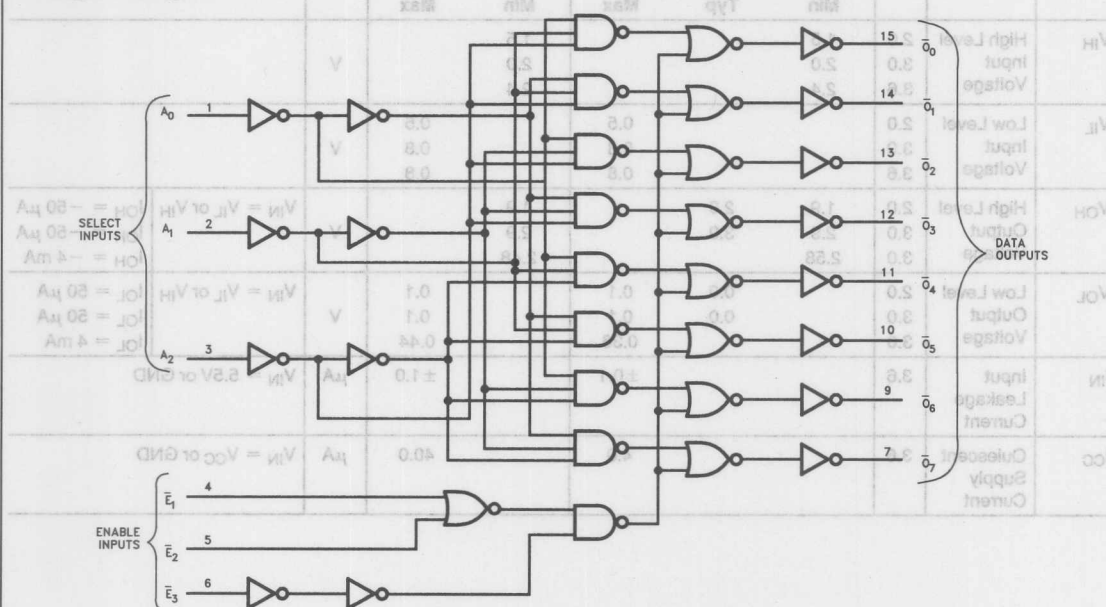
The LVX138 high-speed 1-of-8 decoder/demultiplexer accepts three binary weighted inputs ( $A_0$ ,  $A_1$ ,  $A_2$ ) and, when enabled, provides eight mutually exclusive active-LOW outputs ( $\bar{O}_0$ – $\bar{O}_7$ ). The LVX138 features three Enable inputs, two active-LOW ( $\bar{E}_1$ ,  $\bar{E}_2$ ) and one active-HIGH ( $E_3$ ). All outputs will be HIGH unless  $\bar{E}_1$  and  $\bar{E}_2$  are LOW and  $E_3$  is HIGH.

## Truth Table

Inputs						Outputs							
$\bar{E}_1$	$\bar{E}_2$	$E_3$	$A_0$	$A_1$	$A_2$	$\bar{O}_0$	$\bar{O}_1$	$\bar{O}_2$	$\bar{O}_3$	$\bar{O}_4$	$\bar{O}_5$	$\bar{O}_6$	$\bar{O}_7$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial

## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

TL/F/11615-4

**Absolute Maximum Ratings** (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )  $-0.5V$  to  $+7.0V$

DC Input Diode Current ( $I_{IK}$ )  
 $V_I = -0.5V$   $-20\text{ mA}$

DC Input Voltage ( $V_I$ )  $-0.5V$  to  $7V$

DC Output Diode Current ( $I_{OK}$ )  
 $V_O = -0.5V$   $-20\text{ mA}$   
 $V_O = V_{CC} + 0.5V$   $+20\text{ mA}$

DC Output Voltage ( $V_O$ )  $-0.5V$  to  $V_{CC} + 0.5V$

DC Output Source or Sink Current ( $I_O$ )  $\pm 25\text{ mA}$

DC  $V_{CC}$  or Ground Current ( $I_{CC}$  or  $I_{GND}$ )  $\pm 75\text{ mA}$

Storage Temperature ( $T_{STG}$ )  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$

Power Dissipation  $180\text{ mW}$

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Recommended Operating Conditions**

Supply Voltage ( $V_{CC}$ )  $2.0V$  to  $3.6V$

Input Voltage ( $V_I$ )  $0V$  to  $5.5V$

Output Voltage ( $V_O$ )  $0V$  to  $V_{CC}$

Operating Temperature ( $T_A$ )  $40^\circ\text{C}$  to  $+85^\circ\text{C}$

Input Rise and Fall Time ( $\Delta t_r/\Delta t_f$ )  $0\text{ ns/V}$  to  $100\text{ ns/V}$

**DC Electrical Characteristics**

Symbol	Parameter	V <sub>CC</sub>	74LVX138			74LVX138		Units	Conditions
			T <sub>A</sub> = +25°C			T <sub>A</sub> = -40°C to +85°C			
			Min	Typ	Max	Min	Max		
V <sub>IH</sub>	High Level Input Voltage	2.0 3.0 3.6	1.5 2.0 2.4			1.5 2.0 2.4		V	
V <sub>IL</sub>	Low Level Input Voltage	2.0 3.0 3.6			0.5 0.8 0.8		0.5 0.8 0.8	V	
V <sub>OH</sub>	High Level Output Voltage	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0		1.9 2.9 2.48		V	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OH</sub> = -50 μA I <sub>OH</sub> = -50 μA I <sub>OH</sub> = -4 mA
V <sub>OL</sub>	Low Level Output Voltage	2.0 3.0 3.0		0.0 0.0	0.1 0.1 0.36		0.1 0.1 0.44	V	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OL</sub> = 50 μA I <sub>OL</sub> = 50 μA I <sub>OL</sub> = 4 mA
I <sub>IN</sub>	Input Leakage Current	3.6			±0.1		±1.0	μA	V <sub>IN</sub> = 5.5V or GND
I <sub>CC</sub>	Quiescent Supply Current	3.6			4.0		40.0	μA	V <sub>IN</sub> = V <sub>CC</sub> or GND

Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = 25°C		Units	V <sub>L</sub> (pF)
			Typ	Limit		
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	3.3	0.3	0.5	V	50
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	3.3	-0.3	-0.5	V	50
V <sub>IHD</sub>	Minimum High Level Dynamic Input Voltage	3.3		2.0	V	50
V <sub>ILD</sub>	Maximum Low Level Dynamic Input Voltage	3.3		0.8	V	50

Note: Input  $t_r = t_f = 3$  ns

## AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	74LVX138			74LVX138		Units	C <sub>L</sub> (pF)
			T <sub>A</sub> = +25°C			T <sub>A</sub> = −40°C to +85°C			
			Min	Typ	Max	Min	Max		
t <sub>PLH</sub>	Propagation Delay Time A <sub>n</sub> to $\overline{O}_n$	2.7		7.1	13.8	1.0	16.5	ns	15
t <sub>PHL</sub>				9.6	17.3	1.0	20.0		50
		3.3 ± 0.3		5.5	8.8	1.0	10.5		15
				8.0	12.3	1.0	14.0		50
t <sub>PLH</sub>	Propagation Delay Time E <sub>1</sub> or E <sub>2</sub> to $\overline{O}_n$	2.7		8.8	16.0	1.0	18.5	ns	15
t <sub>PHL</sub>				11.3	19.5	1.0	22.0		50
		3.3 ± 0.3		6.9	10.4	1.0	11.5		15
				9.4	13.9	1.0	15.0		50
t <sub>PLH</sub>	Propagation Delay Time E <sub>3</sub> to $\overline{O}_n$	2.7		8.7	16.3	1.0	19.5	ns	15
t <sub>PHL</sub>				11.2	19.8	1.0	23.0		50
		3.3 ± 0.3		6.8	10.6	1.0	12.5		15
				9.3	14.1	1.0	16.0		50
t <sub>OSHL</sub>	Output to Output Skew (Note 1)	2.7						ns	50
t <sub>OSLH</sub>			1.5			1.5			

Note 1: Parameter guaranteed by design.  $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$ ,  $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$

## Capacitance

Symbol	Parameter	74LVX138			74LVX138		Units
		T <sub>A</sub> = +25°C			T <sub>A</sub> = −40°C to +85°C		
		Min	Typ	Max	Min	Max	
C <sub>IN</sub>	Input Capacitance		4	10		10	pF
C <sub>PD</sub>	Power Dissipation Capacitance (Note 1)		34				pF

Note 1: C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:  $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}$



# 74LVX157

## Low Voltage Quad 2-Input Multiplexer

### General Description

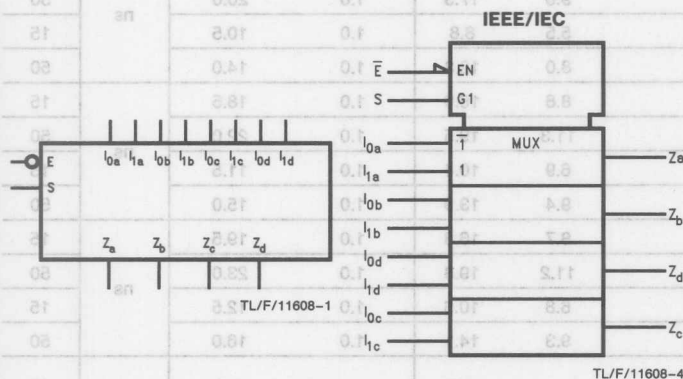
The LVX157 is a high-speed quad 2-input multiplexer. Four bits of data from two sources can be selected using the common Select and Enable inputs. The four outputs present the selected data in the true (noninverted) form. The LVX157 can also be used as a function generator.

### Features

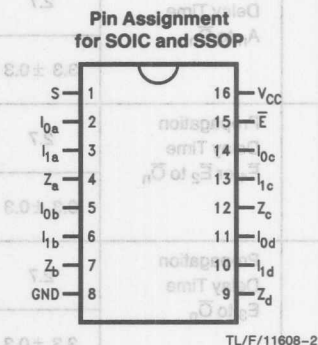
- Input voltage level translation from 5V to 3V
- Ideal for low power/low noise 3.3V applications
- Available in SOIC JEDEC, SOIC EIAJ and SSOP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance

**Ordering Code:** See Section 11

### Logic Symbols



### Connection Diagram



Pin Names	Description
I <sub>0a</sub> -I <sub>0d</sub>	Source 0 Data Inputs
I <sub>1a</sub> -I <sub>1d</sub>	Source 1 Data Inputs
$\bar{E}$	Enable Input
S	Select Input
Z <sub>a</sub> -Z <sub>d</sub>	Outputs

	SOIC JEDEC	SOIC EIAJ	SSOP TYPE I
Order Number	74LVX157M 74LVX157MX	74LVX157SJ 74LVX157SJJ	74LVX157MSCX
See NS Package Number	M16A	M16D	MSC16

## Functional Description

The LVX157 is a quad 2-input multiplexer. It selects four bits of data from two sources under the control of a common Select input (S). The Enable input (E) is active-LOW. When  $\bar{E}$  is HIGH, all of the outputs (Z) are forced LOW regardless of all other inputs. The LVX157 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

$$Z_a = \bar{E} \cdot (I_{1a} \cdot S + I_{0a} \cdot \bar{S})$$

$$Z_b = \bar{E} \cdot (I_{1b} \cdot S + I_{0b} \cdot \bar{S})$$

$$Z_c = \bar{E} \cdot (I_{1c} \cdot S + I_{0c} \cdot \bar{S})$$

$$Z_d = \bar{E} \cdot (I_{1d} \cdot S + I_{0d} \cdot \bar{S})$$

A common use of the LVX157 is the moving of data from two groups of registers to four common output busses. The particular register from which the data comes is determined by the state of the Select input. A less obvious use is as a function generator. The LVX157 can generate any four of the sixteen different functions of two variables with one variable common. This is useful for implementing gating functions.

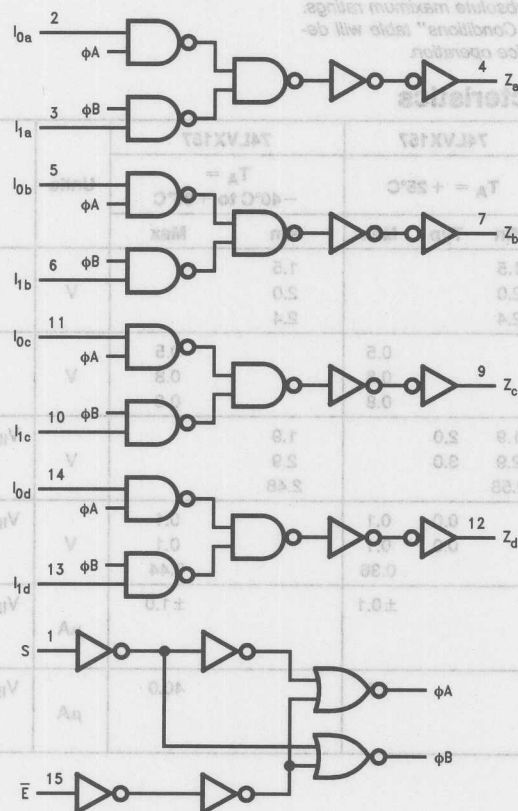
## Truth Table

Inputs				Outputs
$\bar{E}$	S	$I_0$	$I_1$	Z
H	X	X	X	L
L	H	X	X	L
L	H	H	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial



TL/F/11608-3

## Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )	X	-0.5V to +7.0V
DC Input Diode Current ( $I_{IK}$ )	X	-20 mA
$V_I = -0.5V$	X	-0.5V to 7V
DC Input Voltage ( $V_I$ )	X	-20 mA
DC Output Diode Current ( $I_{OK}$ )	X	+20 mA
$V_O = -0.5V$	X	-0.5V to $V_{CC} + 0.5V$
$V_O = V_{CC} + 0.5V$	X	±25 mA
DC Output Voltage ( $V_O$ )	X	±50 mA
DC Output Source or Sink Current ( $I_O$ )	X	-65°C to +150°C
DC $V_{CC}$ or Ground Current ( $I_{CC}$ or $I_{GND}$ )	X	180 mW
Storage Temperature ( $T_{STG}$ )	X	
Power Dissipation	X	

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## DC Electrical Characteristics

Symbol	Parameter	V <sub>CC</sub>	74LVX157			74LVX157		Units	Conditions	
			T <sub>A</sub> = +25°C			T <sub>A</sub> = −40°C to +85°C				
			Min	Typ	Max	Min	Max			
V <sub>IH</sub>	High Level Input Voltage	2.0	1.5			1.5		V		
		3.0	2.0			2.0				
		3.6	2.4			2.4				
V <sub>IL</sub>	Low Level Input Voltage	2.0			0.5		0.5	V		
		3.0			0.8		0.8			
		3.6			0.8		0.8			
V <sub>OH</sub>	High Level Output Voltage	2.0	1.9	2.0		1.9		V	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub>	I <sub>OH</sub> = −50 μA I <sub>OH</sub> = −50 μA I <sub>OH</sub> = −4 mA
		3.0	2.9	3.0		2.9				
		3.0	2.58			2.48				
V <sub>OL</sub>	Low Level Output Voltage	2.0	0.0	0.1		0.1		V	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub>	I <sub>OL</sub> = 50 μA I <sub>OL</sub> = 50 μA I <sub>OL</sub> = 4 mA
		3.0	0.0	0.1		0.1				
		3.0		0.36		0.44				
I <sub>IN</sub>	Input Leakage Current	3.6			±0.1		±1.0	μA	V <sub>IN</sub> = 5.5V or GND	
I <sub>CC</sub>	Quiescent Supply Current	3.6			4.0		40.0	μA	V <sub>IN</sub> = V <sub>CC</sub> or GND	

## Recommended Operating Conditions

Supply Voltage ( $V_{CC}$ )	2.0V to 3.6V
Input Voltage ( $V_I$ )	0V to 5.5V
Output Voltage ( $V_O$ )	0V to $V_{CC}$
Operating Temperature ( $T_A$ )	-40°C to +85°C
Input Rise and Fall Time ( $\Delta t_r/\Delta t_f$ )	0 ns/V to 100 ns/V

**Noise Characteristics:** See Section 2 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	74LVX157		Units	C <sub>L</sub> (pF)
			T <sub>A</sub> = 25°C			
			Typ	Limit		
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	3.3	0.3	0.5	V	50
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	3.3	−0.3	−0.5	V	50
V <sub>IHD</sub>	Minimum High Level Dynamic Input Voltage	3.3		2.0	V	50
V <sub>ILD</sub>	Maximum Low Level Dynamic Input Voltage	3.3		0.8	V	50

Note: (Input t<sub>r</sub> = t<sub>f</sub> = 3 ns)**AC Electrical Characteristics:** See Section 2 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	74LVX157			74LVX157		Units	C <sub>L</sub> (pF)
			T <sub>A</sub> = +25°C			T <sub>A</sub> = −40°C to +85°C			
			Min	Typ	Max	Min	Max		
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay Time I <sub>n</sub> to Z <sub>n</sub>	2.7		6.6	12.5	1.0	15.5	ns	15
				9.1	16.0	1.0	19.0		50
		3.3 ± 0.3		5.1	7.9	1.0	9.5		15
				7.6	11.4	1.0	13.0		50
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay Time S to Z <sub>n</sub>	2.7		8.9	16.9	1.0	20.5	ns	15
				11.4	20.4	1.0	24.0		50
		3.3 ± 0.3		7.0	11.0	1.0	13.0		15
				9.5	14.5	1.0	16.5		50
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay Time E to Z <sub>n</sub>	2.7		9.1	17.6	1.0	20.5	ns	15
				11.6	21.1	1.0	24.0		50
		3.3 ± 0.3		7.2	11.5	1.0	13.5		15
				9.7	15.0	1.0	17.0		50
t <sub>OSHL</sub> , t <sub>OSLH</sub>	Output to Output Skew (Note 1)	2.7			1.5		1.5	ns	50

Note 1: Parameter guaranteed by design. t<sub>OSLH</sub> = |t<sub>PLHm</sub> - t<sub>PLHn</sub>|.  
t<sub>OSHL</sub> = |t<sub>PHLm</sub> - t<sub>PHLn</sub>|.

**Capacitance**

Symbol	Parameter	74LVX157			74LVX157		Units
		T <sub>A</sub> = +25°C			T <sub>A</sub> = −40°C to +85°C		
		Min	Typ	Max	Min	Max	
C <sub>IN</sub>	Input Capacitance		4	10		10	pF
C <sub>PD</sub>	Power Dissipation Capacitance (Note 1)		20				pF

Note 1: C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation: I<sub>CC(opr)</sub> = C<sub>PD</sub> × V<sub>CC</sub> × f<sub>IN</sub> + I<sub>CC</sub>



## 74LVX174

### Low Voltage Hex D Flip-Flop with Master Reset

#### General Description

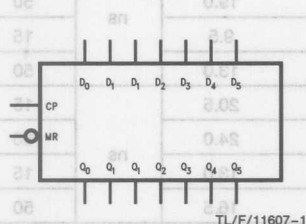
The LVX174 is a high-speed hex D flip-flop. The device is used primarily as a 6-bit edge-triggered storage register. The information on the D inputs is transferred to storage during the LOW-to-HIGH clock transition. The device has a Master Reset to simultaneously clear all flip-flops.

#### Features

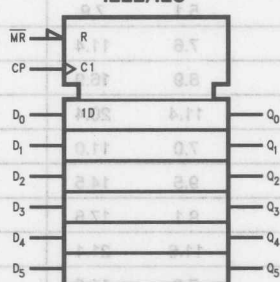
- Input voltage level translation from 5V to 3V
- Ideal for low power/low noise 3.3V applications
- Available in SOIC JEDEC, SOIC EIAJ and SSOP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance

**Ordering Code:** See Section 11

#### Logic Symbols



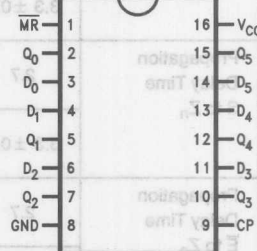
IEEE/IEC



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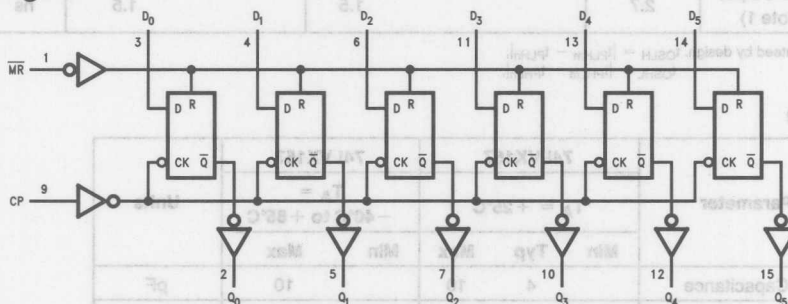
#### Connection Diagram

Pin Assignment for  
SOIC and SSOP



TL/F/11607-2

#### Logic Diagram



TL/F/11607-3

Pin Names	Description
D <sub>0</sub> -D <sub>5</sub>	Data Inputs
CP	Clock Pulse Input
MR	Master Reset Input
Q <sub>0</sub> -Q <sub>5</sub>	Outputs

	SOIC JEDEC	SOIC EIAJ	SSOP TYPE I
Order Number	74LVX174M 74LVX174MX	74LVX174SJ 74LVX174SJX	74LVX174MSCX
See NS Package Number	M16A	M16D	MSC16

**Absolute Maximum Ratings** (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )  $-0.5V$  to  $+7.0V$

DC Input Diode Current ( $I_{IK}$ )  $-20$  mA  
 $V_I = -0.5V$

DC Input Voltage ( $V_I$ )  $-0.5V$  to  $7V$

DC Output Diode Current ( $I_{OK}$ )  $-20$  mA  
 $V_O = -0.5V$   
 $V_O = V_{CC} + 0.5V$   $+20$  mA

DC Output Voltage ( $V_O$ )  $-0.5V$  to  $V_{CC} + 0.5V$

DC Output Source or Sink Current ( $I_O$ )  $\pm 25$  mA

DC  $V_{CC}$  or Ground Current ( $I_{CC}$  or  $I_{GND}$ )  $\pm 50$  mA

Storage Temperature ( $T_{STG}$ )  $-65^\circ C$  to  $+150^\circ C$

Power Dissipation ( $P_D$ )  $180$  mW

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**DC Electrical Characteristics**

Symbol	Parameter	V <sub>CC</sub>	74LVX174			74LVX174		Units	Conditions
			T <sub>A</sub> = +25°C			T <sub>A</sub> = −40°C to +85°C			
			Min	Typ	Max	Min	Max		
V <sub>IH</sub>	High Level Input Voltage	2.0	1.5		1.5		V		
		3.0	2.0		2.0				
		3.6	2.4		2.4				
V <sub>IL</sub>	Low Level Input Voltage	2.0		0.5		0.5	V		
		3.0		0.8		0.8			
		3.6		0.8		0.8			
V <sub>OH</sub>	High Level Output Voltage	2.0	1.9	2.0	1.9		V	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OH</sub> = −50 μA I <sub>OH</sub> = −50 μA I <sub>OH</sub> = −4 mA	
		3.0	2.9	3.0	2.9				
		3.0	2.58		2.48				
V <sub>OL</sub>	Low Level Output Voltage	2.0		0.0	0.1	0.1	V	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OL</sub> = 50 μA I <sub>OL</sub> = 50 μA I <sub>OL</sub> = 4 mA	
		3.0		0.0	0.1	0.1			
		3.0		0.36		0.44			
I <sub>IN</sub>	Input Leakage Current	3.6			±0.1	±1.0	μA	V <sub>IN</sub> = 5.5V or GND	
I <sub>CC</sub>	Quiescent Supply Current	3.6			4.0	40.0	μA	V <sub>IN</sub> = V <sub>CC</sub> or GND	

**Recommended Operating Conditions**

Supply Voltage ( $V_{CC}$ )  $2.0V$  to  $3.6V$

Input Voltage ( $V_I$ )  $0V$  to  $5.5V$

Output Voltage ( $V_O$ )  $0V$  to  $V_{CC}$

Operating Temperature ( $T_A$ )  $-40^\circ C$  to  $+85^\circ C$

Input Rise and Fall Time ( $\Delta t/\Delta V$ )  $0$  ns/V to  $100$  ns/V

**Noise Characteristics:** See Section 2 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	74LVX174		Units	C <sub>L</sub> (pF)
			T <sub>A</sub> = 25°C			
			Typ	Limit		
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	3.3	0.3	0.5	V	50
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	3.3	−0.3	−0.5	V	50
V <sub>IHD</sub>	Minimum High Level Dynamic Input Voltage	3.3		2.0	V	50
V <sub>ILD</sub>	Maximum Low Level Dynamic Input Voltage	3.3		0.8	V	50

Note: (Input t<sub>r</sub> = t<sub>f</sub> = 3 ns)**AC Electrical Characteristics:** See Section 2 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	74LVX174			74LVX174		Units	C <sub>L</sub> (pF)
			T <sub>A</sub> = +25°C			T <sub>A</sub> = −40°C to +85°C			
			Min	Typ	Max	Min	Max		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Time CP to Q <sub>n</sub>	2.7		7.6	14.5	1.0	17.5		15
				10.1	18.0	1.0	21.0		50
		3.3 ± 0.3		5.9	9.3	1.0	11.0	ns	15
				8.4	12.8	1.0	14.5		50
t <sub>PHL</sub>	Propagation Delay MR to Q <sub>n</sub>	2.7		7.9	15.0	1.0	18.5		15
				10.4	18.5	1.0	22.0		50
		3.3 ± 0.3		6.2	9.7	1.0	11.5	ns	15
				8.7	13.2	1.0	15.0		50
t <sub>S</sub>	Setup Time D <sub>n</sub> to CP	2.7	7.5		8.5			ns	
		3.3 ± 0.3	5.0		6.0				
t <sub>H</sub>	Hold Time D <sub>n</sub> to CP	2.7	0		0			ns	
		3.3 ± 0.3	0		0				
t <sub>REM</sub>	Removal Time MR to CP	2.7	4.5		4.5			ns	
		3.3 ± 0.3	3.0		3.0				
t <sub>W</sub>	Clock Pulse Width	2.7	6.5		7.5			ns	
		3.3 ± 0.3	5.0		5.0				
t <sub>W</sub>	MR Pulse Width	2.7	6.5		7.5			ns	
		3.3 ± 0.3	5.0		5.0				
f <sub>MAX</sub>	Maximum Clock Frequency	2.7	65	130		55		MHz	15
			45	60		40			50
		3.3 ± 0.3	115	180		95		15	
			65	95		55		50	
t <sub>OSLH</sub> t <sub>OSHL</sub>	Output to Output Skew (Note 1)	2.7		1.5		1.5	ns	50	

Note 1: Parameter guaranteed by design. t<sub>OSLH</sub> = |t<sub>PLHm</sub> - t<sub>PLHn</sub>|, t<sub>OSHL</sub> = |t<sub>PHLm</sub> - t<sub>PHLn</sub>|**Capacitance**

Symbol	Parameter	74LVX174			74LVX174		Units
		T <sub>A</sub> = +25°C			T <sub>A</sub> = -40°C to +85°C		
		Min	Typ	Max	Min	Max	
C <sub>IN</sub>	Input Capacitance		4	10		10	pF
C <sub>PD</sub>	Power Dissipation Capacitance (Note 1)		29				pF

Note 1: C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.Average operating current can be obtained by the equation:  $I_{CC(opr)} = \frac{C_{PD} \times V_{CC} \times f_{IN} + I_{CC}}{4 \text{ (per F/F)}}$

## 74LVX240

Low Voltage Octal Buffer/Line Driver  
with TRI-STATE® Outputs

## General Description

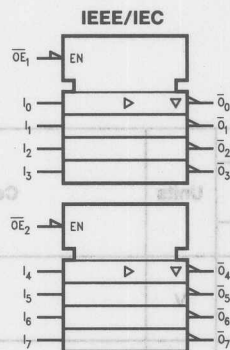
The LVX240 is an octal inverting buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter or receiver which provides improved PC board density. The inputs tolerate up to 7V allowing interface of 5V systems to 3V systems.

## Features

- Input voltage translation from 5V to 3V
- Ideal for low power/low noise 3.3V applications
- Available in SOIC JEDEC, SOIC EIAJ and SSOP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance

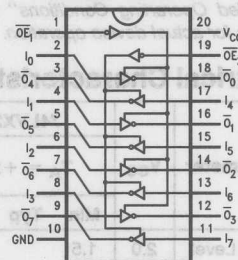
**Ordering Code:** See Section 11

## Logic Symbol



TL/F/11609-2

## Connection Diagram

Pin Assignment  
for SOIC and SSOP

TL/F/11609-1

Pin Names	Description
$\overline{OE}_1, \overline{OE}_2$	TRI-STATE Output Enable Inputs
$I_0-I_7$	Inputs
$O_0-O_7$	Outputs

## Truth Tables

Inputs		Outputs (Pins 12, 14, 16, 18)	
$\overline{OE}_1$	$I_n$		
L	L	H	
L	H	L	
H	X	Z	

Inputs		Outputs (Pins 3, 5, 7, 9)	
$\overline{OE}_2$	$I_n$		
L	L	H	
L	H	L	
H	X	Z	

H = HIGH Voltage Level L = LOW Voltage Level X = Immaterial Z = High Impedance

	SOIC JEDEC	SOIC EIAJ	SSOP TYPE I
Order Number	74LVX240M 74LVX240MX	74LVX240SJ 74LVX240SJX	74LVX240MSCX
See NS Package Number	M20B	M20D	MSC20

## Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Input Diode Current ( $I_{IK}$ )	-20 mA
$V_I = -0.5V$	-0.5V to 7V
DC Input Voltage ( $V_I$ )	-0.5V to 7V
DC Output Diode Current ( $I_{OK}$ )	-20 mA
$V_O = -0.5V$	+20 mA
$V_O = V_{CC} + 0.5V$	-0.5V to $V_{CC} + 0.5V$
DC Output Voltage ( $V_O$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Source or Sink Current ( $I_O$ )	$\pm 25$ mA
DC $V_{CC}$ or Ground Current ( $I_{CC}$ or $I_{GND}$ )	$\pm 75$ mA
Storage Temperature ( $T_{STG}$ )	-65°C to +150°C
Power Dissipation ( $P_D$ )	180 mW

Note: Absolute Maximum Ratings are those values beyond which the safety to the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## Recommended Operating Conditions

Supply Voltage ( $V_{CC}$ )	2.0V to 3.6V
Input Voltage ( $V_I$ )	0V to 5.5V
Output Voltage ( $V_O$ )	0V to $V_{CC}$
Operating Temperature ( $T_A$ )	-40°C to +85°C
Input Rise and Fall Time ( $\Delta t/\Delta V$ )	0 ns/V to 100 ns/V

## DC Electrical Characteristics

Symbol	Parameter	V <sub>CC</sub>	74LVX240			74LVX240		Units	Conditions	
			T <sub>A</sub> = +25°C			T <sub>A</sub> = −40°C to +85°C				
			Min	Typ	Max	Min	Max			
V <sub>IH</sub>	High Level Input Voltage	2.0 3.0 3.6	1.5 2.0 2.4			1.5 2.0 2.4		V		
V <sub>IL</sub>	Low Level Input Voltage	2.0 3.0 3.6			0.5 0.8 0.8		0.5 0.8 0.8	V		
V <sub>OH</sub>	High Level Output Voltage	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0		1.9 2.9 2.48		V	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>OH</sub> = −50 μA I <sub>OH</sub> = −50 μA I <sub>OH</sub> = −4 mA	
V <sub>OL</sub>	Low Level Output Voltage	2.0 3.0 3.0		0.0 0.0 0.36	0.1 0.1		0.1 0.1 0.44	V	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>OL</sub> = 50 μA I <sub>OL</sub> = 50 μA I <sub>OL</sub> = 4 mA	
I <sub>OZ</sub>	TRI-STATE Output Off-State Current	3.6		±0.25		±2.5		μA	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>OUT</sub> = V <sub>CC</sub> or GND	
I <sub>IN</sub>	Input Leakage Current	3.6		±0.1		±1.0		μA	V <sub>IN</sub> = 5.5V or GND	
I <sub>CC</sub>	Quiescent Supply Current	3.6		4.0		40.0		μA	V <sub>IN</sub> = V <sub>CC</sub> or GND	

**Noise Characteristics:** See Section 2 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	74LVX240		Units	C <sub>L</sub> (pF)
			T <sub>A</sub> = 25°C			
			Typ	Limit		
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	3.3	0.5	0.8	V	50
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	3.3	−0.5	−0.8	V	50
V <sub>IHD</sub>	Minimum High Level Dynamic Input Voltage	3.3		2.0	V	50
V <sub>ILD</sub>	Maximum Low Level Dynamic Input Voltage	3.3		0.8	V	50

Note: (Input t<sub>r</sub> = t<sub>f</sub> = 3 ns)**AC Electrical Characteristics:** See Section 2 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	74LVX240			74LVX240		Units	Conditions
			T <sub>A</sub> = +25°C			T <sub>A</sub> = −40°C to +85°C			
			Min	Typ	Max	Min	Max		
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay Time	2.7		5.7	10.1	1.0	12.5	ns	C <sub>L</sub> = 15 pF
				8.2	13.6	1.0	16.0		C <sub>L</sub> = 50 pF
		3.3 ± 0.3		4.3	6.2	1.0	7.5		C <sub>L</sub> = 15 pF
				6.8	9.7	1.0	11.0		C <sub>L</sub> = 50 pF
t <sub>pZL</sub> , t <sub>pZH</sub>	TRI-STATE Output Enable Time	2.7		7.1	13.8	1.0	16.5	ns	C <sub>L</sub> = 15 pF, R <sub>L</sub> = 1 kΩ
				9.6	17.3	1.0	20.0		C <sub>L</sub> = 50 pF, R <sub>L</sub> = 1 kΩ
		3.3 ± 0.3		5.5	8.8	1.0	10.5		C <sub>L</sub> = 15 pF, R <sub>L</sub> = 1 kΩ
				8.0	12.3	1.0	14.0		C <sub>L</sub> = 50 pF, R <sub>L</sub> = 1 kΩ
t <sub>PLZ</sub> , t <sub>PHZ</sub>	TRI-STATE Output Disable Time	2.7		11.6	16.0	1.0	19.0	ns	C <sub>L</sub> = 50 pF, R <sub>L</sub> = 1 kΩ
		3.3 ± 0.3		9.7	11.4	1.0	13.0		C <sub>L</sub> = 50 pF, R <sub>L</sub> = 1 kΩ
t <sub>OSLH</sub> t <sub>OSHL</sub>	Output to Output Skew (Note 1)	2.7			1.5		1.5	ns	C <sub>L</sub> = 50 pF

Note 1: Parameter guaranteed by design. t<sub>OSLH</sub> = |t<sub>PLHm</sub> - t<sub>PLHn</sub>|, t<sub>OSHL</sub> = |t<sub>PHLm</sub> - t<sub>PHLn</sub>|**Capacitance**

Symbol	Parameter	74LVX240			74LVX240		Units
		T <sub>A</sub> = +25°C			T <sub>A</sub> = −40°C to +85°C		
		Min	Typ	Max	Min	Max	
C <sub>IN</sub>	Input Capacitance		4	10		10	pF
C <sub>OUT</sub>	Output Capacitance		6				pF
C <sub>PD</sub>	Power Dissipation Capacitance (Note 1)		17	10			pF

Note 1: C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.Average operating current can be obtained by the equation:  $I_{CC(oper)} = \frac{C_{PD} \times V_{CC} \times f_{IN} + I_{CC}}{8 \text{ (per bit)}}$ 

Order Number	74LVX240M	74LVX240M	74LVX240M
See NS Package Number	74LVX240MX	74LVX240LX	74LVX240SCX
	M20B	M20D	M20C0



# 74LVX244

## Low Voltage Octal Buffer/Line Driver with TRI-STATE® Outputs

### General Description

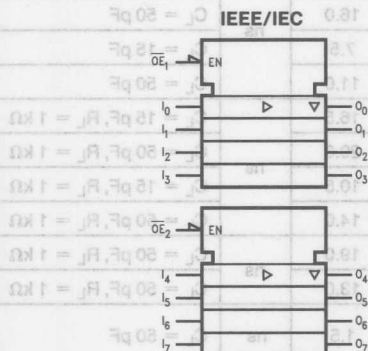
The LVX244 is an octal non-inverting buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter or receiver which provides improved PC board density. The inputs tolerate up to 7V allowing interface of 5V systems to 3V systems.

### Features

- Input voltage translation from 5V to 3V
- Ideal for low power/low noise 3.3V applications
- Available in SOIC JEDEC, SOIC EIAJ and SSOP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance

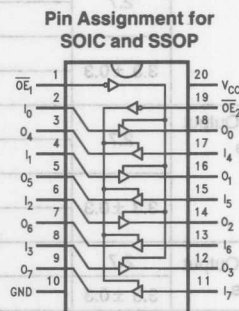
**Ordering Code:** See Section 11

### Logic Symbol



TL/F/11552-2

### Connection Diagram



TL/F/11552-1

Pin Names	Description
$\overline{OE}_1, \overline{OE}_2$	TRI-STATE Output Enable Inputs
$I_0-I_7$	Inputs
$O_0-O_7$	Outputs

### Truth Tables

Inputs		Outputs (Pins 12, 14, 16, 18)	
$\overline{OE}_1$	$I_n$		
L	L	L	
L	H	H	
H	X	Z	

Inputs		Outputs (Pins 3, 5, 7, 9)	
$\overline{OE}_2$	$I_n$		
L	L	L	
L	H	H	
H	X	Z	

H = HIGH Voltage Level

X = Immaterial

L = LOW Voltage Level

Z = High Impedance

	SOIC JEDEC	SOIC EIAJ	SSOP TYPE I
Order Number	74LVX244M 74LVX244MX	74LVX244SJ 74LVX244SJX	74LVX244MSCX
See NS Package Number	M20B	M20D	MSC20

**Absolute Maximum Ratings** (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )  $-0.5V$  to  $+7.0V$

DC Input Diode Current ( $I_{IK}$ )  
 $V_I = -0.5V$   $-20$  mA

DC Input Voltage ( $V_I$ )  $-0.5V$  to  $7V$

DC Output Diode Current ( $I_{OK}$ )  
 $V_O = -0.5V$   $-20$  mA  
 $V_O = V_{CC} + 0.5V$   $+20$  mA

DC Output Voltage ( $V_O$ )  $-0.5V$  to  $V_{CC} + 0.5V$

DC Output Source or Sink Current ( $I_O$ )  $\pm 25$  mA

DC  $V_{CC}$  or Ground Current ( $I_{CC}$  or  $I_{GND}$ )  $\pm 75$  mA

Storage Temperature ( $T_{STG}$ )  $-65^\circ C$  to  $+150^\circ C$

Power Dissipation  $180$  mW

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Recommended Operating Conditions**

Supply Voltage ( $V_{CC}$ )  $2.0V$  to  $3.6V$

Input Voltage ( $V_I$ )  $0V$  to  $5.5V$

Output Voltage ( $V_O$ )  $0V$  to  $V_{CC}$

Operating Temperature ( $T_A$ )  $-40^\circ C$  to  $+85^\circ C$

Input Rise and Fall Time ( $\Delta t/\Delta V$ )  $0$  ns/V to  $100$  ns/V

**DC Electrical Characteristics**

Symbol	Parameter	V <sub>CC</sub>	74LVX244			74LVX244		Units	Conditions
			T <sub>A</sub> = +25°C			T <sub>A</sub> = −40°C to +85°C			
			Min	Typ	Max	Min	Max		
V <sub>IH</sub>	High Level Input Voltage	2.0 3.0 3.6	1.5 2.0 2.4			1.5 2.0 2.4		V	
V <sub>IL</sub>	Low Level Input Voltage	2.0 3.0 3.6			0.5 0.8 0.8		0.5 0.8 0.8	V	
V <sub>OH</sub>	High Level Output Voltage	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0		1.9 2.9 2.48		V	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>OH</sub> = −50 μA I <sub>OH</sub> = −50 μA I <sub>OH</sub> = −4 mA
V <sub>OL</sub>	Low Level Output Voltage	2.0 3.0 3.0		0.0 0.0 0.36	0.1 0.1		0.1 0.44	V	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>OL</sub> = 50 μA I <sub>OL</sub> = 50 μA I <sub>OL</sub> = 4 mA
I <sub>OZ</sub>	TRI-STATE Output Off-State Current	3.6			±0.25		±2.5	μA	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>OUT</sub> = V <sub>CC</sub> or GND
I <sub>IN</sub>	Input Leakage Current	3.6			±0.1		±1.0	μA	V <sub>IN</sub> = 5.5V or GND
I <sub>CC</sub>	Quiescent Supply Current	3.6			4.0		40.0	μA	V <sub>IN</sub> = V <sub>CC</sub> or GND

**Noise Characteristics:** See Section 2 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	74LVX244		Units	C <sub>L</sub> (pF)
			T <sub>A</sub> = 25°C			
			Typ	Limit		
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	3.3	0.5	0.8	V	50
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	3.3	−0.5	−0.8	V	50
V <sub>IHD</sub>	Minimum High Level Dynamic Input Voltage	3.3		2.0	V	50
V <sub>ILD</sub>	Maximum Low Level Dynamic Input Voltage	3.3		0.8	V	50

Note: Input  $t_r = t_f = 3$  ns**AC Electrical Characteristics:** See Section 2 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	74LVX244			74LVX244			Units	Conditions
			T <sub>A</sub> = +25°C			T <sub>A</sub> = -40°C to +85°C				
			Min	Typ	Max	Min	Typ	Max		
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay Time	2.7	6.1	11.4		1.0		13.5	ns	C <sub>L</sub> = 15 pF
			8.6	14.9		1.0		17.0		C <sub>L</sub> = 50 pF
		3.3 ± 0.3	4.7	7.1		1.0		8.5		C <sub>L</sub> = 15 pF
			7.2	10.6		1.0		12.0		C <sub>L</sub> = 50 pF
t <sub>PZL</sub> , t <sub>PZH</sub>	TRI-STATE Output Enable Time	2.7	7.1	13.8		1.0		16.5	ns	C <sub>L</sub> = 15 pF, R <sub>L</sub> = 1 kΩ
			9.6	17.3		1.0		20.0		C <sub>L</sub> = 50 pF, R <sub>L</sub> = 1 kΩ
		3.3 ± 0.3	5.5	8.8		1.0		10.5		C <sub>L</sub> = 15 pF, R <sub>L</sub> = 1 kΩ
			8.0	12.3		1.0		14.0		C <sub>L</sub> = 50 pF, R <sub>L</sub> = 1 kΩ
t <sub>PLZ</sub> , t <sub>PHZ</sub>	TRI-STATE Output Disable Time	2.7	11.6	16.0		1.0		19.0	ns	C <sub>L</sub> = 50 pF, R <sub>L</sub> = 1 kΩ
		3.3 ± 0.3	9.7	11.4		1.0		13.0		C <sub>L</sub> = 50 pF, R <sub>L</sub> = 1 kΩ
t <sub>OSLH</sub> , t <sub>OSHL</sub>	Output to Output Skew (Note 1)	2.7		1.5				1.5	ns	C <sub>L</sub> = 50 pF

Note 1: Parameter guaranteed by design. t<sub>OSLH</sub> = |t<sub>PLHm</sub> - t<sub>PLHn</sub>|, t<sub>OSHL</sub> = |t<sub>PHLm</sub> - t<sub>PHLn</sub>|**Capacitance**

Symbol	Parameter	74LVX244			74LVX244		Units
		T <sub>A</sub> = +25°C			T <sub>A</sub> = −40°C to +85°C		
		Min	Typ	Max	Min	Max	
C <sub>IN</sub>	Input Capacitance		4	10		10	pF
C <sub>OUT</sub>	Output Capacitance		6				pF
C <sub>PD</sub>	Power Dissipation Capacitance (Note 1)		19				pF

Note 1: C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.Average operating current can be obtained by the equation:  $I_{CC(opr)} = \frac{C_{PD} \times V_{CC} \times f_{IN} + I_{CC}}{8 \text{ (per bit)}}$

# 74LVX245

## Low Voltage Octal Bidirectional Transceiver

### General Description

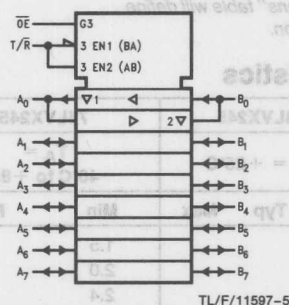
The LVX245 contains eight non-inverting bidirectional buffers. The Transmit/Receive (T/R) input determines the direction of data flow through the bidirectional transceiver. Transmit (active-HIGH) enables data from A ports to B ports; Receive (active-LOW) enables data from B ports to A ports. The Output Enable input, when HIGH, disables both A and B ports by placing them in a HIGH-Z condition.

### Features

- Ideal for low power/low noise 3.3V applications
- Available in SOIC JEDEC, SOIC EIAJ and SSOP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance

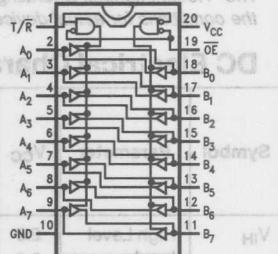
**Ordering Code:** See Section 11

### Logic Symbols



### Connection Diagram

#### Pin Assignment for SSOP and SOIC



Pin Names	Description
OE	Output Enable Input
T/R	Transmit/Receive Input
A0-A7	Side A TRI-STATE® Inputs or TRI-STATE Outputs
B0-B7	Side B TRI-STATE Inputs or TRI-STATE Outputs

### Truth Table

Inputs		Outputs
OE	T/R	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	HIGH-Z State

H = HIGH Voltage Level L = LOW Voltage Level X = Immaterial

	SOIC JEDEC	SOIC EIAJ	SSOP TYPE I
Order Number	74LVX245M	74LVX245SJ	74LVX245MSCX
See NS Package Number	M20B	M20D	MSC20

## Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Input Diode Current ( $I_{IK}$ )	-20 mA
$V_I = -0.5V$	
DC Input Voltage $T/\bar{R}$ , $\overline{OE}$ ( $V_I$ )	-0.5V to 7V
DC Diode Current ( $I_{OK}$ )	-20 mA
$V_O = -0.5V$	
$V_O = V_{CC} + 0.5V$	+20 mA
DC Bus I/O Voltage ( $V_{I/O}$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Source or Sink Current ( $I_O$ )	$\pm 25$ mA
DC $V_{CC}$ or Ground Current ( $I_{CC}$ or $I_{GND}$ )	$\pm 75$ mA
Storage Temperature ( $T_{STG}$ )	-65°C to +150°C
Power Dissipation	180 mW

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## Recommended Operating Conditions

Supply Voltage ( $V_{CC}$ )	2.0V to 3.6V
Input Voltage $T/\bar{R}$ , $\overline{OE}$ ( $V_I$ )	0V to 5.5V
Bus I/O Voltage ( $V_{I/O}$ )	0V to $V_{CC}$
Operating Temperature ( $T_A$ )	-40°C to +85°C
Input Rise and Fall Time ( $\Delta t/\Delta V$ )	0 ns/V to 100 ns/V

## DC Electrical Characteristics

Symbol	Parameter	V <sub>CC</sub>	74LVX245			74LVX245		Units	Conditions	
			T <sub>A</sub> = +25°C			T <sub>A</sub> = −40°C to +85°C				
			Min	Typ	Max	Min	Max			
V <sub>IH</sub>	High Level Input Voltage	2.0 3.0 3.6	1.5 2.0 2.4			1.5 2.0 2.4		V		
V <sub>IL</sub>	Low Level Input Voltage	2.0 3.0 3.6			0.5 0.8 0.8		0.5 0.8 0.8		V	
V <sub>OH</sub>	High Level Output Voltage	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0		1.9 2.9 2.48		V	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = −50 μA I <sub>OH</sub> = −50 μA I <sub>OH</sub> = −4 mA
V <sub>OL</sub>	Low Level Output Voltage	2.0 3.0 3.0		0.0 0.0 0.36	0.1 0.1 0.44		0.1 0.1 0.44	V	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 50 μA I <sub>OL</sub> = 50 μA I <sub>OL</sub> = 4 mA
I <sub>OZ</sub>	TRI-STATE Output Off-State Current	3.6			±0.25		±2.5	μA	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>OUT</sub> = V <sub>CC</sub> or GND	
I <sub>IN</sub>	Input Leakage Current	3.6			±0.1		±1.0	μA	V <sub>IN</sub> = 5.5V or GND	
I <sub>CC</sub>	Quiescent Supply Current	3.6			4.0		40.0	μA	V <sub>IN</sub> = V <sub>CC</sub> or GND	

**Noise Characteristics:** See Section 2 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	74LVX245		Units	Conditions C <sub>L</sub> (pF)
			T <sub>A</sub> = 25°C			
			Typ	Limit		
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	3.3	0.5	0.8	V	50
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	3.3	−0.5	−0.8	V	50
V <sub>IHD</sub>	Minimum High Level Dynamic Input Voltage	3.3		2.0	V	50
V <sub>ILD</sub>	Maximum Low Level Dynamic Input Voltage	3.3		0.8	V	50

Note: Input  $t_r = t_f = 3$  ns**AC Electrical Characteristics:** See Section 2 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	74LVX245			74LVX245		Units	Conditions
			T <sub>A</sub> = +25°C			T <sub>A</sub> = -40°C to +85°C			
			Min	Typ	Max	Min	Max		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Time	2.7	6.1	10.7	1.0	13.5	ns	C <sub>L</sub> = 15 pF	
			8.6	14.2	1.0	17.0		C <sub>L</sub> = 50 pF	
		3.3 ± 0.3	4.7	6.8	1.0	8.0		C <sub>L</sub> = 15 pF	
			7.2	10.1	1.0	11.5		C <sub>L</sub> = 50 pF	
t <sub>pZL</sub> t <sub>pZH</sub>	TRI-STATE Output Enable Time	2.7	9.0	16.9	1.0	20.5	ns	C <sub>L</sub> = 15 pF, R <sub>L</sub> = 1 kΩ	
			11.5	20.4	1.0	24.0		C <sub>L</sub> = 50 pF, R <sub>L</sub> = 1 kΩ	
		3.3 ± 0.3	7.1	11.0	1.0	13.0		C <sub>L</sub> = 15 pF, R <sub>L</sub> = 1 kΩ	
			9.6	14.5	1.0	16.5		C <sub>L</sub> = 50 pF, R <sub>L</sub> = 1 kΩ	
t <sub>PLZ</sub> t <sub>PHZ</sub>	TRI-STATE Output Disable Time	2.7	11.5	18.0	1.0	21.0	ns	C <sub>L</sub> = 50 pF, R <sub>L</sub> = 1 kΩ	
		3.3 ± 0.3	9.6	12.8	1.0	14.5		C <sub>L</sub> = 50 pF, R <sub>L</sub> = 1 kΩ	
t <sub>OSLH</sub> t <sub>OSHL</sub>	Output to Output Skew (Note 1)	2.7	1.5			1.5	ns	C <sub>L</sub> = 50 pF (Note 1)	

Note 1: Parameter guaranteed by design: t<sub>OSLH</sub> = |t<sub>PLHm</sub> - t<sub>PLHn</sub>|, t<sub>OSHL</sub> = |t<sub>PHLm</sub> - t<sub>PHLn</sub>|**Capacitance**

Symbol	Parameter	74LVX245			74LVX245		Units
		T <sub>A</sub> = +25°C			T <sub>A</sub> = −40°C to +85°C		
		Min	Typ	Max	Min	Max	
C <sub>IN</sub>	Input Capacitance T/R, $\overline{OE}$		4	10		10	pF
C <sub>I/O</sub>	Output Capacitance A <sub>n</sub> , B <sub>n</sub>		8				pF
C <sub>PD</sub>	Power Dissipation Capacitance (Note 1)		21				pF

Note 1: C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.Average operating current can be obtained by the equation:  $I_{CC(opr)} = \frac{C_{PD} \times V_{CC} \times f_{IN} + I_{CC1}}{8}$  (per bit)



## 74LVX273

### Low Voltage Octal D Flip-Flop

#### General Description

The LVX273 has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset (MR) input load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output.

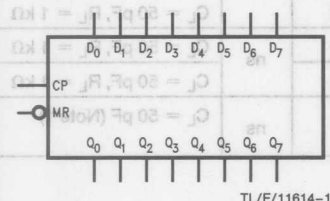
All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the MR input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements. The inputs tolerate up to 7V allowing interface of 5V systems to 3V systems.

#### Features

- Input voltage translation from 5V to 3V
- Ideal for low power/low noise 3.3V applications
- Available in SOIC JEDEC, SOIC EIAJ and SSOP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance

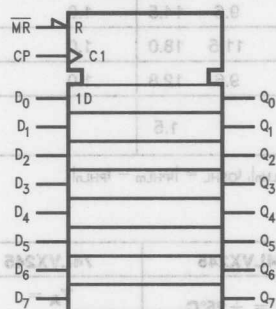
#### Ordering Code: See Section 11

#### Logic Symbols



TL/F/11614-1

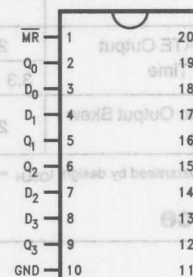
#### IEEE/IEC



TL/F/11614-4

#### Connection Diagram

##### Pin Assignment for SOIC and SSOP



TL/F/11614-2

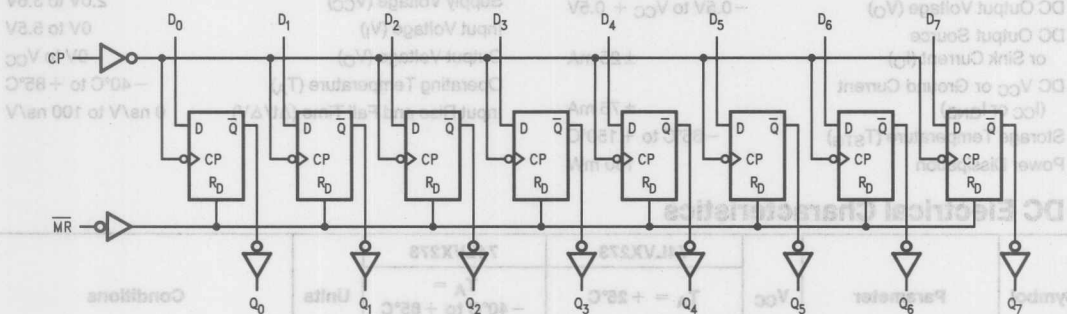
Pin Names	Description
D <sub>0</sub> -D <sub>7</sub>	Data Inputs
MR	Master Reset
CP	Clock Pulse Input
Q <sub>0</sub> -Q <sub>7</sub>	Data Outputs

	SOIC JEDEC	SOIC EIAJ	SSOP TYPE I
Order Number	74LVX273M 74LVX273MX	74LVX273SJ 74LVX273SJX	74LVX273MSCX
See NS Package Number	M20B	M20D	MSC20

Reset (Clear)	L	X	X	L
Load '1'	H		H	H
Load '0'	H		L	L

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial  
↗ = LOW-to-HIGH Transition

## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Symbol	Parameter	Units	Typ	Limit
$V_{IH}$	High Level Input Voltage	V	2.0	2.4
$V_{IL}$	Low Level Input Voltage	V	0.8	0.4
$V_{OH}$	High Level Output Voltage	V	2.0	2.4
$V_{OL}$	Low Level Output Voltage	V	0.8	0.4
$I_{OS}$	Tri-State <sup>®</sup> Output Off-State Current	$\mu A$	$\pm 0.25$	
$I_{IN}$	Input Leakage Current	$\mu A$	$\pm 1.0$	
$I_{CC}$	Quiescent Supply Current	$\mu A$	4.0	

## Noise Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	Units	Typ	Limit
$V_{OLP}$	Quiet Output Minimum Dynamic $V_{OL}$	V	0.8	0.4
$V_{OLV}$	Quiet Output Maximum Dynamic $V_{OL}$	V	0.8	0.4
$V_{IHD}$	Minimum High Level Dynamic Input Voltage	V	2.0	2.4
$V_{ILD}$	Minimum Low Level Dynamic Input Voltage	V	0.8	0.4

Notes: Input  $\beta = 10$

# Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Input Diode Current ( $I_{IK}$ )	-20 mA
$V_I = -0.5V$	-0.5V to 7V
DC Input Voltage ( $V_I$ )	
DC Output Diode Current ( $I_{OK}$ )	-20 mA
$V_O = -0.5V$	+20 mA
$V_O = V_{CC} + 0.5V$	
DC Output Voltage ( $V_O$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Source or Sink Current ( $I_O$ )	$\pm 25$ mA
DC $V_{CC}$ or Ground Current ( $I_{CC}$ or $I_{GND}$ )	$\pm 75$ mA
Storage Temperature ( $T_{STG}$ )	-65°C to +150°C
Power Dissipation	180 mW

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## Recommended Operating Conditions

Supply Voltage ( $V_{CC}$ )	2.0V to 3.6V
Input Voltage ( $V_I$ )	0V to 5.5V
Output Voltage ( $V_O$ )	0V to $V_{CC}$
Operating Temperature ( $T_A$ )	-40°C to +85°C
Input Rise and Fall Time ( $\Delta t/\Delta V$ )	0 ns/V to 100 ns/V

## DC Electrical Characteristics

Symbol	Parameter	V <sub>CC</sub>	74LVX273			74LVX273		Units	Conditions	
			T <sub>A</sub> = +25°C			T <sub>A</sub> = −40°C to +85°C				
			Min	Typ	Max	Min	Max			
V <sub>IH</sub>	High Level Input Voltage	2.0 3.0 3.6	1.5 2.0 2.4			1.5 2.0 2.4		V		
V <sub>IL</sub>	Low Level Input Voltage	2.0 3.0 3.6			0.5 0.8 0.8		0.5 0.8 0.8	V		
V <sub>OH</sub>	High Level Output Voltage	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0		1.9 2.9 2.48		V	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = −50 μA I <sub>OH</sub> = −50 μA I <sub>OH</sub> = −4 mA
V <sub>OL</sub>	Low Level Output Voltage	2.0 3.0 3.0		0.0 0.0 0.36		0.1 0.1 0.44		V	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 50 μA I <sub>OL</sub> = 50 μA I <sub>OL</sub> = 4 mA
I <sub>OZ</sub>	TRI-STATE® Output Off-State Current	3.6			± 0.25		± 2.5	μA	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>OUT</sub> = V <sub>CC</sub> or GND	
I <sub>IN</sub>	Input Leakage Current	3.6			± 0.1		± 1.0	μA	V <sub>IN</sub> = 5.5V or GND	
I <sub>CC</sub>	Quiescent Supply Current	3.6			4.0		40.0	μA	V <sub>IN</sub> = V <sub>CC</sub> or GND	

## Noise Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	74LVX273		Units	C <sub>L</sub> (pF)
			T <sub>A</sub> = 25°C			
			Typ	Limit		
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	3.3	0.5	0.8	V	50
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	3.3	−0.5	−0.8	V	50
V <sub>IHD</sub>	Minimum High Level Dynamic Input Voltage	3.3		2.0	V	50
V <sub>ILD</sub>	Maximum Low Level Dynamic Input Voltage	3.3		0.8	V	50

Note: Input  $t_r = t_f = 3 \text{ ns}$

# AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	74LVX273			74LVX273		Units	C <sub>L</sub> (pF)
			T <sub>A</sub> = + 25°C			T <sub>A</sub> = − 40°C to + 85°C			
			Min	Typ	Max	Min	Max		
t <sub>PLH</sub>	Propagation Delay Time CP to Q <sub>n</sub>	2.7	9.0	16.9	1.0	20.5	ns	15	
t <sub>PHL</sub>			11.5	20.4	1.0	24.0		50	
		3.3 ± 0.3	7.1	11.0	1.0	13.0	ns	15	
			9.6	14.5	1.0	16.5		50	
t <sub>PHL</sub>	Propagation Delay MR to Q <sub>n</sub>	2.7	9.3	17.8	1.0	20.5	ns	15	
			11.8	21.1	1.0	24.0		50	
		3.3 ± 0.3	7.3	11.5	1.0	13.5	ns	15	
			9.8	15.0	1.0	17.0		50	
t <sub>S</sub>	Setup Time D <sub>n</sub> to CP	2.7	8.0		9.5	ns			
		3.3 ± 0.3	5.5		6.5				
t <sub>H</sub>	Hold Time D <sub>n</sub> to CP	2.7	1.0		1.0	ns			
		3.3 ± 0.3	1.0		1.0				
t <sub>REM</sub>	Removal Time MR to CP	2.7	4.0		4.0	ns			
		3.3 ± 0.3	2.5		2.5				
t <sub>W</sub>	Clock Pulse Width	2.7	8.0		9.5	ns			
		3.3 ± 0.3	5.5		6.5				
t <sub>W</sub>	MR Pulse Width	2.7	7.5		8.5	ns			
		3.3 ± 0.3	5.0		6.0				
f <sub>MAX</sub>	Maximum Clock Frequency	2.7	55	110	45	MHz	15		
			45	60	40		50		
		3.3 ± 0.3	95	150	80		15		
			60	90	50		50		
t <sub>OSLH</sub> t <sub>OSHL</sub>	Output to Output Skew (Note 1)	2.7		1.5	1.5	ns	50		

Note 1: Parameter guaranteed by design. t<sub>OSLH</sub> = |t<sub>PLHm</sub> - t<sub>PLHn</sub>|; t<sub>OSHL</sub> = |t<sub>PHLm</sub> - t<sub>PHLn</sub>|

## Capacitance

Symbol	Parameter	74LVX273			74LVX273		Units
		T <sub>A</sub> = +25°C			T <sub>A</sub> = -40°C to +85°C		
		Min	Typ	Max	Min	Max	
C <sub>IN</sub>	Input Capacitance		4	10		10	pF
C <sub>OUT</sub>	Output Capacitance		6				pF
C <sub>PD</sub>	Power Dissipation Capacitance (Note 1)		31				pF

Note 1: C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:  $I_{CC(opr)} = \frac{C_{PD} \times V_{CC} \times f_{IN} + I_{CC}}{8 \text{ (per F/F)}}$



## 74LVX373

### Low Voltage Octal Transparent Latch with TRI-STATE® Outputs

#### General Description

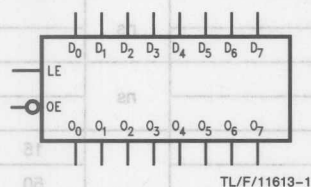
The LVX373 consists of eight latches with TRI-STATE outputs for bus organized system applications. The latches appear transparent to the data when Latch Enable (LE) is HIGH. When LE is low, the data satisfying the input timing requirements is latched. Data appears on the bus when the Output Enable (OE) is LOW. When OE is HIGH, the bus output is in the high impedance state. The inputs tolerate up to 7V allowing interface of 5V systems to 3V systems.

#### Features

- Input voltage translation from 5V to 3V
- Ideal for low power/low noise 3.3V applications
- Available in SOIC JEDEC, SOIC EIAJ and SSOP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance

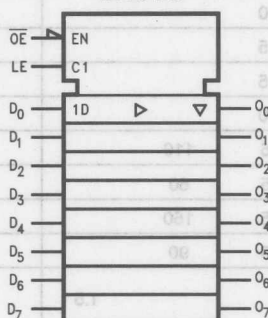
**Ordering Code:** See Section 11

#### Logic Symbols



TL/F/11613-1

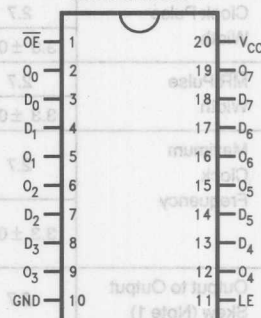
#### IEEE/IEC



TL/F/11613-4

#### Connection Diagram

##### Pin Assignment for SOIC and SSOP



TL/F/11613-2

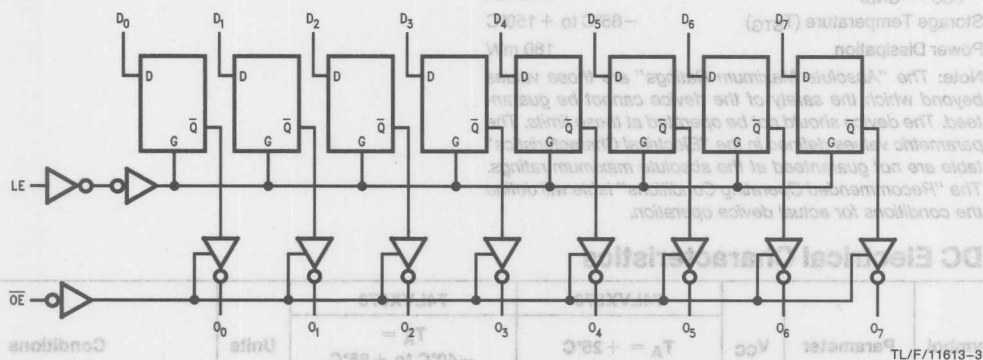
Pin Names	Description
D <sub>0</sub> -D <sub>7</sub>	Data Inputs
LE	Latch Enable Input
OE	Output Enable Input
O <sub>0</sub> -O <sub>7</sub>	TRI-STATE Latch Outputs

	SOIC JEDEC	SOIC EIAJ	SSOP TYPE I
Order Number	74LVX373M 74LVX373MX	74LVX373SJ 74LVX373SJX	74LVX373MSCX
See NS Package Number	M20B	M20D	MSC20

## Functional Description

The LVX373 contains eight D-type latches with TRI-STATE standard outputs. When the Latch Enable (LE) input is HIGH, data on the  $D_n$  inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE standard outputs are controlled by the Output Enable ( $\overline{OE}$ ) input. When  $\overline{OE}$  is LOW, the standard outputs are in the 2-state mode. When  $\overline{OE}$  is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Truth Table

Inputs		Outputs	
LE	$\overline{OE}$	$D_n$	$O_n$
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	$O_0$

H = HIGH Voltage Level

L = LOW Voltage Level

Z = High Impedance

X = Immaterial

$O_0$  = Previous  $O_0$  before HIGH to Low transition of Latch Enable

Parameter		Min	Typ	Max	Unit
$V_{IH}$	High Level Input Voltage	2.0	2.5	3.0	V
	High Level Output Voltage	2.0	2.5	3.0	V
$V_{IL}$	Low Level Input Voltage	0.8	0.8	0.8	V
	Low Level Output Voltage	0.8	0.8	0.8	V
$V_{OH}$	High Level Output Voltage	2.0	2.5	3.0	V
	High Level Input Voltage	2.0	2.5	3.0	V
$V_{OL}$	Low Level Output Voltage	0.8	0.8	0.8	V
	Low Level Input Voltage	0.8	0.8	0.8	V
$I_{OZ}$	TRI-STATE Output Current	±0.25	±0.25	±0.25	mA
	TRI-STATE Input Current	±0.1	±0.1	±0.1	mA
$I_{IN}$	Input Leakage Current	±0.1	±0.1	±0.1	mA
	Input Leakage Current	±0.1	±0.1	±0.1	mA
$I_{CC}$	Supply Current	3.8	4.0	4.0	mA
	Supply Current	3.8	4.0	4.0	mA

**Absolute Maximum Ratings** (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Input Diode Current ( $I_{IK}$ )	-20 mA
$V_I = -0.5V$	+20 mA
DC Input Voltage ( $V_I$ )	-0.5V to 7V
DC Output Diode Current ( $I_{OK}$ )	-20 mA
$V_O = -0.5V$	+20 mA
$V_O = V_{CC} + 0.5V$	
DC Output Voltage ( $V_O$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Source or Sink Current ( $I_O$ )	$\pm 25$ mA
DC $V_{CC}$ or Ground Current ( $I_{CC}$ or $I_{GND}$ )	$\pm 75$ mA
Storage Temperature ( $T_{STG}$ )	-65°C to +150°C
Power Dissipation	180 mW

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Recommended Operating Conditions**

Supply Voltage ( $V_{CC}$ )	2.0V to 3.6V
Input Voltage ( $V_I$ )	0V to 5.5V
Output Voltage ( $V_O$ )	0V to $V_{CC}$
Operating Temperature ( $T_A$ )	-40°C to +85°C
Input Rise and Fall Time ( $\Delta t/\Delta V$ )	0 ns/V to 100 ns/V

**DC Electrical Characteristics**

Symbol	Parameter	V <sub>CC</sub>	74LVX373			74LVX373		Units	Conditions	
			T <sub>A</sub> = +25°C			T <sub>A</sub> = −40°C to +85°C				
			Min	Typ	Max	Min	Max			
V <sub>IH</sub>	High Level Input Voltage	2.0 3.0 3.6	1.5 2.0 2.4			1.5 2.0 2.4		V		
V <sub>IL</sub>	Low Level Input Voltage	2.0 3.0 3.6			0.5 0.8 0.8		0.5 0.8 0.8	V		
V <sub>OH</sub>	High Level Output Voltage	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0		1.9 2.9 2.48		V	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = −50 μA I <sub>OH</sub> = −50 μA I <sub>OH</sub> = −4 mA
V <sub>OL</sub>	Low Level Output Voltage	2.0 3.0 3.0		0.0 0.0	0.1 0.1 0.36		0.1 0.1 0.44	V	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 50 μA I <sub>OL</sub> = 50 μA I <sub>OL</sub> = 4 mA
I <sub>OZ</sub>	TRI-STATE Output Off-State Current	3.6			±0.25		±2.5	μA	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>OUT</sub> = V <sub>CC</sub> or GND	
I <sub>IN</sub>	Input Leakage Current	3.6			±0.1		±1.0	μA	V <sub>IN</sub> = 5.5V or GND	
I <sub>CC</sub>	Quiescent Supply Current	3.6			4.0		40.0	μA	V <sub>IN</sub> = V <sub>CC</sub> or GND	

Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = 25°C		Units	C <sub>L</sub> (pF)
			Typ	Limit		
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	3.3	0.5	0.8	V	50
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	3.3	-0.5	-0.8	V	50
V <sub>IHD</sub>	Minimum High Level Dynamic Input Voltage	3.3		2.0	V	50
V <sub>ILD</sub>	Maximum Low Level Dynamic Input Voltage	3.3		0.8	V	50

Note: Input t<sub>r</sub> = t<sub>f</sub> = 3 ns.

## AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	74LVX373			74LVX373		Units	Conditions
			T <sub>A</sub> = +25°C			T <sub>A</sub> = −40°C to +85°C			
			Min	Typ	Max	Min	Max		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Time D <sub>n</sub> to O <sub>n</sub>	2.7	7.7	15.0	1.0	18.5	ns	C <sub>L</sub> = 15 pF	
			10.2	18.5	1.0	22.0		C <sub>L</sub> = 50 pF	
		3.3 ± 0.3	6.0	9.7	1.0	11.5		C <sub>L</sub> = 15 pF	
			8.5	13.2	1.0	15.0		C <sub>L</sub> = 50 pF	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Time LE to O <sub>n</sub>	2.7	7.5	14.5	1.0	17.5	ns	C <sub>L</sub> = 15 pF	
			10.0	18.0	1.0	21.0		C <sub>L</sub> = 50 pF	
		3.3 ± 0.3	5.8	9.3	1.0	11.0		C <sub>L</sub> = 15 pF	
			8.3	12.8	1.0	14.5		C <sub>L</sub> = 50 pF	
t <sub>PZL</sub> t <sub>PZH</sub>	TRI-STATE Output Enable Time	2.7	7.7	15.0	1.0	18.5	ns	C <sub>L</sub> = 15 pF, R <sub>L</sub> = 1 kΩ	
			10.2	18.5	1.0	22.0		C <sub>L</sub> = 50 pF, R <sub>L</sub> = 1 kΩ	
		3.3 ± 0.3	6.0	9.7	1.0	11.5		C <sub>L</sub> = 15 pF, R <sub>L</sub> = 1 kΩ	
			8.5	13.2	1.0	15.0		C <sub>L</sub> = 50 pF, R <sub>L</sub> = 1 kΩ	
t <sub>PLZ</sub> t <sub>PHZ</sub>	TRI-STATE Output Disable Time	2.7	9.8	18.0	1.0	21.0	ns	C <sub>L</sub> = 50 pF, R <sub>L</sub> = 1 kΩ	
		3.3 ± 0.3	8.2	12.8	1.0	14.5		C <sub>L</sub> = 50 pF, R <sub>L</sub> = 1 kΩ	
t <sub>W</sub>	LE Pulse Width, HIGH	2.7	6.5		7.5	ns			
		3.3 ± 0.3	5.0		5.0				
t <sub>S</sub>	Setup Time, D <sub>n</sub> to LE	2.7	6.0		6.0	ns			
		3.3 ± 0.3	4.0		4.0				
t <sub>H</sub>	Hold Time, D <sub>n</sub> to LE	2.7	1.0		1.0	ns			
		3.3 ± 0.3	1.0		1.0				
t <sub>OSLH</sub> t <sub>OSHL</sub>	Output to Output Skew (Note 1)	2.7	1.5		1.5		ns	C <sub>L</sub> = 50 pF	

Note 1: Parameter guaranteed by design. t<sub>OSLH</sub> = |t<sub>PLHm</sub> - t<sub>PLHn</sub>|, t<sub>OSHL</sub> = |t<sub>PHLm</sub> - t<sub>PHLn</sub>|

## Capacitance

Symbol	Parameter	74LVX373			74LVX373		Units
		$T_A = +25^{\circ}\text{C}$			$T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$		
		Min	Typ	Max	Min	Max	
C <sub>IN</sub>	Input Capacitance		4	10		10	pF
C <sub>OUT</sub>	Output Capacitance		6				pF
C <sub>PD</sub>	Power Dissipation Capacitance (Note 1)		27				pF

Note 1:  $C_{PD}$  is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:  $I_{CC(oper)} = \frac{C_{PD} \times V_{CC} \times f_{IN} + I_{CC}}{8 \text{ (per Latch)}}$

Symbol	Parameter	V <sub>CC</sub> (V)	74LVX373			Units	Conditions
			T <sub>A</sub> = +25°C				
			Min	Typ	Max		
t <sub>PLH</sub> t <sub>PLH</sub>	Propagation Delay Time D <sub>n</sub> to Q <sub>n</sub>	5.7	7.7	18.0	1.0	ns	C <sub>L</sub> = 15 pF
			10.2	18.8	1.0		C <sub>L</sub> = 50 pF
		3.3 ± 0.3	8.0	9.7	1.0		C <sub>L</sub> = 15 pF
			8.8	13.2	1.0		C <sub>L</sub> = 50 pF
t <sub>PLH</sub> t <sub>PLH</sub>	Propagation Delay Time LE to Q <sub>n</sub>	5.7	7.8	14.8	1.0	ns	C <sub>L</sub> = 15 pF
			10.0	18.0	1.0		C <sub>L</sub> = 50 pF
		3.3 ± 0.3	8.8	9.7	1.0		C <sub>L</sub> = 15 pF
			8.8	12.8	1.0		C <sub>L</sub> = 50 pF
t <sub>PZH</sub> t <sub>PZH</sub>	TRI-STATE Output Enable Time	5.7	7.7	18.0	1.0	ns	C <sub>L</sub> = 15 pF, R <sub>L</sub> = 1 kΩ
			10.2	18.8	1.0		C <sub>L</sub> = 50 pF, R <sub>L</sub> = 1 kΩ
		3.3 ± 0.3	8.0	9.7	1.0		C <sub>L</sub> = 15 pF, R <sub>L</sub> = 1 kΩ
			8.8	13.2	1.0		C <sub>L</sub> = 50 pF, R <sub>L</sub> = 1 kΩ
t <sub>PZH</sub> t <sub>PZH</sub>	TRI-STATE Output Disable Time	3.3 ± 0.3	8.8	18.0	1.0	ns	C <sub>L</sub> = 50 pF, R <sub>L</sub> = 1 kΩ
			8.2	12.8	1.0		C <sub>L</sub> = 50 pF, R <sub>L</sub> = 1 kΩ
t <sub>W</sub>	LE Pulse Width, HIGH	5.7	8.8		7.5	ns	
			3.3 ± 0.3	8.0	2.0		
t <sub>S</sub>	Setup Time, D <sub>n</sub> to LE	5.7	8.0		6.0	ns	
			3.3 ± 0.3	4.0	4.0		
t <sub>H</sub>	Hold Time, D <sub>n</sub> to LE	5.7	1.0		1.0	ns	
			3.3 ± 0.3	1.0	1.0		
t <sub>OSLH</sub> (Note 1)	Output to Output Skew	5.7	1.8		1.8	ns	C <sub>L</sub> = 50 pF

Note 1: Parameter guaranteed by design:  $t_{OSLH} = t_{PZH} - t_{PZL}$



## 74LVX374

### Low Voltage Octal D Flip-Flop with TRI-STATE® Outputs

#### General Description

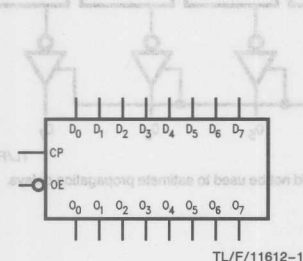
The LVX374 is a high-speed, low-power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and TRI-STATE outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable ( $\overline{OE}$ ) are common to all flip-flops. The inputs tolerate up to 7V allowing interface of 5V systems to 3V systems.

#### Features

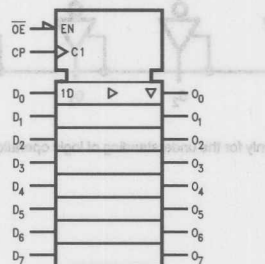
- Input voltage translation from 5V to 3V
- Ideal for low power/low noise 3.3V applications
- Available in SOIC JEDEC, SOIC EIAJ and SSOP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance

**Ordering Code:** See Section 11

#### Logic Symbols

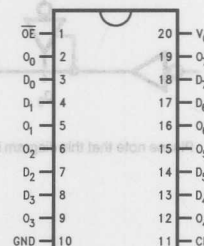


#### IEEE/IEC



#### Connection Diagram

##### Pin Assignment for SOIC and SSOP



Pin Names	Description
D <sub>0</sub> -D <sub>7</sub>	Data Inputs
CP	Clock Pulse Input
$\overline{OE}$	TRI-STATE Output Enable Input
Q <sub>0</sub> -Q <sub>7</sub>	TRI-STATE Outputs

	SOIC JEDEC	SOIC EIAJ	SSOP TYPE I
Order Number	74LVX374M 74LVX374MX	74LVX374SJ 74LVX374SJJ	74LVX374MSCX
See NS Package Number	M20B	M20D	MSC20

## Functional Description

The LVX374 consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ( $\overline{OE}$ ) LOW, the contents of the eight flip-flops are available at the outputs. When the  $\overline{OE}$  is HIGH, the outputs go to the high impedance state. Operation of the  $\overline{OE}$  input does not affect the state of the flip-flops.

## Truth Table

Inputs		Outputs	
$D_n$	CP	$\overline{OE}$	$O_n$
H	—	L	H
L	—	L	L
X	X	H	Z

H = HIGH Voltage Level

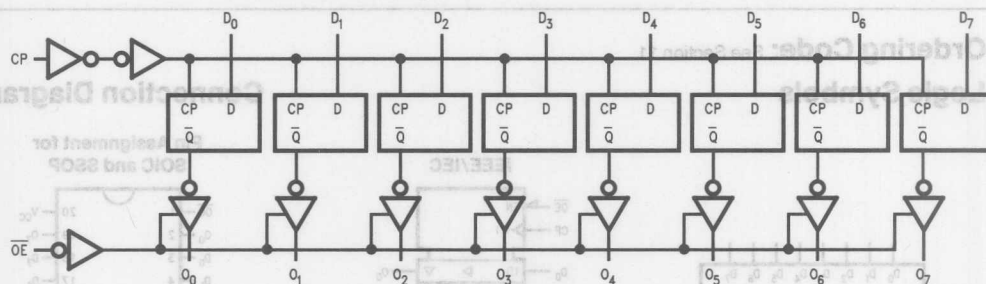
L = LOW Voltage Level

X = Immaterial

Z = High Impedance

— = LOW-to-HIGH Transition

## Logic Diagram



TL/F/11612-3

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Pin Names	Description
$O_0$ – $O_7$	TRI-STATE Outputs
$\overline{OE}$	TRI-STATE Output Enable Input
CP	Clock Pulse Input
$D_0$ – $D_7$	Data Inputs

Order Number	SOIC 16DEC	SOIC EIAL	SSOP TYPE I
See NS Package Number	74LVX374M	74LVX374SL	74LVX374M2CX
	M200	M200	M200

**Absolute Maximum Ratings** (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )  $-0.5V$  to  $+7.0V$

DC Input Diode Current ( $I_{IK}$ )  $-20$  mA  
 $V_I = -0.5V$

DC Input Voltage ( $V_I$ )  $-0.5V$  to  $7V$

DC Output Diode Current ( $I_{OK}$ )  $-20$  mA  
 $V_O = -0.5V$

$V_O = V_{CC} + 0.5V$   $+20$  mA

DC Output Voltage ( $V_O$ )  $-0.5V$  to  $V_{CC} + 0.5V$

DC Output Source or Sink Current ( $I_O$ )  $\pm 25$  mA

DC  $V_{CC}$  or Ground Current ( $I_{CC}$  or  $I_{GND}$ )  $\pm 75$  mA

Storage Temperature ( $T_{STG}$ )  $-65^\circ C$  to  $+150^\circ C$

Power Dissipation  $180$  mW

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**DC Electrical Characteristics**

Symbol	Parameter	V <sub>CC</sub>	74LVX374			74LVX374		Units	Conditions	
			T <sub>A</sub> = +25°C			T <sub>A</sub> = −40°C to +85°C				
			Min	Typ	Max	Min	Max			
V <sub>IH</sub>	High Level	2.0	1.5			1.5		V		
	Input	3.0	2.0			2.0				
	Voltage	3.6	2.4			2.4				
V <sub>IL</sub>	Low Level	2.0			0.5		0.5	V		
	Input	3.0			0.8		0.8			
	Voltage	3.6			0.8		0.8			
V <sub>OH</sub>	High Level	2.0	1.9	2.0		1.9		V	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>OH</sub> = −50 μA I <sub>OH</sub> = −50 μA I <sub>OH</sub> = −4 mA	
	Output	3.0	2.9	3.0		2.9				
	Voltage	3.0	2.58			2.48				
V <sub>OL</sub>	Low Level	2.0		0.0	0.1		0.1	V	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>OL</sub> = 50 μA I <sub>OL</sub> = 50 μA I <sub>OL</sub> = 4 mA	
	Output	3.0		0.0	0.1		0.1			
	Voltage	3.0			0.36		0.44			
I <sub>OZ</sub>	TRI-STATE Output Off-State Current	3.6			±0.25		±2.5	μA	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>OUT</sub> = V <sub>CC</sub> or GND	
I <sub>IN</sub>	Input Leakage Current	3.6			±0.1		±1.0	μA	V <sub>IN</sub> = 5.5V or GND	
I <sub>CC</sub>	Quiescent Supply Current	3.6			4.0		40.0	μA	V <sub>IN</sub> = V <sub>CC</sub> or GND	

**Recommended Operating Conditions**

Supply Voltage ( $V_{CC}$ )  $2.0V$  to  $3.6V$

Input Voltage ( $V_I$ )  $0V$  to  $5.5V$

Output Voltage ( $V_O$ )  $0V$  to  $V_{CC}$

Operating Temperature ( $T_A$ )  $-40^\circ C$  to  $+85^\circ C$

Input Rise and Fall Time ( $\Delta t/\Delta V$ )  $0$  ns/V to  $100$  ns/V

**Noise Characteristics:** See Section 2 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	74LVX374		Units	C <sub>L</sub> (pF)
			T <sub>A</sub> = 25°C			
			Typ	Limit		
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	3.3	0.5	0.8	V	50
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	3.3	−0.5	−0.8	V	50
V <sub>IHD</sub>	Minimum High Level Dynamic Input Voltage	3.3		2.0	V	50
V <sub>ILD</sub>	Maximum Low Level Dynamic Input Voltage	3.3		0.8	V	50

Note: Input t<sub>r</sub> = t<sub>f</sub> = 3 ns**AC Electrical Characteristics:** See Section 2 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	74LVX374			74LVX374		Units	Conditions
			T <sub>A</sub> = +25°C			T <sub>A</sub> = −40°C to +85°C			
			Min	Typ	Max	Min	Max		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Time CP to O <sub>n</sub>	2.7		8.5	16.3	1.0	19.5	ns	C <sub>L</sub> = 15 pF
				11.0	19.8	1.0	23.0		C <sub>L</sub> = 50 pF
		3.3 ± 0.3		6.7	10.6	1.0	12.5	ns	C <sub>L</sub> = 15 pF
				9.2	14.1	1.0	16.0		C <sub>L</sub> = 50 pF
t <sub>PZL</sub> t <sub>PZH</sub>	TRI-STATE Output Enable Time	2.7		7.6	14.5	1.0	17.5	ns	C <sub>L</sub> = 15 pF, R <sub>L</sub> = 1 kΩ
				10.1	18.0	1.0	21.0		C <sub>L</sub> = 50 pF, R <sub>L</sub> = 1 kΩ
		3.3 ± 0.3		5.9	9.3	1.0	11.0	ns	C <sub>L</sub> = 15 pF, R <sub>L</sub> = 1 kΩ
				8.4	12.8	1.0	14.5		C <sub>L</sub> = 50 pF, R <sub>L</sub> = 1 kΩ
t <sub>PLZ</sub> t <sub>PHZ</sub>	TRI-STATE Output Disable Time	2.7		11.5	18.5	1.0	22.0	ns	C <sub>L</sub> = 50 pF, R <sub>L</sub> = 1 kΩ
		3.3 ± 0.3		9.6	13.2	1.0	15.0		C <sub>L</sub> = 50 pF, R <sub>L</sub> = 1 kΩ
t <sub>W</sub>	CP Pulse Width	2.7	7.5			8.0		ns	
		3.3 ± 0.3	5.0			5.5			
t <sub>S</sub>	Setup Time D <sub>n</sub> to CP	2.7	6.5			6.5		ns	
		3.3 ± 0.3	4.5			4.5			
t <sub>H</sub>	Hold Time D <sub>n</sub> to CP	2.7	2.0			2.0		ns	
		3.3 ± 0.3	2.0			2.0			
f <sub>MAX</sub>	Maximum Clock Frequency	2.7	60	115		50		MHz	C <sub>L</sub> = 15 pF
			45	60		40	C <sub>L</sub> = 50 pF		
		3.3 ± 0.3	100	160		85			C <sub>L</sub> = 15 pF
			60	95		55			C <sub>L</sub> = 50 pF
t <sub>OSLH</sub> t <sub>OSHL</sub>	Output to Output Skew (Note 1)	2.7		1.5		1.5	ns	C <sub>L</sub> = 50 pF	

Note 1: Parameter guaranteed by design. t<sub>OSLH</sub> = |t<sub>PLHm</sub> - t<sub>PLHn</sub>|, t<sub>OSHL</sub> = |t<sub>PHLm</sub> - t<sub>PHLn</sub>|**Capacitance**

Symbol	Parameter	74LVX374			74LVX374		Units
		T <sub>A</sub> = +25°C			T <sub>A</sub> = −40°C to +85°C		
		Min	Typ	Max	Min	Max	
C <sub>IN</sub>	Input Capacitance		4	10		10	pF
C <sub>OUT</sub>	Output Capacitance		6				pF
C <sub>PD</sub>	Power Dissipation Capacitance (Note 1)		32				pF

Note 1: C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.Average operating current can be obtained by the equation:  $I_{CC(opr)} = \frac{C_{PD} \times V_{CC} \times f_{IN} + I_{CC}}{8 \text{ (per F/F)}}$



## 74LVX573

### Low Voltage Octal Latch with TRI-STATE® Outputs

#### General Description

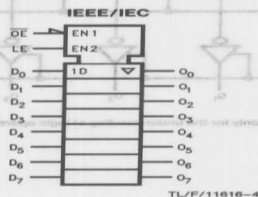
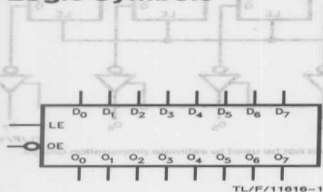
The LVX573 is a high-speed octal latch with buffered common Latch Enable (LE) and buffered common Output Enable (OE) inputs. The LVX573 is functionally identical to the LVX373 but with inputs and outputs on opposite sides of the package. The inputs tolerate up to 7V allowing interface of 5V systems to 3V systems.

#### Features

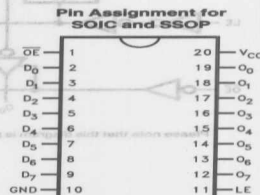
- Input voltage translation from 5V to 3V
- Ideal for low power/low noise 3.3V applications
- Available in SOIC JEDEC, SOIC EIAJ and SSOP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance

**Ordering Code:** See Section 11

#### Logic Symbols



#### Connection Diagram



Pin Names	Description
D <sub>0</sub> -D <sub>7</sub>	Data Inputs
LE	Latch Enable Input
OE	TRI-STATE Output Enable Input
O <sub>0</sub> -O <sub>7</sub>	TRI-STATE Latch Outputs

	SOIC JEDEC	SOIC EIAJ	SSOP TYPE 1
Order Number	74LVX573M 74LVX573MX	74LVX573SJ 74LVX573SJX	74LVX573MSCX
See NS Package Number	M20B	M20D	MSC20

# Functional Description

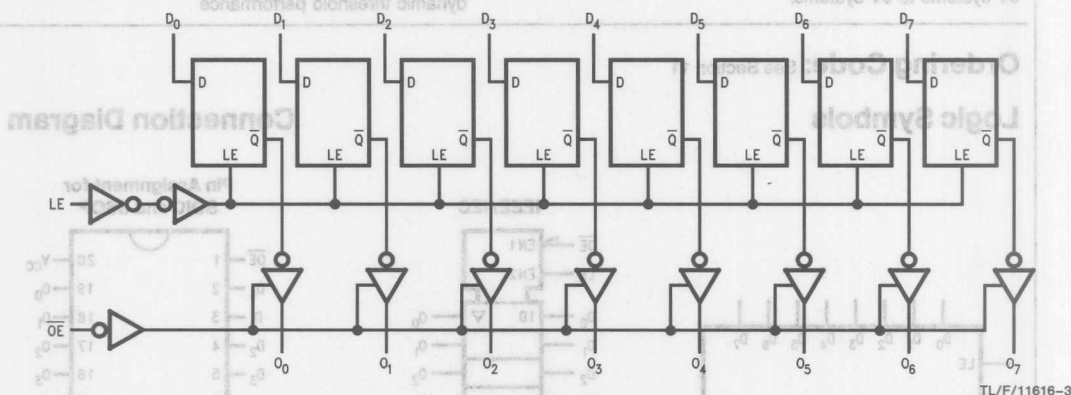
The LVX573 contains eight D-type latches with TRI-STATE® output buffers. When the Latch Enable (LE) input is HIGH, data on the D<sub>n</sub> inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE® buffers are controlled by the Output Enable (OE) input. When OE is LOW, the buffers are enabled. When OE is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches.

# Truth Table

Inputs			Outputs
OE	LE	D	O <sub>n</sub>
L	H	H	H
L	H	L	L
L	L	X	O <sub>0</sub>
H	X	X	Z

H = HIGH Voltage  
L = LOW Voltage  
Z = High Impedance  
X = Immaterial  
O<sub>0</sub> = Previous O<sub>0</sub> before HIGH-to-LOW transition of Latch Enable

# Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Pin Name	Description
D <sub>0</sub> -D <sub>7</sub>	Data inputs
LE	Latch Enable input
OE	TRI-STATE Output Enable input
O <sub>0</sub> -O <sub>7</sub>	TRI-STATE Latch Outputs

Order Number	SOIC JEDEC	SOIC EIAL	SSOP TYPE I
74LVX573M	74LVX573M	74LVX573J	74LVX573SX
74LVX573MX	74LVX573LX	74LVX573LX	74LVX573MSX
See NS Package Number	M20B	M20D	M20C0

Supply Voltage ( $V_{CC}$ )		-0.5V to +7.0V	Input Voltage ( $V_I$ )	0V to 5.5V
DC Input Diode Current ( $I_{IK}$ )		-20 mA	Output Voltage ( $V_O$ )	0V to $V_{CC}$
$V_I = -0.5V$			Operating Temperature ( $T_A$ )	+40°C to +85°C
DC Input Voltage ( $V_I$ )		-0.5V to 7V	Input Rise and Fall Time ( $\Delta t/\Delta V$ )	0 ns/V to 100 ns/V
DC Output Diode Current ( $I_{OK}$ )		-20 mA		
$V_O = -0.5V$		-20 mA		
$V_O = V_{CC} + 0.5V$		+20 mA		
DC Output Voltage ( $V_O$ )		-0.5V to $V_{CC} + 0.5V$		
DC Output Source or Sink Current ( $I_O$ )		$\pm 25$ mA		
DC $V_{CC}$ or Ground Current ( $I_{CC}$ or $I_{GND}$ )		$\pm 75$ mA		
Storage Temperature ( $T_{STG}$ )		-65°C to +150°C		
Power Dissipation		180 mW		
Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.				
DC Electrical Characteristics				
Symbol	Parameter	$V_{CC}$	74LVX573 $T_A = +25^\circ\text{C}$ Min Typ Max	74LVX573 $T_A = -40^\circ\text{C to } +85^\circ\text{C}$ Min Max
$V_{IH}$	High Level Input Voltage	2.0 3.0 3.6	1.5 2.0 2.4	1.5 2.0 2.4
$V_{IL}$	Low Level Input Voltage	2.0 3.0 3.6	0.5 0.8 0.8	0.5 0.8 0.8
$V_{OH}$	High Level Output Voltage	2.0 3.0 3.0	1.9 2.9 2.58	1.9 2.9 2.48
$V_{OL}$	Low Level Output Voltage	2.0 3.0 3.0	0.0 0.0 0.36	0.1 0.1 0.44
$I_{OZ}$	TRI-STATE Output Off-State Current	3.6	$\pm 0.25$	$\pm 2.5$
$I_{IN}$	Input Leakage Current	3.6	$\pm 0.1$	$\pm 1.0$
$I_{CC}$	Quiescent Supply Current	3.6	4.0	40.0

**Noise Characteristics:** See Section 2 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	74LVX573		Units	C <sub>L</sub> (pF)
			T <sub>A</sub> = 25°C			
			Typ	Limit		
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	3.3	0.5	0.8	V	50
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	3.3	−0.5	−0.8	V	50
V <sub>IHD</sub>	Minimum High Level Dynamic Input Voltage	3.3		2.0	V	50
V <sub>ILD</sub>	Maximum Low Level Dynamic Input Voltage	3.3		0.8	V	50

Note: (Input  $t_r = t_f = 3$  ns)**AC Electrical Characteristics:** See Section 2 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	74LVX573			74LVX573		Units	Conditions
			T <sub>A</sub> = +25°C			T <sub>A</sub> = −40°C to +85°C			
			Min	Typ	Max	Min	Max		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Time D <sub>n</sub> to O <sub>n</sub>	2.7		7.6	14.5	1.0	17.5	ns	C <sub>L</sub> = 15 pF
				10.1	18.0	1.0	21.0		C <sub>L</sub> = 50 pF
		3.3 ± 0.3		5.9	9.3	1.0	11.0		C <sub>L</sub> = 15 pF
				8.4	12.8	1.0	14.5		C <sub>L</sub> = 50 pF
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Time LE to O <sub>n</sub>	2.7		8.2	15.6	1.0	18.5	ns	C <sub>L</sub> = 15 pF
				10.7	19.1	1.0	22.0		C <sub>L</sub> = 50 pF
		3.3 ± 0.3		6.4	10.1	1.0	12.0		C <sub>L</sub> = 15 pF
				8.9	13.6	1.0	15.5		C <sub>L</sub> = 50 pF
t <sub>PZL</sub> t <sub>PZH</sub>	TRI-STATE® Output Enable Time	2.7		7.8	15.0	1.0	18.5	ns	C <sub>L</sub> = 15 pF, R <sub>L</sub> = 1 kΩ
				10.3	18.5	1.0	22.0		C <sub>L</sub> = 50 pF, R <sub>L</sub> = 1 kΩ
		3.3 ± 0.3		6.1	9.7	1.0	12.0		C <sub>L</sub> = 15 pF, R <sub>L</sub> = 1 kΩ
				8.6	13.2	1.0	15.5		C <sub>L</sub> = 50 pF, R <sub>L</sub> = 1 kΩ
t <sub>PLZ</sub> t <sub>PHZ</sub>	TRI-STATE® Output Disable Time	2.7		12.1	19.1	1.0	22.0	ns	C <sub>L</sub> = 50 pF, R <sub>L</sub> = 1 kΩ
		3.3 ± 0.3		10.1	13.6	1.0	15.5		C <sub>L</sub> = 50 pF, R <sub>L</sub> = 1 kΩ
t <sub>W</sub>	LE Pulse Width	2.7		6.5		7.5		ns	
		3.3 ± 0.3		5.0		5.0			
t <sub>S</sub>	Setup Time D <sub>n</sub> to LE	2.7		5.0		5.0		ns	
		3.3 ± 0.3		3.5		3.5			
t <sub>H</sub>	Hold Time D <sub>n</sub> to LE	2.7		1.5		1.5		ns	
		3.3 ± 0.3		1.5		1.5			
t <sub>OSHL</sub> t <sub>OSLH</sub>	Output to Output Skew (Note 1)	2.7			1.5		1.5	ns	C <sub>L</sub> = 50 pF

Note 1: Parameter guaranteed by design. t<sub>OSLH</sub> = |t<sub>PLHm</sub> - t<sub>PLHn</sub>|, t<sub>OSHL</sub> = |t<sub>PLHm</sub> - t<sub>PLHn</sub>|.

## Capacitance

Symbol	Parameter	74LVX573			74LVX573		Units
		T <sub>A</sub> = +25°C			T <sub>A</sub> = −40°C to +85°C		
		Min	Typ	Max	Min	Max	
C <sub>IN</sub>	Input Capacitance	4	10		10		pF
C <sub>OUT</sub>	Output Capacitance	6					pF
C <sub>PD</sub>	Power Dissipation Capacitance (Note 1)	27					pF

**Note 1:**  $C_{PD}$  is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:  $I_{CC(opr.)} = \frac{C_{PD} \times V_{CC} \times f_{IN} + I_{CC}}{8 \text{ (per latch)}}$

# Capacitance

Symbol	Parameter	74VX873		Units
		T <sub>A</sub> = +25°C		
		Min	Typ	
		Max	Max	
C <sub>IN</sub>	Input Capacitance	4	10	pF
C <sub>OUT</sub>	Output Capacitance	8		pF
C <sub>PD</sub>	Power Dissipation Capacitance (Note 1)	27		pF

Note 1: C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:  $I_{OP(avg)} = \frac{C_{PD} \times V_{CC} \times (f_{IN} + f_{OUT})}{2}$  (per lot).



## Section 9 Contents

9-3	LVQ Family Features
9-4	74LVQ00 Low Voltage Quad 2-Input NAND Gate
9-7	74LVQ02 Low Voltage Quad 2-Input NOR Gate
9-10	74LVQ04 Low Voltage Hex Inverter
9-13	74LVQ08 Low Voltage Quad 2-Input AND Gate
9-16	74LVQ14 Low Voltage Hex Inverter Schmitt Trigger Input
9-19	74LVQ32 Low Voltage Quad 2-Input OR Gate
9-22	74LVQ74 Low Voltage Dual D-Type Positive Edge-Triggered Flip-Flop
9-27	74LVQ86 Low Voltage Quad 2-Input XOR Gate
9-30	74LVQ125 Low Voltage Quad Buffer with TRI-STATE Outputs
9-34	74LVQ138 Low Voltage 3-Input Multiplexer
9-39	74LVQ151 Low Voltage 8-Input Multiplexer
9-44	74LVQ157 Low Voltage Quad 2-Input Multiplexer
9-49	74LVQ174 Low Voltage Hex D Flip-Flop with Master Reset
9-54	74LVQ240 Low Voltage Octal Buffer/Line Driver with TRI-STATE Outputs
9-58	74LVQ241 Low Voltage Octal Buffer/Line Driver with TRI-STATE Outputs
9-62	74LVQ244 Low Voltage Octal Buffer/Line Driver with TRI-STATE Outputs
9-65	74LVQ245 Low Voltage Octal Bidirectional Transceiver with TRI-STATE Outputs
9-69	74LVQ273 Low Voltage Octal D Flip-Flop
9-73	74LVQ273 Low Voltage Octal Transparent Latch with TRI-STATE Outputs
9-78	74LVQ274 Low Voltage Octal D Flip-Flop with TRI-STATE Outputs
9-83	74LVQ273 Low Voltage Octal Latch with TRI-STATE Outputs

## Section 9 LVQ Family

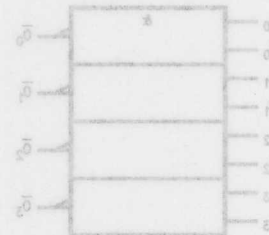
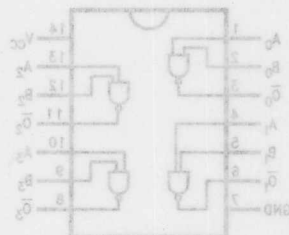


## Section 9 Contents

LVQ Family Features .....	9-3
74LVQ00 Low Voltage Quad 2-Input NAND Gate .....	9-4
74LVQ02 Low Voltage Quad 2-Input NOR Gate .....	9-7
74LVQ04 Low Voltage Hex Inverter .....	9-10
74LVQ08 Low Voltage Quad 2-Input AND Gate .....	9-13
74LVQ14 Low Voltage Hex Inverter Schmitt Trigger Input .....	9-16
74LVQ32 Low Voltage Quad 2-Input OR Gate .....	9-19
74LVQ74 Low Voltage Dual D-Type Positive Edge-Triggered Flip-Flop .....	9-22
74LVQ86 Low Voltage Quad 2-Input Exclusive-OR Gate .....	9-27
74LVQ125 Low Voltage Quad Buffer with TRI-STATE Outputs .....	9-30
74LVQ138 Low Voltage 1-of-8 Decoder/Demultiplexer .....	9-34
74LVQ151 Low Voltage 8-Input Multiplexer .....	9-39
74LVQ157 Low Voltage Quad 2-Input Multiplexer .....	9-44
74LVQ174 Low Voltage Hex D Flip-Flop with Master Reset .....	9-49
74LVQ240 Low Voltage Octal Buffer/Line Driver with TRI-STATE Outputs .....	9-54
74LVQ241 Low Voltage Octal Buffer/Line Driver with TRI-STATE Outputs .....	9-58
74LVQ244 Low Voltage Octal Buffer/Line Driver with TRI-STATE Outputs .....	9-62
74LVQ245 Low Voltage Octal Bidirectional Transceiver with TRI-STATE Outputs .....	9-65
74LVQ273 Low Voltage Octal D Flip-Flop .....	9-69
74LVQ373 Low Voltage Octal Transparent Latch with TRI-STATE Outputs .....	9-73
74LVQ374 Low Voltage Octal D Flip-Flop with TRI-STATE Outputs .....	9-78
74LVQ573 Low Voltage Octal Latch with TRI-STATE Outputs .....	9-83

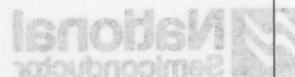
## LVQ Family Low Voltage Quiet CMOS Logic

Features	Advantages
Extended $V_{CC}$ range from 2.7V to 3.6V, compatible with JEDEC Std. No. 8-1B	Fully characterized for unregulated battery operation
1.5 $\mu$ m CMOS process	Good performance with propagation delays as fast as 9.5 ns max for octals
Low standby current ( $I_{CC}$ 40 $\mu$ A max for octal over temp)	Saves power, extends battery life
$\pm 12$ mA drive current	Balanced drive, guaranteed incident wave switching into 75 $\Omega$
SOIC, EIAJ-SOIC, and QSOP (octals only) packaging	Saves board space and weight; same form between QSOP (20 leads) and SOIC (14 leads)
Alternate source available	Product standardization. Ensured product supply



Pin Names	Description
$A_n, B_n$	Inputs
$O_n$	Outputs

Order Number	SOIC JEDEC	SOIC EIAJ
74LVQ00SC	74LVQ00SL	
74LVQ00SCX	74LVQ00SLX	
See NS Package Number	M14A	M14D



# 74LVQ00 Low Voltage Quad 2-Input NAND Gate

## General Description

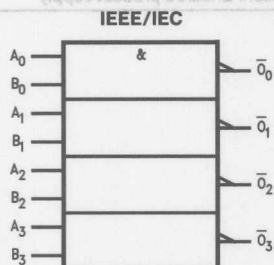
The LVQ00 contains four 2-input NAND gates.

## Features

- Ideal for low power/low noise 3.3V applications
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Guaranteed incident wave switching into 75Ω
- MIL-STD-883 54AC products are available for Military/Aerospace applications

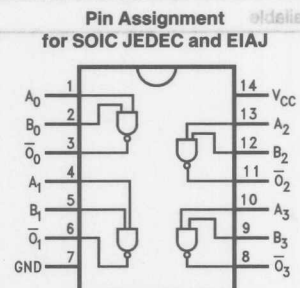
**Ordering Code:** See Section 11

## Logic Symbol



TL/F/11341-1

## Connection Diagram



TL/F/11341-2

Pin Names	Description
$A_n, B_n$	Inputs
$\bar{O}_n$	Outputs

	SOIC JEDEC	SOIC EIAJ
Order Number	74LVQ00SC 74LVQ00SCX	74LVQ00SJ 74LVQ00SJX
See NS Package Number	M14A	M14D

**Absolute Maximum Ratings** (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Input Diode Current ( $I_{IK}$ )	
$V_I = -0.5V$	-20 mA
$V_I = V_{CC} \pm 0.5V$	+20 mA
DC Input Voltage ( $V_I$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Diode Current ( $I_{OK}$ )	
$V_O = -0.5V$	-20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage ( $V_O$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Source or Sink Current ( $I_O$ )	$\pm 50$ mA
DC $V_{CC}$ or Ground Current ( $I_{CC}$ or $I_{GND}$ )	$\pm 200$ mA
Storage Temperature ( $T_{STG}$ )	-65°C to +150°C
DC Latch-Up Source or Sink Current	$\pm 100$ mA

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Recommended Operating Conditions**

Supply Voltage ( $V_{CC}$ )	2.0V to 3.6V
LVQ	
Input Voltage ( $V_I$ )	0V to $V_{CC}$
Output Voltage ( $V_O$ )	0V to $V_{CC}$
Operating Temperature ( $T_A$ )	-40°C to +85°C
74LVQ	
Minimum Input Edge Rate ( $\Delta V/\Delta t$ )	
$V_{IN}$ from 0.8V to 2.0V	
$V_{CC}$ @ 3.0V	125 mV/ns

**DC Characteristics**

Symbol	Parameter	V <sub>CC</sub> (V)	74LVQ00		74LVQ00	Units	Conditions
			T <sub>A</sub> = +25°C		T <sub>A</sub> = −40°C to +85°C		
			Typ	Guaranteed Limits			
V <sub>IH</sub>	Minimum High Level Input Voltage	3.0	1.5	2.0	2.0	V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> − 0.1V
V <sub>IL</sub>	Maximum Low Level Input Voltage	3.0	1.5	0.8	0.8	V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> − 0.1V
V <sub>OH</sub>	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I <sub>OUT</sub> = −50 μA
		3.0		2.58	2.48	V	*V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OH</sub> = −12 mA
V <sub>OL</sub>	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I <sub>OUT</sub> = 50 μA
		3.0		0.36	0.44	V	*V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OL</sub> = 12 mA
I <sub>IN</sub>	Maximum Input Leakage Current	3.6		±0.1	±1.0	μA	V <sub>I</sub> = V <sub>CC</sub> , GND

\*All outputs loaded; thresholds on input associated with output under test.

Symbol	Parameter	Units	Typ	Conditions
$C_{IN}$	Input Capacitance	pf	4.5	$V_{CC} = \text{Open}$
$C_{PD}$ (Note 1)	Power Dissipation Capacitance	pf	55	$V_{CC} = 3.3V$

Note 1:  $C_{PD}$  is measured at 10 MHz.

## DC Characteristics (Continued)

Symbol	Parameter	V <sub>CC</sub> (V)	74LVQ00		74LVQ00		Units	Conditions
			T <sub>A</sub> = +25°C		T <sub>A</sub> = -40°C to +85°C			
			Typ	Guaranteed Limits				
I <sub>OLD</sub>	†Minimum Dynamic Output Current	3.6			36		mA	V <sub>OLD</sub> = 0.8V Max (Note 1)
I <sub>OHD</sub>		3.6			-25		mA	V <sub>OHD</sub> = 2.0V Min (Note 1)
I <sub>CC</sub>	Maximum Quiescent Supply Current	3.6	2.0		20.0		μA	V <sub>IN</sub> = V <sub>CC</sub> or GND
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	3.3	0.6	1.0			V	(Notes 2, 3)
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	3.3	-0.5	-1.0			V	(Notes 2, 3)
V <sub>IHD</sub>	Maximum High Level Dynamic Input Voltage	3.3	1.5	2.0			V	(Notes 2, 4)
V <sub>ILD</sub>	Maximum Low Level Dynamic Input Voltage	3.3	1.5	0.8			V	(Notes 2, 4)

† Maximum test duration 2.0 ms, one output loaded at a time.

**Note 1:** Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed for 74LVQ.

**Note 2:** Worst case package.

**Note 3:** Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V; one output at GND.

**Note 4:** Max number of Data Inputs (n) switching. (n - 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V<sub>ILD</sub>), 0V to threshold (V<sub>IHD</sub>). f = 1 MHz.

## AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	74LVQ00			74LVQ00		Units
			T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF			T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF		
			Min	Typ	Max	Min	Max	
t <sub>PLH</sub>	Propagation Delay	2.7 3.3 ± 0.3	2.0 2.0	8.4 7.0	13.4 9.5	2.0 2.0	14.0 10.0	ns
t <sub>PHL</sub>	Propagation Delay	2.7 3.3 ± 0.3	1.5 1.5	6.6 5.5	11.3 8.0	1.0 1.0	12.0 8.5	ns
t <sub>OSHL</sub> t <sub>OSLH</sub>	Output to Output Skew*	2.7 3.3 ± 0.3		1.0 1.0	1.5 1.5		1.5 1.5	ns

\*Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t<sub>OSHL</sub>) or LOW to HIGH (t<sub>OSLH</sub>). Parameter guaranteed by design.

## Capacitance

Symbol	Parameter	Typ	Units	Conditions
C <sub>IN</sub>	Input Capacitance	4.5	pF	V <sub>CC</sub> = Open
C <sub>PD</sub> (Note 1)	Power Dissipation Capacitance	22	pF	V <sub>CC</sub> = 3.3V

**Note 1:** C<sub>PD</sub> is measured at 10 MHz.

# 74LVQ02

## Low Voltage Quad 2-Input NOR Gate

### General Description

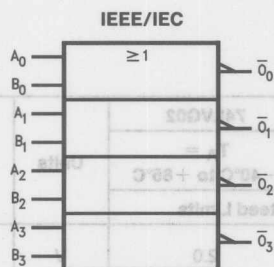
The LVQ02 contains four, 2-input NOR gates.

### Features

- Ideal for low power/low noise 3.3V applications
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Guaranteed incident wave switching into 75Ω
- MIL-STD-883 54AC products are available for Military/Aerospace applications

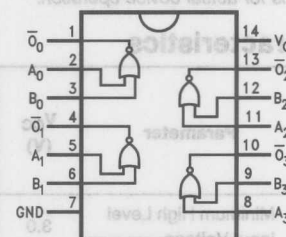
**Ordering Code:** See Section 11

### Logic Symbol



### Connection Diagram

Pin Assignment for  
SOIC JEDEC and EIAJ



TL/F/11342-1				TL/F/11342-2			
Pin	Symbol	Maximum Low Level Output Voltage	Minimum High Level Output Voltage	Pin	Symbol	Maximum Low Level Output Voltage	Minimum High Level Output Voltage
1	O <sub>0</sub>	0.8	2.9	1	O <sub>0</sub>	0.8	2.9
2	A <sub>0</sub>	0.8	2.9	2	A <sub>0</sub>	0.8	2.9
3	B <sub>0</sub>	0.8	2.9	3	B <sub>0</sub>	0.8	2.9
4	O <sub>1</sub>	0.8	2.9	4	O <sub>1</sub>	0.8	2.9
5	A <sub>1</sub>	0.8	2.9	5	A <sub>1</sub>	0.8	2.9
6	B <sub>1</sub>	0.8	2.9	6	B <sub>1</sub>	0.8	2.9
7	GND	0.8	2.9	7	GND	0.8	2.9
8	A <sub>3</sub>	0.8	2.9	8	A <sub>3</sub>	0.8	2.9
9	B <sub>3</sub>	0.8	2.9	9	B <sub>3</sub>	0.8	2.9
10	O <sub>3</sub>	0.8	2.9	10	O <sub>3</sub>	0.8	2.9
11	A <sub>2</sub>	0.8	2.9	11	A <sub>2</sub>	0.8	2.9
12	B <sub>2</sub>	0.8	2.9	12	B <sub>2</sub>	0.8	2.9
13	O <sub>2</sub>	0.8	2.9	13	O <sub>2</sub>	0.8	2.9
14	V <sub>CC</sub>	0.8	2.9	14	V <sub>CC</sub>	0.8	2.9

Pin Names	Description
A <sub>n</sub> , B <sub>n</sub>	Inputs
O <sub>n</sub>	Outputs

	SOIC JEDEC	SOIC EIAJ
Order Number	74LVQ02SC 74LVQ02SCX	74LVQ02SJ 74LVQ02SJX
See NS Package Number	M14A	M14D

**Absolute Maximum Ratings** (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Input Diode Current ( $I_{IK}$ )	-20 mA +20 mA
DC Input Voltage ( $V_I$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Diode Current ( $I_{OK}$ )	-20 mA +20 mA
DC Output Voltage ( $V_O$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Source or Sink Current ( $I_O$ )	$\pm 50$ mA
DC $V_{CC}$ or Ground Current ( $I_{CC}$ or $I_{GND}$ )	$\pm 200$ mA
Storage Temperature ( $T_{STG}$ )	-65°C to +150°C
DC Latch-Up Source or Sink Current	$\pm 100$ mA

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**DC Characteristics**

Symbol	Parameter	V <sub>CC</sub> (V)	74LVQ02		74LVQ02	Units	Conditions
			T <sub>A</sub> = +25°C		T <sub>A</sub> = −40°C to +85°C		
			Typ	Guaranteed Limits			
V <sub>IH</sub>	Minimum High Level Input Voltage	3.0	1.5	2.0	2.0	V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> − 0.1V
V <sub>IL</sub>	Maximum Low Level Input Voltage	3.0	1.5	0.8	0.8	V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> − 0.1V
V <sub>OH</sub>	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I <sub>OUT</sub> = −50 μA
		3.0		2.58	2.48	V	*V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OH</sub> = −12 mA
V <sub>OL</sub>	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I <sub>OUT</sub> = 50 μA
		3.0		0.36	0.44	V	*V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OL</sub> = 12 mA
I <sub>IN</sub>	Maximum Input Leakage Current	3.6		±0.1	±1.0	μA	V <sub>I</sub> = V <sub>CC</sub> , GND

\*All outputs loaded; thresholds on input associated with output under test.

**Recommended Operating Conditions**

Supply Voltage ( $V_{CC}$ )	2.0V to 3.6V
LVQ	0V to $V_{CC}$
Input Voltage ( $V_I$ )	0V to $V_{CC}$
Output Voltage ( $V_O$ )	0V to $V_{CC}$
Operating Temperature ( $T_A$ )	-40°C to +85°C
74LVQ	
Minimum Input Edge Rate ( $\Delta V/\Delta t$ )	125 mV/ns
$V_{IN}$ from 0.8V to 2.0V	
$V_{CC} @ 3.0V$	

Order Number	74LVQ02SC	74LVQ02SL
See NS Package Number	M14	M1D

## DC Characteristics (Continued)

Symbol	Parameter	V <sub>CC</sub> (V)	74LVQ02		74LVQ02		Units	Conditions
			T <sub>A</sub> = +25°C		T <sub>A</sub> = −40°C to +85°C			
			Typ	Guaranteed Limits				
I <sub>OLD</sub>	†Minimum Dynamic Output Current	3.6			36	mA	V <sub>OLD</sub> = 0.8V Max (Note 1)	
I <sub>OHD</sub>		3.6			−25	mA	V <sub>OHD</sub> = 2.0V Min (Note 1)	
I <sub>CC</sub>	Maximum Quiescent Supply Current	3.6		2.0	20.0	μA	V <sub>IN</sub> = V <sub>CC</sub> or GND	
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	3.3	0.6	1.0		V	(Notes 2 & 3)	
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	3.3	−0.7	−1.0		V	(Notes 2 & 3)	
V <sub>IHD</sub>	Maximum High Level Dynamic Input Voltage	3.3	1.7	2.0		V	(Notes 2 & 4)	
V <sub>ILD</sub>	Maximum Low Level Dynamic Input Voltage	3.3	1.7	0.8		V	(Notes 2 & 4)	

†Maximum test duration 2.0 ms, one output loaded at a time.

**Note 1:** Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed for 74LVQ.

**Note 2:** Worst case package.

**Note 3:** Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V; one output at GND.

**Note 4:** Max number of Data Inputs (n) switching: (n − 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V<sub>ILD</sub>), 0V to threshold (V<sub>IHD</sub>), f = 1 MHz.

## AC Electrical Characteristics: See Section 2 for Test Waveforms and Output Load

Symbol	Parameter	V <sub>CC</sub> (V)	74LVQ02			74LVQ02		Units
			T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF			T <sub>A</sub> = −40°C to +85°C C <sub>L</sub> = 50 pF		
			Min	Typ	Max	Min	Max	
t <sub>PLH</sub>	Propagation Delay	2.7 3.3 ± 0.3	1.5 1.5	6.0 5.0	10.6 7.5	1.0 1.0	12.0 8.0	ns
t <sub>PHL</sub>	Propagation Delay	2.7 3.3 ± 0.3	1.5 1.5	6.0 5.0	10.6 7.5	1.0 1.0	12.0 8.0	ns
t <sub>OSHL</sub> , t <sub>OSLH</sub>	Output to Output Skew* Data to Output	2.7 3.3 ± 0.3		1.0 1.0	1.5 1.5		1.5 1.5	ns

\*Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t<sub>OSHL</sub>) or LOW to HIGH (t<sub>OSLH</sub>). Parameter guaranteed by design.

## Capacitance

Symbol	Parameter	Typ	Units	Conditions
C <sub>IN</sub>	Input Capacitance	4.5	pF	V <sub>CC</sub> = Open
C <sub>PD</sub> (Note 1)	Power Dissipation Capacitance	20	pF	V <sub>CC</sub> = 3.3V

**Note 1:** C<sub>PD</sub> is measured at 10 MHz.

# 74LVQ04

## Low Voltage Hex Inverter

### General Description

The LVQ04 contains six inverters.

### Features

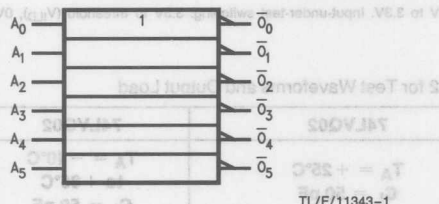
- Ideal for low power/low noise 3.3V applications
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Guaranteed incident wave switching into 75Ω
- MIL-STD-883 54AC Products are available for Military/Aerospace Applications

**Ordering Code:** See Section 11

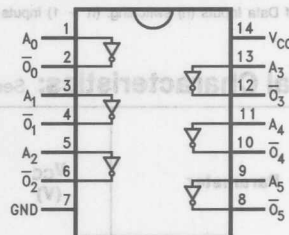
### Logic Symbol

### Connection Diagram

IEEE/IEC



Pin Assignment  
for SOIC JEDEC and EIAJ



Symbol	Parameter	Units	Typ	Min	Max
t <sub>pd</sub>	Propagation Delay	ns	8.0	1.0	15.0
	Output to Output Skew*	ns	1.5	1.0	1.5
t <sub>pd</sub>	Propagation Delay	ns	8.0	1.0	15.0
	Output to Output Skew*	ns	1.5	1.0	1.5

Pin Names	Description
A <sub>n</sub>	Inputs
O <sub>n</sub>	Outputs

Symbol	Parameter	Units	Typ
C <sub>in</sub>	Input Capacitance	pF	4.5
C <sub>pd</sub> (Note 1)	Power Dissipation Capacitance	pF	50

	SOIC JEDEC	SOIC EIAJ
Order Number	74LVQ04SC 74LVQ04SCX	74LVQ04SJ 74LVQ04SJX
See NS Package Number	M14A	M14D

**Absolute Maximum Ratings** (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Input Diode Current ( $I_{IK}$ )	-20 mA
$V_I = -0.5V$	-20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage ( $V_I$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Diode Current ( $I_{OK}$ )	-20 mA
$V_O = -0.5V$	-20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage ( $V_O$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Source or Sink Current ( $I_O$ )	±50 mA
DC $V_{CC}$ or Ground Current ( $I_{CC}$ or $I_{GND}$ )	±200 mA
Storage Temperature ( $T_{STG}$ )	-65°C to +150°C
DC Latch-Up Source or Sink Current	±100 mA

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Recommended Operating Conditions**

Supply Voltage ( $V_{CC}$ )	2.0V to 3.6V
LVQ	0V to $V_{CC}$
Input Voltage ( $V_I$ )	0V to $V_{CC}$
Output Voltage ( $V_O$ )	0V to $V_{CC}$
Operating Temperature ( $T_A$ )	-40°C to +85°C
74LVQ	125 mV/ns
Minimum Input Edge Rate ( $\Delta V/\Delta t$ )	$V_{IN}$ from 0.8V to 2.0V
$V_{CC}$ @ 3.0V	

**DC Characteristics**

Symbol	Parameter	V <sub>CC</sub> (V)	74LVQ04		74LVQ04		Units	Conditions
			T <sub>A</sub> = +25°C		T <sub>A</sub> = −40°C to +85°C			
			Typ	Guaranteed Limits				
V <sub>IH</sub>	Minimum High Level Input Voltage	3.0	1.5	2.0	2.0		V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> − 0.1V
V <sub>IL</sub>	Maximum Low Level Input Voltage	3.0	1.5	0.8	0.8		V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> − 0.1V
V <sub>OH</sub>	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9		V	I <sub>OUT</sub> = −50 μA
		3.0		2.58	2.48		V	*V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OH</sub> = −12 mA
V <sub>OL</sub>	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1		V	I <sub>OUT</sub> = 50 μA
		3.0		0.36	0.44		V	*V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OL</sub> = 12 mA
I <sub>IN</sub>	Maximum Input Leakage Current	3.6		±0.1	±1.0		μA	V <sub>I</sub> = V <sub>CC</sub> , GND

\*All outputs loaded; thresholds on input associated with output under test.

# DC Characteristics (Continued)

Symbol	Parameter	V <sub>CC</sub> (V)	74LVQ04		74LVQ04		Units	Conditions
			T <sub>A</sub> = +25°C		T <sub>A</sub> = −40°C to +85°C			
			Typ	Guaranteed Limits				
I <sub>OLD</sub>	†Minimum Dynamic Output Current	3.6			36	mA	V <sub>OLD</sub> = 0.8V Max (Note 1)	
I <sub>OHD</sub>		3.6			−25	mA	V <sub>OHD</sub> = 2.0V Min (Note 1)	
I <sub>CC</sub>	Maximum Quiescent Supply Current	3.6		2.0		20.0	μA	V <sub>IN</sub> = V <sub>CC</sub> or GND
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	3.3	0.8	1.1			V	(Notes 2 & 3)
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	3.3	−0.8	−1.1			V	(Notes 2 & 3)
V <sub>IHD</sub>	Maximum High Level Dynamic Input Voltage	3.3	1.7	2.0			V	(Notes 2 & 4)
V <sub>ILD</sub>	Maximum Low Level Dynamic Input Voltage	3.3	1.6	0.8			V	(Notes 2 & 4)

†Maximum test duration 2.0 ms, one output loaded at a time.

**Note 1:** Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed for 74LVQ.

**Note 2:** Worst case package.

**Note 3:** Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V; one output at GND.

**Note 4:** Max number of Data Inputs (n) switching. (n - 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V<sub>ILD</sub>) 0V to threshold (V<sub>IHD</sub>) f = 1 MHz.

## AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	74LVQ04			74LVQ04		Units
			T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF			T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF		
			Min	Typ	Max	Min	Max	
t <sub>PLH</sub>	Propagation Delay	2.7 3.3 ± 0.3	1.5	5.4	12.7	1.0	14.0	ns
t <sub>PHL</sub>	Propagation Delay	2.7 3.3 ± 0.3	1.5	5.4	12.0	1.0	12.0	ns
t <sub>OSSL</sub> t <sub>OSLH</sub>	Output to Output Skew* Data to Output	2.7 3.3 ± 0.3		1.0	1.5		1.5	ns

\*Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t<sub>OSSL</sub>) or LOW to HIGH (t<sub>OSLH</sub>). Parameter guaranteed by design.

## Capacitance

Symbol	Parameter	Typ	Units	Conditions
C <sub>IN</sub>	Input Capacitance	4.5	pF	V <sub>CC</sub> = Open
C <sub>PD</sub> (Note 1)	Power Dissipation Capacitance	17	pF	V <sub>CC</sub> = 3.3V

**Note 1:** C<sub>PD</sub> is measured at 10 MHz.



# 74LVQ08

## Low Voltage Quad 2-Input AND Gate

### General Description

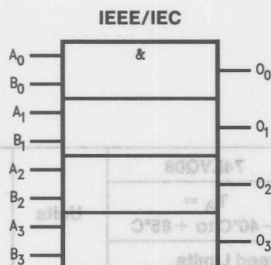
The LVQ08 contains four, 2-input AND gates.

### Features

- Ideal for low power/low noise 3.3V applications
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Guaranteed incident wave switching into 75Ω
- MIL-STD-883 54AC products are available for Military/Aerospace applications

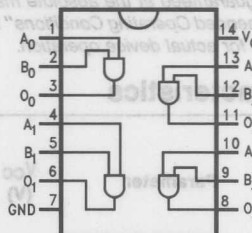
**Ordering Code:** See Section 11

### Logic Symbol



### Connection Diagram

Pin Assignment  
for SOIC JEDEC and EIAJ



Symbol	Pin	Pin Name	Description	Typ	TA = +25°C	TL/F/11344-1	TL/F/11344-2
V <sub>OH</sub>	11	O <sub>2</sub>	Outputs	3.0	2.8	2.8	Minimum High Level Output Voltage
				3.0	2.8	2.8	Minimum High Level Input Voltage
V <sub>OL</sub>	10	A <sub>3</sub>	Inputs	3.0	2.8	2.8	Maximum Low Level Output Voltage
				3.0	2.8	2.8	Maximum Low Level Input Voltage
V <sub>CC</sub>	14	V <sub>CC</sub>	Power Supply	3.0	2.8	2.8	Maximum Input Leakage Current
				3.0	2.8	2.8	Maximum Input Leakage Current

	SOIC JEDEC	SOIC EIAJ
Order Number	74LVQ08SC 74LVQ08SCX	74LVQ08SJ 74LVQ08SJX
See NS Package Number	M14A	M14D

## Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )  $-0.5V$  to  $+7.0V$

DC Input Diode Current ( $I_{IK}$ )

$V_I = -0.5V$   $-20\text{ mA}$   
 $V_I = V_{CC} + 0.5V$   $+20\text{ mA}$

DC Input Voltage ( $V_I$ )  $-0.5V$  to  $V_{CC} + 0.5V$

DC Output Diode Current ( $I_{OK}$ )

$V_O = -0.5V$   $-20\text{ mA}$   
 $V_O = V_{CC} + 0.5V$   $+20\text{ mA}$

DC Output Voltage ( $V_O$ )  $-0.5V$  to  $V_{CC} + 0.5V$

DC Output Source or Sink Current ( $I_O$ )  $\pm 50\text{ mA}$

DC  $V_{CC}$  or Ground Current ( $I_{CC}$  or  $I_{GND}$ )  $\pm 200\text{ mA}$

Storage Temperature ( $T_{STG}$ )  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$

DC Latch-Up Source or Sink Current  $\pm 100\text{ mA}$

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## DC Characteristics

Symbol	Parameter	V <sub>CC</sub> (V)	74LVQ08		74LVQ08	Units	Conditions
			T <sub>A</sub> = +25°C		T <sub>A</sub> = −40°C to +85°C		
			Typ	Guaranteed Limits			
V <sub>IH</sub>	Minimum High Level Input Voltage	3.0	1.5	2.0	2.0	V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> − 0.1V
V <sub>IL</sub>	Maximum Low Level Input Voltage	3.0	1.5	0.8	0.8	V	V <sub>OUT</sub> = 0.1V
V <sub>OH</sub>	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I <sub>OUT</sub> = −50 μA
		3.0		2.58	2.48	V	*V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OH</sub> = −12 mA
V <sub>OL</sub>	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I <sub>OUT</sub> = 50 μA
		3.0		0.36	0.44	V	*V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OL</sub> = 12 mA
I <sub>IN</sub>	Maximum Input Leakage Current	3.6		±0.1	±1.0	μA	V <sub>I</sub> = V <sub>CC</sub> , GND

\*All outputs loaded; thresholds on input associated with output under test.

## Recommended Operating Conditions

Supply Voltage ( $V_{CC}$ )

LVQ 2.0V to 3.6V

Input Voltage ( $V_I$ )

0V to  $V_{CC}$

Output Voltage ( $V_O$ )

0V to  $V_{CC}$

Operating Temperature ( $T_A$ )

74LVQ  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$

Minimum Input Edge Rate ( $\Delta V/\Delta t$ )

$V_{IN}$  from 0.8V to 2.0V

$V_{CC}$  @ 3.0V 125 mV/ns

**DC Characteristics** (Continued)

Symbol	Parameter	V <sub>CC</sub> (V)	74LVQ08		74LVQ08		Units	Conditions
			T <sub>A</sub> = +25°C		T <sub>A</sub> = −40°C to +85°C			
			Typ	Guaranteed Limits				
I <sub>OLD</sub>	†Minimum Dynamic	3.6			36		mA	V <sub>OLD</sub> = 0.8V Max (Note 1)
I <sub>OHD</sub>	Output Current	3.6			−25		mA	V <sub>OHD</sub> = 2.0V Min (Note 1)
I <sub>CC</sub>	Maximum Quiescent Supply Current	3.6		2.0	20.0		μA	V <sub>IN</sub> = V <sub>CC</sub> or GND
V <sub>OLP</sub>	Quiet Output	3.3	0.4	0.8			V	(Notes 2 & 3)
	Maximum Dynamic V <sub>OL</sub>							
V <sub>OLV</sub>	Quiet Output	3.3	−0.4	−0.8			V	(Notes 2 & 3)
	Minimum Dynamic V <sub>OL</sub>							
V <sub>IHD</sub>	Maximum High Level Dynamic Input Voltage	3.3	1.8	2.0			V	(Notes 2 & 4)
V <sub>ILD</sub>	Maximum Low Level Dynamic Input Voltage	3.3	1.8	0.8			V	(Notes 2 & 4)

†Maximum test duration 2.0 ms, one output loaded at a time.

**Note 1:** Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed for 74LVQ.

**Note 2:** Worst case package.

**Note 3:** Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V; one output at GND.

**Note 4:** Max number of Data Inputs (n) switching. (n - 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V<sub>ILD</sub>), 0V to threshold (V<sub>IHD</sub>), f = 1 MHz.

**AC Electrical Characteristics:** See Section 2 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	74LVQ08			74LVQ08		Units
			T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF			T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF		
			Min	Typ	Max	Min	Max	
t <sub>PLH</sub>	Propagation Delay	2.7 3.3 ± 0.3	1.5 1.5	9.0 7.5	13.4 9.5	1.0 1.0	14.0 10.0	ns
t <sub>PHL</sub>	Propagation Delay	2.7 3.3 ± 0.3	1.5 1.5	8.4 7.0	12.0 8.5	1.0 1.0	13.0 9.0	ns
t <sub>OSHL</sub> , t <sub>OSLH</sub>	Output to Output Skew*	2.7 3.3 ± 0.3		1.0 1.0	1.5 1.5		1.5 1.5	ns

\*Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t<sub>OSHL</sub>) or LOW to HIGH (t<sub>OSLH</sub>). Parameter guaranteed by design.

**Capacitance**

Symbol	Parameter	Typ	Units	Conditions
C <sub>IN</sub>	Input Capacitance	4.5	pF	V <sub>CC</sub> = Open
C <sub>PD</sub> (Note 1)	Power Dissipation Capacitance	17	pF	V <sub>CC</sub> = 3.3V

**Note 1:** C<sub>PD</sub> is measured at 10 MHz.



## 74LVQ14

### Low Voltage Hex Inverter with Schmitt Trigger Input

#### General Description

The LVQ14 contains six inverter gates each with a Schmitt trigger input. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. In addition, they have a greater noise margin than conventional inverters.

The LVQ14 has hysteresis between the positive-going and negative-going input thresholds (typically 1.0V) which is determined internally by transistor ratios and is essentially insensitive to temperature and supply voltage variations.

#### Features

- Ideal for low power/low noise 3.3V applications
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Guaranteed incident wave switching into 75Ω
- MIL-STD-883 54AC products are available for Military/Aerospace applications

**Ordering Code:** See Section 11

#### Logic Symbol

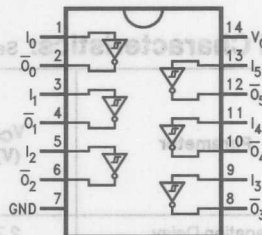
IEEE/IEC



TL/F/11345-1

#### Connection Diagram

Pin Assignment  
for SOIC JEDEC and EIAJ



TL/F/11345-2

#### Pin Names

$I_n$   
 $O_n$

#### Description

Inputs  
Outputs

#### Truth Table

Input	Output
A	$\bar{O}$
L	H
H	L

	SOIC JEDEC	SOIC EIAJ
Order Number	74LVQ14SC 74LVQ14SCX	74LVQ14SJ 74LVQ14SJX
See NS Package Number	M14A	M14D

**Absolute Maximum Ratings** (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Input Diode Current ( $I_{IK}$ )	-20 mA
$V_I = -0.5V$	
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage ( $V_I$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Diode Current ( $I_{OK}$ )	-20 mA
$V_O = -0.5V$	
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage ( $V_O$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Source or Sink Current ( $I_O$ )	±50 mA
DC $V_{CC}$ or Ground Current ( $I_{CC}$ or $I_{GND}$ )	±200 mA
Storage Temperature ( $T_{STG}$ )	-65°C to +150°C
DC Latch-Up Source or Sink Current	±100 mA

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Recommended Operating Conditions**

Supply Voltage ( $V_{CC}$ )	2.0V to 3.6V
LVQ	
Input Voltage ( $V_I$ )	0V to $V_{CC}$
Output Voltage ( $V_O$ )	0V to $V_{CC}$
Operating Temperature ( $T_A$ )	-40°C to +85°C
74LVQ	
Minimum Input Edge Rate ( $\Delta V/\Delta t$ )	125 mV/ns
$V_{IN}$ from 0.8V to 2.0V	
$V_{CC} @ 3.0V$	

**DC Characteristics**

Symbol	Parameter	V <sub>CC</sub> (V)	74LVQ14		74LVQ14		Units	Conditions
			T <sub>A</sub> = +25°C		T <sub>A</sub> = −40°C to +85°C			
			Typ	Guaranteed Limits				
V <sub>OH</sub>	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I <sub>OUT</sub> = −50 μA	
		3.0		2.58	2.48	V	*V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OH</sub> = −12 mA	
V <sub>OL</sub>	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I <sub>OUT</sub> = 50 μA	
		3.0		0.36	0.44	V	*V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OL</sub> = 12 mA	
I <sub>IN</sub>	Maximum Input Leakage Current	3.6		±0.1	±1.0	μA	V <sub>I</sub> = V <sub>CC</sub> , GND	
V <sub>t+</sub>	Maximum Positive Threshold	3.0		2.2	2.2	V	T <sub>A</sub> = Worst Case	
V <sub>t−</sub>	Minimum Negative Threshold	3.0		0.5	0.5	V	T <sub>A</sub> = Worst Case	

\*All outputs loaded; thresholds on input associated with output under test.

Symbol	Parameter	Typ
$C_{in}$	Input Capacitance	4.5
$C_{pd}$	Power Dissipation Capacitance	50
		$V_{CC} = 3.3V$
		$V_{CC} = \text{Open}$

Note 1:  $C_{pd}$  is measured at 10 MHz.

Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = +25°C		T <sub>A</sub> = −40°C to +85°C		Units	Conditions
			Typ	Guaranteed Limits				
V <sub>h(max)</sub>	Maximum Hysteresis	3.0	1.2		1.2		V	T <sub>A</sub> = Worst Case
V <sub>h(min)</sub>	Minimum Hysteresis	3.0	0.3		0.3		V	T <sub>A</sub> = Worst Case
I <sub>OLD</sub>	†Minimum Dynamic Output Current	3.6			36		mA	V <sub>OLD</sub> = 0.8V Max (Note 1)
I <sub>OHD</sub>		3.6			−25		mA	V <sub>OHD</sub> = 2.0V Min (Note 1)
I <sub>CC</sub>	Maximum Quiescent Supply Current	3.6		2.0	20.0		μA	V <sub>IN</sub> = V <sub>CC</sub> or GND
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	3.3	0.9	1.1			V	(Notes 2, 3)
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	3.3	−0.8	−1.1			V	(Notes 2, 3)
V <sub>IHD</sub>	Maximum High Level Dynamic Input Voltage	3.3	1.9	2.0			V	(Notes 2, 4)
V <sub>ILD</sub>	Maximum Low Level Dynamic Input Voltage	3.3	1.3	2.0			V	(Notes 2, 4)

† Maximum test duration 2.0 ms, one output loaded at a time.

**Note 1:** Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed for 74LVQ.

**Note 2:** Worst case package.

**Note 3:** Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V; one output at GND.

**Note 4:** Max number of Data Inputs (n) switching. (n − 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V<sub>ILD</sub>), 0V to threshold (V<sub>IHD</sub>), f = 1 MHz.

## AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	74LVQ14			74LVQ14		Units
			T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF			T <sub>A</sub> = −40°C to +85°C C <sub>L</sub> = 50 pF		
			Min	Typ	Max	Min	Max	
t <sub>PLH</sub>	Propagation Delay	2.7	1.5	11.4	19.0	1.5	21.0	ns
		3.3 ±0.3	1.5	9.5	13.5	1.5	15.0	
t <sub>PHL</sub>	Propagation Delay	2.7	1.5	9.0	16.2	1.5	19.0	ns
		3.3 ±0.3	1.5	7.5	11.5	1.5	13.0	
t <sub>OSHL</sub> , t <sub>OSLH</sub> *	Output to Output Skew*	2.7		1.0	1.5		1.5	ns
		3.3 ±0.3		1.0	1.5		1.5	
	Data to Output							

\* Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t<sub>OSHL</sub>) or LOW to HIGH (t<sub>OSLH</sub>). Parameter guaranteed by design.

## Capacitance

Symbol	Parameter	Typ	Units	Conditions
C <sub>IN</sub>	Input Capacitance	4.5	pF	V <sub>CC</sub> = Open
C <sub>PD</sub> (Note 1)	Power Dissipation Capacitance	20	pF	V <sub>CC</sub> = 3.3V

**Note 1:** C<sub>PD</sub> is measured at 10 MHz.



## 74LVQ32

### Low Voltage Quad 2-Input OR Gate

## General Description

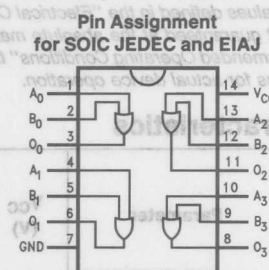
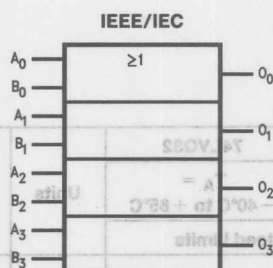
The LVQ32 contains four, 2-input OR gates.

## Features

- Ideal for low power/low noise 3.3V applications
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Guaranteed incident wave switching into 75 $\Omega$
- MIL-STD-883 54AC products are available for Military/Aerospace applications

**Ordering Code:** See Section 11

### Logic Symbol

[illegible]

	SOIC JEDEC	SOIC EIAJ
Order Number	74LVQ32SC 74LVQ32SCX	74LVQ32SJ 74LVQ32SJX
See NS Package Number	M14A	M14D

**Absolute Maximum Ratings** (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Input Diode Current ( $I_{IK}$ )	-20 mA
$V_I = -0.5V$	+20 mA
$V_I = V_{CC} + 0.5V$	
DC Input Voltage ( $V_I$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Diode Current ( $I_{OK}$ )	-20 mA
$V_O = -0.5V$	+20 mA
$V_O = V_{CC} + 0.5V$	
DC Output Voltage ( $V_O$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Source or Sink Current ( $I_O$ )	$\pm 50$ mA
DC $V_{CC}$ or Ground Current ( $I_{CC}$ or $I_{GND}$ )	$\pm 200$ mA
Storage Temperature ( $T_{STG}$ )	-65°C to +150°C
DC Latch-Up Source or Sink Current	$\pm 100$ mA

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**DC Characteristics**

Symbol	Parameter	V <sub>CC</sub> (V)	74LVQ32		74LVQ32	Units	Conditions
			T <sub>A</sub> = +25°C		T <sub>A</sub> = −40°C to +85°C		
			Typ	Guaranteed Limits			
V <sub>IH</sub>	Minimum High Level Input Voltage	3.0	1.5	2.0	2.0	V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> − 0.1V
V <sub>IL</sub>	Maximum Low Level Input Voltage	3.0	1.5	0.8	0.8	V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> − 0.1V
V <sub>OH</sub>	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I <sub>OUT</sub> = −50 μA
		3.0		2.58	2.48	V	*V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OH</sub> = −12 mA
V <sub>OL</sub>	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I <sub>OUT</sub> = 50 μA
		3.0		0.36	0.44	V	*V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OL</sub> = 12 mA
I <sub>IN</sub>	Maximum Input Leakage Current	3.6		±0.1	±1.0	μA	V <sub>I</sub> = V <sub>CC</sub> , GND

\*All outputs loaded; thresholds on input associated with output under test.

**Recommended Operating Conditions**

Supply Voltage ( $V_{CC}$ )	2.0V to 3.6V
LVQ	
Input Voltage ( $V_I$ )	0V to $V_{CC}$
Output Voltage ( $V_O$ )	0V to $V_{CC}$
Operating Temperature ( $T_A$ )	-40°C to +85°C
74LVQ	
Minimum Input Edge Rate ( $\Delta V/\Delta t$ )	125 mV/ns
$V_{IN}$ from 0.8V to 2.0V	
$V_{CC}$ @ 3.0V	

Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = +25°C		Units	Conditions
			Typ	Guaranteed Limits		
I <sub>OLD</sub>	† Minimum Dynamic Output Current	3.6		36	mA	V <sub>OLD</sub> = 0.8V Max (Note 1)
I <sub>OHD</sub>		3.6		25	mA	V <sub>OHD</sub> = 2.0V Min (Note 1)
I <sub>CC</sub>	Maximum Quiescent Supply Current	3.6	2.0	20.0	μA	V <sub>IN</sub> = V <sub>CC</sub> or GND
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	3.3	0.5	0.8	V	(Notes 2 & 3)
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	3.3	-0.5	-0.8	V	(Notes 2 & 3)
V <sub>IHD</sub>	Maximum High Level Dynamic Input Voltage	3.3	1.9	2.0	V	(Notes 2 & 4)
V <sub>ILD</sub>	Maximum Low Level Dynamic Input Voltage	3.3	1.8	0.8	V	(Notes 2 & 4)

† Maximum test duration 2.0 ms, one output loaded at a time.

**Note 1:** Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed for 74LVQ.

**Note 2:** Worst case package.

**Note 3:** Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V; one output at GND.

**Note 4:** Max number of Data Inputs (n) switching. (n - 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V<sub>ILD</sub>), 0V to threshold (V<sub>IHD</sub>), f = 1 MHz.

## AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	74LVQ32			74LVQ32		Units
			T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF			T <sub>A</sub> = −40°C to +85°C C <sub>L</sub> = 50 pF		
			Min	Typ	Max	Min	Max	
t <sub>PLH</sub>	Propagation Delay	2.7 3.3 ± 0.3	1.5 1.5	8.4 7.0	12.7 9.0	1.5 1.5	14.0 10.0	ns
t <sub>PHL</sub>	Propagation Delay	2.7 3.3 ± 0.3	1.5 1.5	8.4 7.0	12.0 8.5	1.0 1.5	13.0 9.0	ns
t <sub>OSHL</sub> , t <sub>OSLH</sub>	Output to Output Skew*	2.7 3.3 ± 0.3		1.0 1.0	1.5 1.5		1.5 1.5	ns

\*Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t<sub>OSHL</sub>) or LOW to HIGH (t<sub>OSLH</sub>). Parameter guaranteed by design.

## Capacitance

Symbol	Parameter	Typ	Units	Conditions
C <sub>IN</sub>	Input Capacitance	4.5	pF	V <sub>CC</sub> = Open
C <sub>PD</sub> (Note 1)	Power Dissipation Capacitance	17	pF	V <sub>CC</sub> = 3.3V

**Note 1:** C<sub>PD</sub> is measured at 10 MHz.



## 74LVQ74

### Low Voltage Dual D-Type Positive Edge-Triggered Flip-Flop

#### General Description

The LVQ74 is a dual D-type flip-flop with Asynchronous Clear and Set inputs and complementary ( $Q$ ,  $\bar{Q}$ ) outputs. Information at the input is transferred to the outputs on the positive edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. After the Clock Pulse input threshold voltage has been passed, the Data input is locked out and information present will not be transferred to the outputs until the next rising edge of the Clock Pulse input.

#### Asynchronous Inputs:

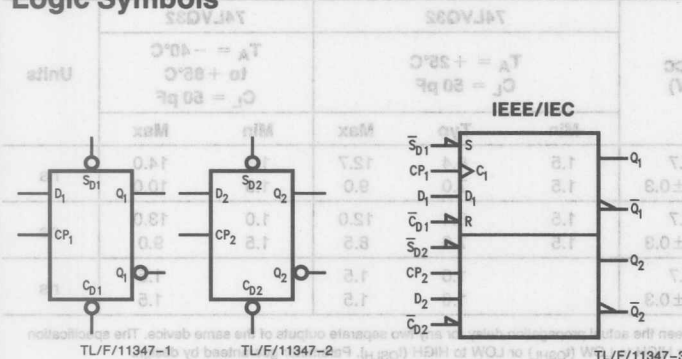
- LOW input to  $\bar{S}_D$  (Set) sets  $Q$  to HIGH level
- LOW input to  $\bar{C}_D$  (Clear) sets  $Q$  to LOW level
- Clear and Set are independent of clock
- Simultaneous LOW on  $\bar{C}_D$  and  $\bar{S}_D$  makes both  $Q$  and  $\bar{Q}$  HIGH

#### Features

- Ideal for low power/low noise 3.3V applications
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Guaranteed incident wave switching into 75 $\Omega$
- MIL-STD-883 54AC products are available for Military/Aerospace applications

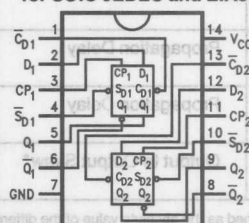
**Ordering Code:** See Section 11

#### Logic Symbols



#### Connection Diagram

Pin Assignment for SOIC JEDEC and EIAJ



Pin Names	Description
$D_1, D_2$	Data Inputs
$CP_1, CP_2$	Clock Pulse Inputs
$\bar{C}_D1, \bar{C}_D2$	Direct Clear Inputs
$\bar{S}_D1, \bar{S}_D2$	Direct Set Inputs
$Q_1, \bar{Q}_1, Q_2, \bar{Q}_2$	Outputs

	SOIC JEDEC	SOIC EIAJ
Order Number	74LVQ74SC 74LVQ74SCX	74LVQ74SJ 74LVQ74SJX
See NS Package Number	M14A	M14D

Truth Table (Each Half)

Inputs			Outputs		
$\bar{S}_D$	$\bar{C}_D$	CP	D	Q	$\bar{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H
H	H	X	X	H	L
H	H	X	L	L	H
H	H	L	X	Q <sub>0</sub>	$\bar{Q}_0$

H = HIGH Voltage Level

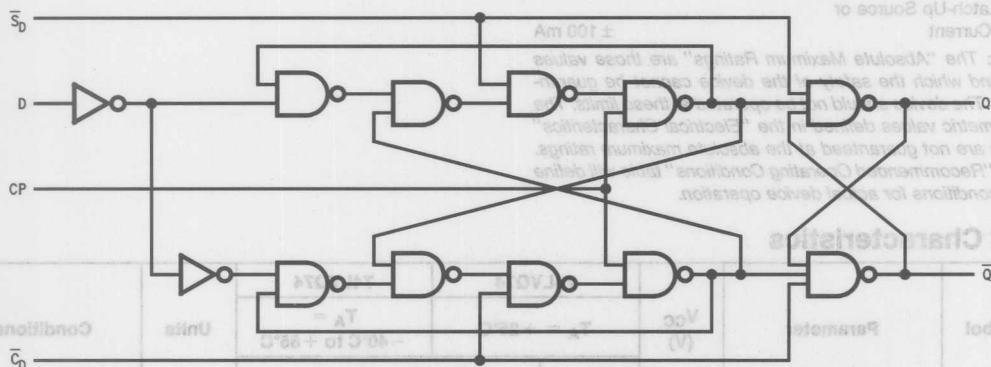
L = LOW Voltage Level

X = Immaterial

/ = LOW-to-HIGH Clock Transition

Q<sub>0</sub>( $\bar{Q}_0$ ) = Previous Q( $\bar{Q}$ ) before LOW-to-HIGH Transition of Clock

Logic Diagram



(Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.)

Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> (°C)	Units	Conditions
V <sub>OH</sub>	Minimum High Level Output Voltage	3.0	2.0	V	V <sub>OH</sub> = V <sub>CC</sub> - 0.1V
	Minimum High Level Input Voltage	3.0	2.0	V	V <sub>OH</sub> = V <sub>CC</sub> - 0.1V
V <sub>OL</sub>	Maximum Low Level Output Voltage	3.0	2.0	V	V <sub>OL</sub> = 0.1V
	Maximum Low Level Input Voltage	3.0	2.0	V	V <sub>OL</sub> = 0.1V
I <sub>IN</sub>	Maximum Input Leakage Current	3.0	2.0	μA	V <sub>I</sub> = V <sub>CC</sub> GND

**Absolute Maximum Ratings** (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Input Diode Current ( $I_{IK}$ )	-20 mA
$V_I = -0.5V$	+20 mA
$V_I = V_{CC} + 0.5V$	
DC Input Voltage ( $V_I$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Diode Current ( $I_{OK}$ )	-20 mA
$V_O = -0.5V$	+20 mA
$V_O = V_{CC} + 0.5V$	
DC Output Voltage ( $V_O$ )	-0.5V to to $V_{CC} + 0.5V$
DC Output Source or Sink Current ( $I_O$ )	±50 mA
DC $V_{CC}$ or Ground Current ( $I_{CC}$ or $I_{GND}$ )	±200 mA
Storage Temperature ( $T_{STG}$ )	-65°C to +150°C
DC Latch-Up Source or Sink Current	±100 mA

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Recommended Operating Conditions**

Supply Voltage ( $V_{CC}$ )	2.0V to 3.6V
LVQ	
Input Voltage ( $V_I$ )	0V to $V_{CC}$
Output Voltage ( $V_O$ )	0V to $V_{CC}$
Operating Temperature ( $T_A$ )	-40°C to +85°C
74LVQ	
Minimum Input Edge Rate ( $\Delta V/\Delta t$ )	
$V_{IN}$ from 0.8V to 2.0V	
$V_{CC}$ @ 3.0V	125 mV/ns

**DC Characteristics**

Symbol	Parameter	V <sub>CC</sub> (V)	74LVQ74		74LVQ74		Units	Conditions
			T <sub>A</sub> = +25°C		T <sub>A</sub> = −40°C to +85°C			
			Typ	Guaranteed Limits				
V <sub>IH</sub>	Minimum High Level	3.0	1.5	2.0	2.0	V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> − 0.1V	
V <sub>IL</sub>	Maximum Low Level Input Voltage	3.0	1.5	0.8	0.8	V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> − 0.1V	
V <sub>OH</sub>	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I <sub>OUT</sub> = −50 μA	
		3.0		2.58	2.48	V	*V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OH</sub> = −12 mA	
V <sub>OL</sub>	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I <sub>OUT</sub> = 50 μA	
		3.0		0.36	0.44	V	*V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OL</sub> = 12 mA	
I <sub>IN</sub>	Maximum Input Leakage Current	3.6		±0.1	±1.0	μA	V <sub>I</sub> = V <sub>CC</sub> , GND	

\*All outputs loaded; thresholds on input associated with output under test.

## DC Characteristics (Continued)

Symbol	Parameter	V <sub>CC</sub> (V)	74LVQ74		74LVQ74		Units	Conditions
			T <sub>A</sub> = +25°C		T <sub>A</sub> = −40°C to +85°C			
			Typ	Guaranteed Limits				
I <sub>OLD</sub>	†Minimum Dynamic Output Current	3.6			36	mA	V <sub>OLD</sub> = 0.8V Max (Note 1)	
I <sub>OHD</sub>		3.6			−25	mA	V <sub>OHD</sub> = 2.0V Min (Note 1)	
I <sub>CC</sub>	Maximum Quiescent Supply Current	3.6		2.0	20.0	μA	V <sub>IN</sub> = V <sub>CC</sub> or GND	
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	3.3	0.2	0.8		V	(Notes 2 and 3)	
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	3.3	−0.2	−0.8		V	(Notes 2 and 3)	
V <sub>IHD</sub>	Maximum High Level Dynamic Input Voltage	3.3	1.7	2.0		V	(Notes 2 and 4)	
V <sub>ILD</sub>	Maximum Low Level Dynamic Input Voltage	3.3	1.6	0.8		V	(Notes 2 and 4)	

† Maximum test duration 2.0 ms, one output loaded at a time.

**Note 1:** Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed for 74LVQ.

**Note 2:** Worst case package.

**Note 3:** Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V; one output at GND.

**Note 4:** Max number of Data Inputs (n) switching. (n - 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V<sub>ILD</sub>, 0V to threshold (V<sub>IHD</sub>, f = 1 MHz.

## AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	74LVQ74			74LVQ74		Units
			T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF			T <sub>A</sub> = −40°C to +85°C C <sub>L</sub> = 50 pF		
			Min	Typ	Max	Min	Max	
f <sub>max</sub>	Maximum Clock Frequency	2.7 3.3 ± 0.3	50 100	100 125		40 95		MHz
t <sub>PLH</sub>	Propagation Delay C <sub>Dn</sub> or S <sub>Dn</sub> to Q <sub>n</sub>	2.7 3.3 ± 0.3	3.5 3.5	9.6 8.0	16.9 12.0	3.5 2.5	19.0 13.0	ns
t <sub>PHL</sub>	Propagation Delay C <sub>Dn</sub> or S <sub>Dn</sub> to Q <sub>n</sub>	2.7 3.3 ± 0.3	4.0 4.0	12.6 10.5	16.9 12.0	3.5 3.5	19.0 13.5	ns
t <sub>PLH</sub>	Propagation Delay CP <sub>n</sub> to Q <sub>n</sub> or Q <sub>n</sub>	2.7 3.3 ± 0.3	4.5 4.5	9.6 8.0	19.0 13.5	4.0 4.0	23.0 16.0	ns
t <sub>PHL</sub>	Propagation Delay CP <sub>n</sub> to Q <sub>n</sub> or Q <sub>n</sub>	2.7 3.3 ± 0.3	3.5 3.5	9.6 8.0	19.7 14.0	3.5 3.5	21.0 14.5	ns
t <sub>OSHL</sub> , t <sub>OSLH</sub>	Output to Output Skew* Data to Output	2.7 3.3 ± 0.3		1.0 1.0	1.5 1.5		1.5 1.5	ns

\*Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t<sub>OSHL</sub>) or LOW to HIGH (t<sub>OSLH</sub>). Parameter guaranteed by design.

# AC Operating Requirements: See Section 2 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	74LVQ74		74LVQ74		Units
			T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF		T <sub>A</sub> = −40°C to +85°C C <sub>L</sub> = 50 pF		
			Typ	Guaranteed Minimum			
t <sub>s</sub>	Set-up Time, HIGH or LOW	2.7 3.3 ± 0.3	1.8 1.5	5.0 4.0	6.5 4.5	ns	
t <sub>H</sub>	Hold Time, HIGH or LOW D <sub>n</sub> to CP <sub>n</sub>	2.7 3.3 ± 0.3	−2.4 −2.0	0.5 0.5	0.5 0.5	ns	
t <sub>W</sub>	Pulse Width	2.7 3.3 ± 0.3	3.6 3.0	7.0 5.5	10.0 7.0	ns	
t <sub>rec</sub>	Recovery Time	2.7 3.3 ± 0.3	3.0 −2.5	0 0	0 0	ns	

## Capacitance

Symbol	Parameter	Typ	Units	Conditions
C <sub>IN</sub>	Input Capacitance	4.5	pF	V <sub>CC</sub> = Open
C <sub>PD</sub> (Note 1)	Power Dissipation Capacitance	25	pF	V <sub>CC</sub> = 3.3V

Note 1: C<sub>PD</sub> is measured at 10 MHz.

## AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF		T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF		Units
			Min	Typ	Max	Min	
f <sub>max</sub>	Maximum Clock Frequency	2.7 3.3 ± 0.3	30 100	100	100	40 98	MHz
t <sub>PLH</sub>	Propagation Delay Q <sub>n</sub> to Q <sub>d</sub> or Q <sub>d</sub> to Q <sub>n</sub>	2.7 3.3 ± 0.3	3.5 3.5	9.5 8.0	18.5 12.0	3.5 2.5	ns
t <sub>PLH</sub>	Propagation Delay Q <sub>d</sub> to Q <sub>n</sub> or Q <sub>n</sub> to Q <sub>d</sub>	2.7 3.3 ± 0.3	4.0 4.0	12.5 10.5	18.5 12.0	3.5 2.5	ns
t <sub>PLH</sub>	Propagation Delay Q <sub>n</sub> to Q <sub>n</sub> or Q <sub>d</sub> to Q <sub>d</sub>	2.7 3.3 ± 0.3	4.5 4.5	9.5 9.0	19.0 12.5	4.0 4.0	ns
t <sub>PLH</sub>	Propagation Delay Q <sub>n</sub> to Q <sub>n</sub> or Q <sub>d</sub> to Q <sub>d</sub>	2.7 3.3 ± 0.3	3.5 3.5	9.5 8.0	19.5 14.0	3.5 2.5	ns
t <sub>OSK</sub>	Output to Output Skew Data to Output	2.7 3.3 ± 0.3	1.0 1.0	1.0 1.0	1.5 1.5	1.5 1.5	ns

\*Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction (either HIGH to LOW (Q<sub>out</sub>) or LOW to HIGH (Q<sub>in</sub>)). Parameters guaranteed by design.

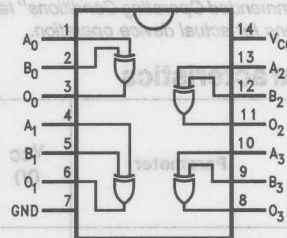
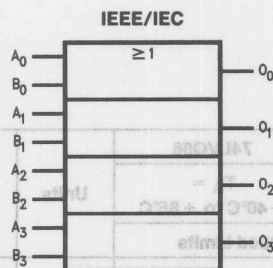
## Low Voltage Quad 2-Input Exclusive-OR Gate

The LVQ86 contains four, 2-input exclusive-OR gates.

- Ideal for low power/low noise 3.3V applications
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Guaranteed incident wave switching into 75Ω
- MIL-STD-883 54AC Products are available for Military/Aerospace applications

## Logic Symbol

### Pin Assignment for SOIC JEDEC and EIAJ



Pin 1		Pin 2		Pin 3	
Pin 4		Pin 5		Pin 6	
Pin 7		Pin 8		Pin 9	
Pin 10		Pin 11		Pin 12	
Pin 13		Pin 14		Pin 15	
Pin 16		Pin 17		Pin 18	
Pin 19		Pin 20		Pin 21	
Pin 22		Pin 23		Pin 24	
Pin 25		Pin 26		Pin 27	
Pin 28		Pin 29		Pin 30	
Pin 31		Pin 32		Pin 33	
Pin 34		Pin 35		Pin 36	
Pin 37		Pin 38		Pin 39	
Pin 40		Pin 41		Pin 42	
Pin 43		Pin 44		Pin 45	
Pin 46		Pin 47		Pin 48	
Pin 49		Pin 50		Pin 51	
Pin 52		Pin 53		Pin 54	
Pin 55		Pin 56		Pin 57	
Pin 58		Pin 59		Pin 60	
Pin 61		Pin 62		Pin 63	
Pin 64		Pin 65		Pin 66	
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Pin 859					

	SOIC JEDEC	SOIC EIAJ
Order Number	74LVQ86SC 74LVQ86SCX	74LVQ86SJ 74LVQ86SJX
See NS Package Number	M14A	M14D

Supply voltage ( $V_{CC}$ )  $-0.5V$  to  $+7.0V$

DC Input Diode Current ( $I_{IK}$ )  
 $V_I = -0.5V$   $-20\text{ mA}$   
 $V_I = V_{CC} + 0.5V$   $+20\text{ mA}$

DC Input Voltage ( $V_I$ )  $-0.5V$  to  $V_{CC} + 0.5V$

DC Output Diode Current ( $I_{OK}$ )  
 $V_O = -0.5V$   $-20\text{ mA}$   
 $V_O = V_{CC} + 0.5V$   $+20\text{ mA}$

DC Output Voltage ( $V_O$ )  $-0.5V$  to  $V_{CC} + 0.5V$

DC Output Source or Sink Current ( $I_O$ )  $\pm 50\text{ mA}$

DC  $V_{CC}$  or Ground Current ( $I_{CC}$  or  $I_{GND}$ )  $\pm 200\text{ mA}$

Storage Temperature ( $T_{STG}$ )  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$

DC Latch-Up Source or Sink Current  $\pm 100\text{ mA}$

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## DC Characteristics

Symbol	Parameter	V <sub>CC</sub> (V)	74LVQ86		74LVQ86		Units	Conditions
			T <sub>A</sub> = 25°C		T <sub>A</sub> = −40°C to +85°C			
			Typ	Guaranteed Limits				
V <sub>IH</sub>	Minimum High Level Input Voltage	3.0	1.5	2.0	2.0	V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> − 0.1V	
V <sub>IL</sub>	Maximum Low Level Input Voltage	3.0	1.5	0.8	0.8	V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> − 0.1V	
V <sub>OH</sub>	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I <sub>OUT</sub> = −50 μA	
		3.0		2.58	2.48	V	*V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OH</sub> = −12 mA	
V <sub>OL</sub>	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I <sub>OUT</sub> = 50 μA	
		3.0		0.36	0.44		*V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OL</sub> = 12 mA	
I <sub>IN</sub>	Maximum Input Leakage Current	3.6		±0.1	±1.0	μA	V <sub>I</sub> = V <sub>CC</sub> , GND	

\*All outputs loaded; thresholds on input associated with output under test.

Order Number	74LVQ86C	74LVQ86C
See NS Package Number	74LVQ86CX	74LVQ86CX
	M14D	M14D

**DC Characteristics** (Continued)

Symbol	Parameter	V <sub>CC</sub> (V)	74LVQ86		74LVQ86		Units	Conditions
			T <sub>A</sub> = 25°C		T <sub>A</sub> = − 40°C to + 85°C			
			Typ	Guaranteed Limits				
I <sub>OLD</sub>	†Minimum Dynamic Output Current	3.6			36	mA	V <sub>OLD</sub> = 0.8V Max (Note 1)	
I <sub>OHD</sub>		3.6			− 25	mA	V <sub>OHD</sub> = 2.0V Min (Note 1)	
I <sub>CC</sub>	Maximum Quiescent Supply Current	3.6		2.0	20.0	μA	V <sub>IN</sub> = V <sub>CC</sub> or GND	
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	3.3	0.5	0.8		V	(Notes 2, 3)	
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	3.3	− 0.5	− 0.8		V	(Notes 2, 3)	
V <sub>IHD</sub>	Maximum High Level Dynamic Input Voltage	3.3	1.8	2.0		V	(Notes 2, 4)	
V <sub>ILD</sub>	Maximum Low Level Dynamic Input Voltage	3.3	1.8	0.8		V	(Notes 2, 4)	

†Maximum test duration 20 ms, one output loaded at a time.

**Note 1:** Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed for 74LVQ.

**Note 2:** Worst case package.

**Note 3:** Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V; one output at GND.

**Note 4:** Max number of Data Inputs (n) switching. (n − 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V<sub>ILD</sub>), 0V to threshold (V<sub>IHD</sub>), f = 1 MHz.

**AC Electrical Characteristics:** See Section 2 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	74LVQ86			74LVQ86		Units
			T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF			T <sub>A</sub> = −40°C to +85°C C <sub>L</sub> = 50 pF		
			Min	Typ	Max	Min	Max	
t <sub>PLH</sub>	Propagation Delay	2.7	2.0	7.2	16.2	1.5	18.0	ns
		3.3 ± 0.3	2.0	6.0	11.5	1.5	12.5	
t <sub>PHL</sub>	Propagation Delay	2.7	2.0	7.8	16.2	1.5	18.0	ns
		3.3 ± 0.3	2.0	6.5	11.5	1.5	12.5	
t <sub>OSSL</sub> , t <sub>OSLH</sub>	Output to Output Skew*	2.7		1.0	1.5		1.5	ns
		3.3 ± 0.3		1.0	1.5		1.5	

\*Skews defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t<sub>OSSL</sub>) or LOW to HIGH (t<sub>OSLH</sub>). Parameter guaranteed by design.

**Capacitance**

Symbol	Parameter	Typ	Units	Conditions
C <sub>IN</sub>	Input Capacitance	4.5	pF	V <sub>CC</sub> = Open
C <sub>PD</sub> (Note 1)	Power Dissipation Capacitance	23	pF	V <sub>CC</sub> = 3.3V

**Note 1:** C<sub>PD</sub> is measured at 10 MHz.



## 74LVQ125

### Low Voltage Quad Buffer with TRI-STATE® Outputs

#### General Description

The LVQ125 contains four independent non-inverting buffers with TRI-STATE outputs.

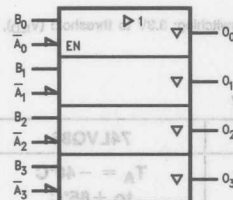
#### Features

- Ideal for low power/low noise 3.3V applications
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Guaranteed incident wave switching into 75Ω
- MIL-STD-883 54AC products are available for Military/Aerospace applications

**Ordering Code:** See Section 11

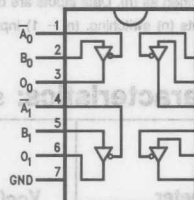
#### Logic Symbol

##### IEEE/IEC



TL/F/11349-1

##### Pin Assignment for SOIC JEDEC and EIAJ



TL/F/11349-2

Pin Names	Description
$\bar{A}_n, B_n$	Inputs
$\bar{O}_n$	Outputs

#### Truth Table

Inputs		Output
$\bar{A}_n$	$B_n$	$\bar{O}_n$
L	L	L
L	H	H
H	X	Z

H = HIGH Voltage Level  
L = LOW Voltage Level  
Z = HIGH Impedance  
X = Immaterial

	SOIC JEDEC	SOIC EIAJ
Order Number	74LVQ125SC 74LVQ125SCX	74LVQ125SJ 74LVQ125SJX
See NS Package Number	M14A	M14D

please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Input Diode Current ( $I_{IK}$ )	-20 mA
$V_I = -0.5V$ $V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage ( $V_I$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Diode Current ( $I_{OK}$ )	-20 mA
$V_O = -0.5V$ $V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage ( $V_O$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Source or Sink Current ( $I_O$ )	$\pm 50$ mA
DC $V_{CC}$ or Ground Current ( $I_{CC}$ or $I_{GND}$ )	$\pm 200$ mA
Storage Temperature ( $T_{STG}$ )	-65°C to +150°C
DC Latch-Up Source or Sink Current	$\pm 100$ mA

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Supply Voltage ( $V_{CC}$ )	2.0V to 3.6V
LVQ	
Input Voltage ( $V_I$ )	0V to $V_{CC}$
Output Voltage ( $V_O$ )	0V to $V_{CC}$
Operating Temperature ( $T_A$ )	-40°C to +85°C
74LVQ	
Minimum Input Edge Rate ( $\Delta V/\Delta t$ )	
$V_{IN}$ from 0.8V to 2.0V	
$V_{CC}$ @ 3.0V	125 mV/ns

## DC Characteristics

Symbol	Parameter	V <sub>CC</sub> (V)	74LVQ125		74LVQ125	Units	Conditions
			T <sub>A</sub> = +25°C		T <sub>A</sub> = −40°C to +85°C		
			Typ	Guaranteed Limits			
V <sub>IH</sub>	Minimum High Level Input Voltage	3.0	1.5	2.0	2.0	V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> − 0.1V
V <sub>IL</sub>	Maximum Low Level Input Voltage	3.0	1.5	0.8	0.8	V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> − 0.1V
V <sub>OH</sub>	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I <sub>OUT</sub> = −50 μA
		3.0		2.58	2.48	V	*V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OH</sub> = −12 mA
V <sub>OL</sub>	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I <sub>OUT</sub> = 50 μA
		3.0		0.36	0.44	V	*V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OL</sub> = 12 mA
I <sub>IN</sub>	Maximum Input Leakage Current	3.6		±0.1	±1.0	μA	V <sub>I</sub> = V <sub>CC</sub> , GND
I <sub>OZ</sub>	Maximum TRI-STATE Leakage Current	3.6		±0.25	±2.5	μA	V <sub>I</sub> (OE) = V <sub>IL</sub> , V <sub>IH</sub> V <sub>I</sub> = V <sub>CC</sub> , GND V <sub>O</sub> = V <sub>CC</sub> , GND

\*All outputs loaded; thresholds on input associated with output under test.

## DC Characteristics (Continued)

Symbol	Parameter	V <sub>CC</sub> (V)	74LVQ125		74LVQ125		Units	Conditions
			T <sub>A</sub> = +25°C		T <sub>A</sub> = −40°C to +85°C			
			Typ	Guaranteed Limits				
I <sub>OLD</sub>	†Minimum Dynamic Output Current	3.6			36		mA	V <sub>OLD</sub> = 0.8V Min (Note 1)
I <sub>OHD</sub>		3.6			−25		mA	V <sub>OHD</sub> = 2.0V Min (Note 1)
I <sub>CC</sub>	Maximum Quiescent Supply Current	3.6	4.0		40.0		μA	V <sub>IN</sub> = V <sub>CC</sub> or GND
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	3.3	0.6	1.0			V	(Notes 2 and 3)
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	3.3	−0.6	−1.0			V	(Notes 2 and 3)
V <sub>IHD</sub>	Maximum High Level Dynamic Input Voltage	3.3	1.7	2.0			V	(Notes 2 and 4)
V <sub>ILD</sub>	Maximum Low Level Dynamic Input Voltage	3.3	1.5	0.8			V	(Notes 2 and 4)

†Maximum test duration 2.0 ms, one output loaded at a time.

**Note 1:** Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed for 74LVQ.

**Note 2:** Worst case package.

**Note 3:** Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V; one output at GND.

**Note 4:** Max number of Data Inputs (n) switching. (n - 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V<sub>ILD</sub>), 0V to threshold (V<sub>IHD</sub>), f = 1 MHz.

## AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	74LVQ125			74LVQ125		Units
			T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF			T <sub>A</sub> = −40°C to +85°C C <sub>L</sub> = 50 pF		
			Min	Typ	Max	Min	Max	
t <sub>PLH</sub>	Propagation Delay Data to Output	2.7 3.3 ± 0.3	1.0 1.0	7.8 6.5	12.7 9.0	1.0 1.0	14.0 10.0	ns
t <sub>PHL</sub>	Propagation Delay Data to Output	2.7 3.3 ± 0.3	1.0 1.0	7.8 6.5	12.7 9.0	1.0 1.0	14.0 10.0	ns
t <sub>PZH</sub>	Output Enable Time	2.7 3.3 ± 0.3	1.0 1.0	7.2 6.0	14.8 10.5	1.0 1.0	16.0 11.0	ns
t <sub>PZL</sub>	Output Enable Time	2.7 3.3 ± 0.3	1.0 1.0	9.0 7.5	14.0 10.0	1.0 1.0	16.0 11.0	ns
t <sub>PHZ</sub>	Output Disable Time	2.7 3.3 ± 0.3	1.0 1.0	9.0 7.5	14.0 10.0	1.0 1.0	15.0 10.5	ns
t <sub>PLZ</sub>	Output Disable Time	2.7 3.3 ± 0.3	1.0 1.0	9.0 7.5	14.8 10.5	1.0 1.0	16.5 11.5	ns
t <sub>OSHL</sub> , t <sub>OSLH</sub>	Output to Output Skew* Data to Output	2.7 3.3 ± 0.3		1.0 1.0	1.5 1.5		1.5 1.5	ns

\*Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t<sub>OSHL</sub>) or LOW to HIGH (t<sub>OSLH</sub>). Parameter guaranteed by design.

## Capacitance

Symbol	Parameter	Typ	Units	Conditions
$C_{IN}$	Input Capacitance	4.5	pF	$V_{CC} = \text{Open}$
$C_{PD}$ (Note 1)	Power Dissipation Capacitance	34	pF	$V_{CC} = 3.3V$

Note 1:  $C_{PD}$  is measured at 10 MHz.

## Features

- Ideal for low power/low noise 3.3V applications
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Improved latch-up immunity
- Guaranteed incident wave switching into TSL
- 4 kV minimum ESD immunity
- Demultiplexing capability
- Multiple input enable for each expansion
- Active LOW mutually exclusive outputs
- MIL-STD-883 5-A/C products are available for Military Aerospace applications

## General Description

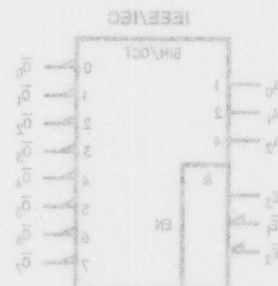
The LVQ138 is a high-speed 1-of-8 decoder/demultiplexer. This device is ideally suited for high-speed bipolar memory chip select address decoding. The multiple input enables allow parallel expansion to a 1-of-24 decoder using just three LVQ138 devices or a 1-of-32 decoder using four LVQ138 devices and one inverter.

Ordering Code: See Section 11

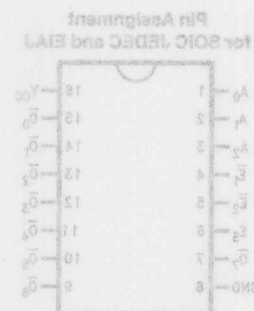
## Logic Symbols



LVQ138-1



LVQ138-4



LVQ138-2

Pin Names	Description
$A_0-A_7$	Address inputs
$E_0-E_3$	Enable inputs
$E_0$	Enable input
$Y_0-Y_7$	Outputs

Order Number	SOIC JEDEC	SOIC EIA1
74LVQ138C	74LVQ138C	74LVQ138C
74LVQ138CX	74LVQ138CX	74LVQ138CX
See NS Package Number	M16A	M16D



## 74LVQ138

### Low Voltage 1-of-8 Decoder/Demultiplexer

#### General Description

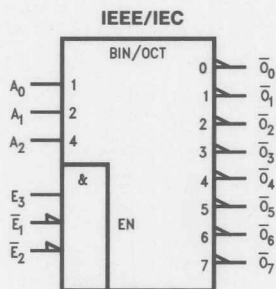
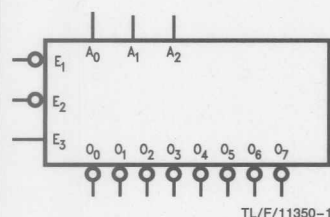
The LVQ138 is a high-speed 1-of-8 decoder/demultiplexer. This device is ideally suited for high-speed bipolar memory chip select address decoding. The multiple input enables allow parallel expansion to a 1-of-24 decoder using just three LVQ138 devices or a 1-of-32 decoder using four LVQ138 devices and one inverter.

#### Features

- Ideal for low power/low noise 3.3V applications
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Improved latch-up immunity
- Guaranteed incident wave switching into 75Ω
- 4 kV minimum ESD immunity
- Demultiplexing capability
- Multiple input enable for each expansion
- Active LOW mutually exclusive outputs
- MIL-STD-883 54AC products are available for Military/Aerospace applications

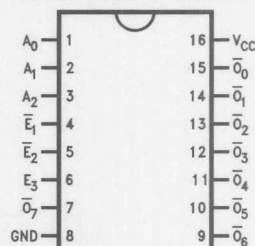
**Ordering Code:** See Section 11

#### Logic Symbols



#### Connection Diagram

Pin Assignment  
for SOIC JEDEC and EIAJ



Pin Names	Description
A <sub>0</sub> -A <sub>2</sub>	Address Inputs
E <sub>1</sub> -E <sub>2</sub>	Enable Inputs
E <sub>3</sub>	Enable Input
O <sub>0</sub> -O <sub>7</sub>	Outputs

	SOIC JEDEC	SOIC EIAJ
Order Number	74LVQ138SC 74LVQ138SCX	74LVQ138SJ 74LVQ138SJX
See NS Package Number	M16A	M16D

## Functional Description

The LVQ138 high-speed 1-of-8 decoder/demultiplexer accepts three binary weighted inputs ( $A_0$ ,  $A_1$ ,  $A_2$ ) and, when enabled, provides eight mutually exclusive active-LOW outputs ( $\bar{O}_0$ – $\bar{O}_7$ ). The LVQ138 features three Enable inputs, two active-LOW ( $\bar{E}_1$ ,  $\bar{E}_2$ ) and one active-HIGH ( $E_3$ ). All outputs will be HIGH unless  $\bar{E}_1$  and  $\bar{E}_2$  are LOW and  $E_3$  is HIGH. This multiple enable function allows easy parallel ex-

pansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four LVQ138 devices and one inverter (see Figure 7). The LVQ138 can be used as an 8-output demultiplexer by using one of the active LOW Enable inputs as the data input and the other Enable inputs as strobes. The Enable inputs which are not used must be permanently tied to their appropriate active-HIGH or active-LOW state.

## Truth Table

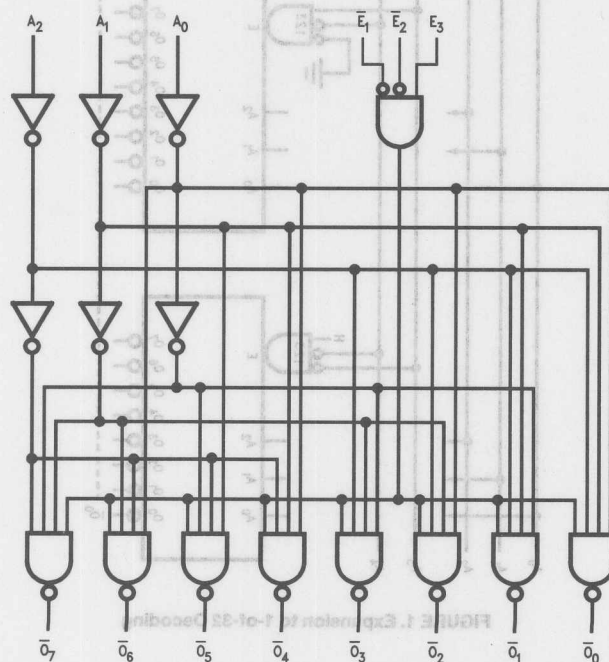
Inputs						Outputs							
$\bar{E}_1$	$\bar{E}_2$	$E_3$	$A_0$	$A_1$	$A_2$	$\bar{O}_0$	$\bar{O}_1$	$\bar{O}_2$	$\bar{O}_3$	$\bar{O}_4$	$\bar{O}_5$	$\bar{O}_6$	$\bar{O}_7$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH Voltage Level

L = LOW Voltage Level

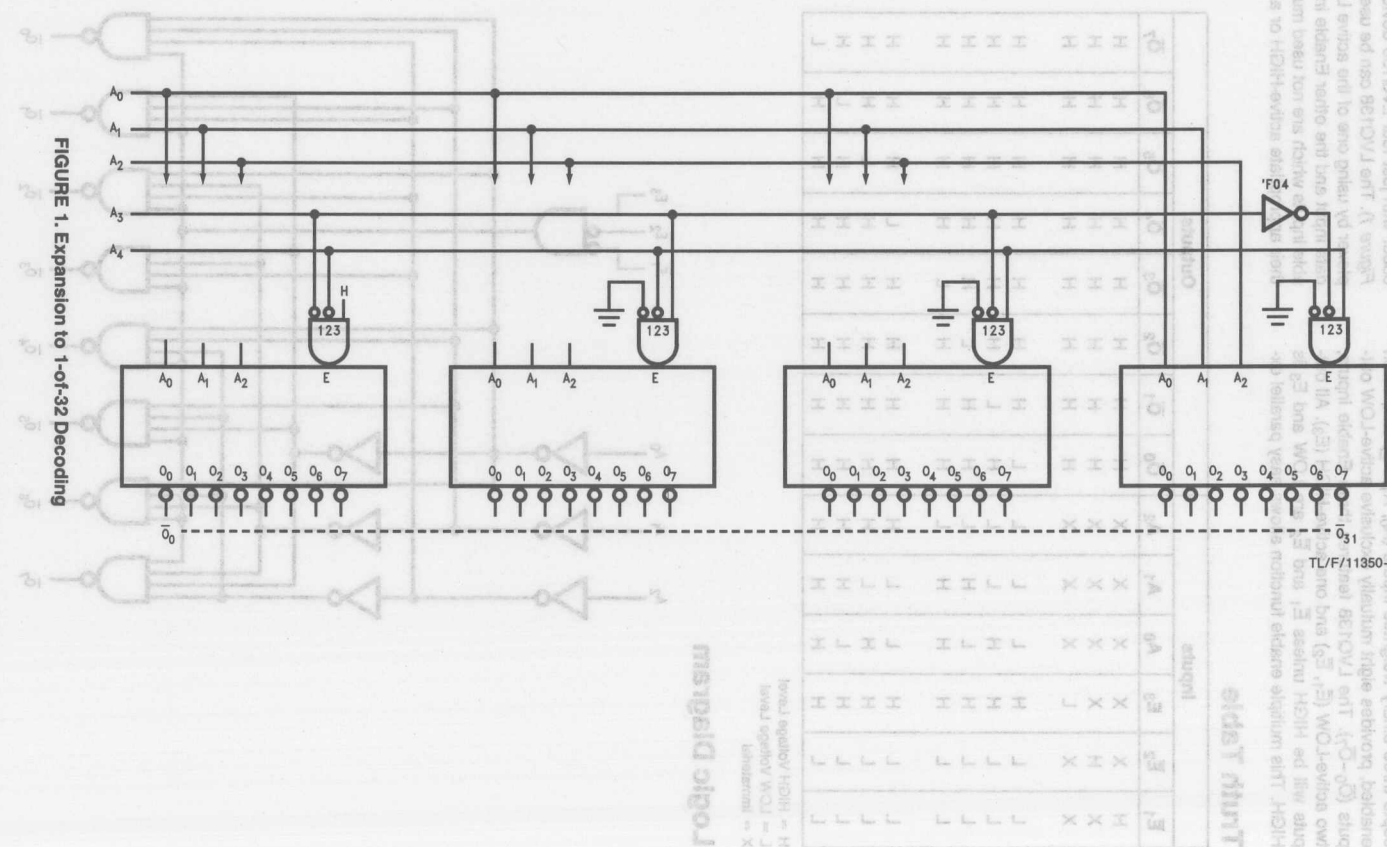
X = Immaterial

## Logic Diagram



TL/F/11350-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.



3-00001-00001

Any other information or data not shown here and is not subject to the same conditions as the information shown here.

**Office/Distributors for availability and specifications.**

 Supply Voltage ( $V_{CC}$ )

-0.5V to +7.0V

 DC Input Diode Current ( $I_{IK}$ )

 $V_I = -0.5V$ 

-20 mA

 $V_I = V_{CC} + 0.5V$ 

+20 mA

 DC Input Voltage ( $V_I$ )

 -0.5V to  $V_{CC} + 0.5V$ 

 DC Output Diode Current ( $I_{OK}$ )

 $V_O = -0.5V$ 

-20 mA

 $V_O = V_{CC} + 0.5V$ 

+20 mA

 DC Output Voltage ( $V_O$ )

 -0.5V to  $V_{CC} + 0.5V$ 

DC Output Source

 or Sink Current ( $I_O$ )

 $\pm 50$  mA

 DC  $V_{CC}$  or Ground Current

 ( $I_{CC}$  or  $I_{GND}$ )

 $\pm 200$  mA

 Storage Temperature ( $T_{STG}$ )

-65°C to +150°C

DC Latch-Up Source or

Sink Current

 $\pm 300$  mA

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**DC Characteristics**

Symbol	Parameter	V <sub>CC</sub> (V)	74LVQ138		74LVQ138		Units	Conditions
			T <sub>A</sub> = +25°C		T <sub>A</sub> = −40°C to +85°C			
			Typ	Guaranteed Limits				
V <sub>IH</sub>	Minimum High Level Input Voltage	3.0	1.5	2.0	2.0	V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> − 0.1V	
V <sub>IL</sub>	Maximum Low Level Input Voltage	3.0	1.5	0.8	0.8	V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> − 0.1V	
V <sub>OH</sub>	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I <sub>OUT</sub> = −50 μA	
		3.0	2.58	2.48	2.48	V	*V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OH</sub> = −12 mA	
V <sub>OL</sub>	Maximum Low Level Outut Voltage	3.0	0.002	0.1	0.1	V	I <sub>OUT</sub> = 50 μA	
		3.0	0.36	0.44	0.44	V	*V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OL</sub> = 12 mA	
I <sub>IN</sub>	Maximum Input Leakage Current	3.6	±0.1		±1.0	μA	V <sub>I</sub> = V <sub>CC</sub> , GND	
I <sub>OLD</sub>	†Minimum Dynamic Output Current	3.6	36		36	mA	V <sub>OLD</sub> = 0.8V Max (Note 1)	
I <sub>OHD</sub>		3.6	−25		−25	mA	V <sub>OHD</sub> = 2.0V Min (Note 1)	

\*All outputs loaded; thresholds on input associated with output under test.

Symbol	Parameter	Typ
$C_{IN}$	Input Capacitance	4.5 pF
$C_{PD}$	Power Dissipation Capacitance (Note 1)	45 pF

Note 1:  $C_{PD}$  is measured at 10 MHz.

## DC Characteristics (Continued)

Symbol	Parameter	V <sub>CC</sub> (V)	74LVQ138		74LVQ138		Units	Conditions
			T <sub>A</sub> = +25°C		T <sub>A</sub> = -40°C to +85°C			
			Typ	Guaranteed Limits				
I <sub>CC</sub>	Maximum Quiescent Supply Current	3.6		4.0		40.0	μA	V <sub>IN</sub> = V <sub>CC</sub> or GND
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	3.3		0.8			V	(Notes 2 & 3)
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	3.3		-0.8			V	(Notes 2 & 3)
V <sub>IHD</sub>	Maximum High Level Dynamic Input Voltage	3.3	1.7	2.0			V	(Notes 2 & 4)
V <sub>ILD</sub>	Maximum Low Level Dynamic Input Voltage	3.3	1.7	0.8			V	(Notes 2 & 4)

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed for 74LVQ.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V; one output at GND.

Note 4: Max number of Data Inputs (n) switching. (n - 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V<sub>ILD</sub>), 0V to threshold (V<sub>IHD</sub>), f = 1 MHz.

## AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	74LVQ138			74LVQ138		Units
			T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF			T <sub>A</sub> = −40°C to +85°C C <sub>L</sub> = 50 pF		
			Min	Typ	Max	Min	Max	
t <sub>PLH</sub>	Propagation Delay A <sub>n</sub> to $\overline{O}_n$	2.7 3.3 ± 0.3	1.5 1.5	10.2 8.5	18.3 13.0	1.5 1.5	21.0 15.0	ns
t <sub>PHL</sub>	Propagation Delay A <sub>n</sub> to $\overline{O}_n$	2.7 3.3 ± 0.3	1.5 1.5	9.6 8.0	17.6 12.5	1.5 1.5	20.0 14.0	ns
t <sub>PLH</sub>	Propagation Delay $\overline{E}_1$ or $\overline{E}_2$ to $\overline{O}_n$	2.7 3.3 ± 0.3	1.5 1.5	13.2 11.0	21.0 15.0	1.5 1.5	23.0 16.0	ns
t <sub>PHL</sub>	Propagation Delay $\overline{E}_1$ or $\overline{E}_2$ to $\overline{O}_n$	2.7 3.3 ± 0.3	1.5 1.5	11.4 9.5	19.0 13.5	1.5 1.5	21.0 15.0	ns
t <sub>PLH</sub>	Propagation Delay E <sub>3</sub> to $\overline{O}_n$	2.7 3.3 ± 0.3	1.5 1.5	13.2 11.0	21.8 15.5	1.5 1.5	23.5 16.5	ns
t <sub>PHL</sub>	Propagation Delay E <sub>3</sub> to $\overline{O}_n$	2.7 3.3 ± 0.3	1.5 1.5	10.2 8.5	18.3 13.0	1.5 1.5	20.0 14.0	ns
t <sub>OSSL</sub> , t <sub>OSLH</sub>	Output to Output Skew* Data to Output	2.7 3.3 ± 0.3		1.0 1.0	1.5 1.5		1.5 1.5	ns

\*Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t<sub>OSSL</sub>) or LOW to HIGH (t<sub>OSLH</sub>). Parameter guaranteed by design.

## Capacitance

Symbol	Parameter	Typ	Units	Conditions
C <sub>IN</sub>	Input Capacitance	4.5	pF	V <sub>CC</sub> = Open
C <sub>PD</sub> (Note 1)	Power Dissipation Capacitance	45	pF	V <sub>CC</sub> = 3.3V

Note 1: C<sub>PD</sub> is measured at 10 MHz.



# 74LVQ151

## Low Voltage 8-Input Multiplexer

### General Description

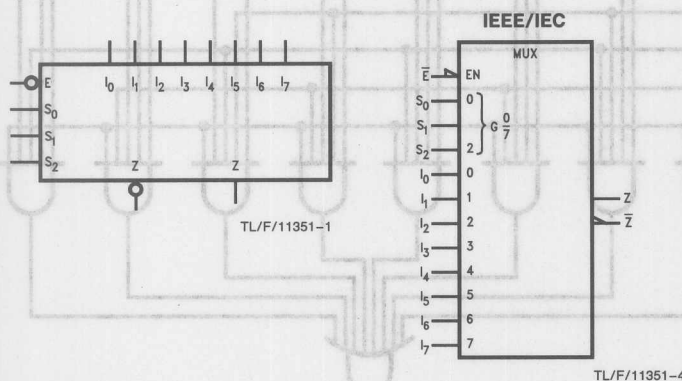
The LVQ151 is a high-speed 8-input digital multiplexer. It provides, in one package, the ability to select one line of data from up to eight sources. The LVQ151 can be used as a universal function generator to generate any logic function of four variables. Both true and complementary outputs are provided.

### Features

- Ideal for low power/low noise 3.3V applications
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Guaranteed incident wave switching into 75Ω
- MIL-STD-883 54AC products are available for Military/Aerospace applications

**Ordering Code:** See Section 11

### Logic Symbols



### Truth Table

Inputs				Outputs	
$\bar{E}$	$S_2$	$S_1$	$S_0$	$\bar{Z}$	$Z$
H	X	X	X	H	L
L	X	L	L	$\bar{I}_0$	$I_0$
L	L	L	H	$\bar{I}_1$	$I_1$
L	L	H	L	$\bar{I}_2$	$I_2$
L	L	H	H	$\bar{I}_3$	$I_3$
L	H	L	L	$\bar{I}_4$	$I_4$
L	H	L	H	$\bar{I}_5$	$I_5$
L	H	H	L	$\bar{I}_6$	$I_6$
L	H	H	H	$\bar{I}_7$	$I_7$

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial

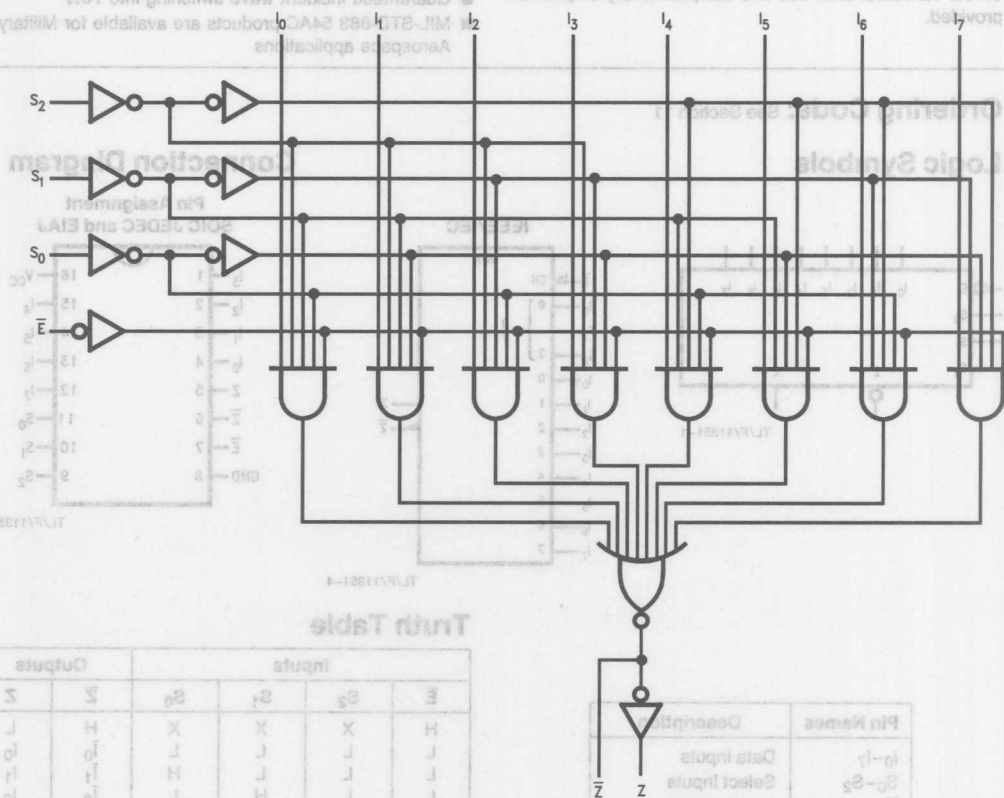
	SOIC JEDEC	SOIC EIAJ
Order Number	74LVQ151SC 74LVQ151SCX	74LVQ151SJ 74LVQ151SJX
See NS Package Number	M16A	M16D

## Functional Description

The LVQ151 is a logic implementation of a single pole, 8-position switch with the switch position controlled by the state of three Select inputs,  $S_0$ ,  $S_1$ ,  $S_2$ . Both true and complementary outputs are provided. The Enable input ( $\bar{E}$ ) is active LOW. When it is not activated, the complementary output is HIGH and the true output is LOW regardless of all other inputs. The logic function provided at the output is:

$$Z = \bar{E} \cdot (I_0 \cdot \bar{S}_0 \cdot \bar{S}_1 \cdot \bar{S}_2 + I_1 \cdot S_0 \cdot \bar{S}_1 \cdot \bar{S}_2 + I_2 \cdot \bar{S}_0 \cdot S_1 \cdot \bar{S}_2 + I_3 \cdot S_0 \cdot S_1 \cdot \bar{S}_2 + I_4 \cdot \bar{S}_0 \cdot \bar{S}_1 \cdot S_2 + I_5 \cdot S_0 \cdot \bar{S}_1 \cdot S_2 + I_6 \cdot \bar{S}_0 \cdot S_1 \cdot S_2 + I_7 \cdot S_0 \cdot S_1 \cdot S_2)$$

## Logic Diagram



Outputs		Inputs			
Z	$\bar{Z}$	$S_2$	$S_1$	$S_0$	$\bar{E}$
L	H	X	X	X	H
L	H	L	L	L	L
L	H	L	L	H	L
L	H	L	H	L	L
L	H	L	H	H	L
L	H	H	L	L	L
L	H	H	L	H	L
L	H	H	H	L	L
L	H	H	H	H	L
H	L	X	X	X	H
H	L	L	L	L	L
H	L	L	L	H	L
H	L	L	H	L	L
H	L	L	H	H	L
H	L	H	L	L	L
H	L	H	L	H	L
H	L	H	H	L	L
H	L	H	H	H	L

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Indifferent

Order Number		See NS Package Number	
74LVQ151SC	SOIC JEDEC	M15A	
74LVQ151SX	SOIC JEDEC	M15D	

The LVQ151 provides the ability, in one package to select from eight sources of data or control information. By proper manipulation of the inputs, the LVQ151 can provide any logic function of four variables and its complement.

The LVQ151 is a high-speed 8-input digital multiplexer. It provides, in one package, the ability to select one line of data from up to eight sources. The LVQ151 can be used as a universal function generator to generate any logic function of four variables. Both true and complementary outputs are provided.

TL/F/11351-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

**Absolute Maximum Ratings** (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Input Diode Current ( $I_{IK}$ )	
$V_I = -0.5V$	-20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage ( $V_I$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Diode Current ( $I_{OK}$ )	
$V_O = -0.5V$	-20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage ( $V_O$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Source or Sink Current ( $I_O$ )	$\pm 50$ mA
DC $V_{CC}$ or Ground Current ( $I_{CC}$ or $I_{GND}$ )	$\pm 200$ mA
Storage Temperature ( $T_{STG}$ )	-65°C to +150°C
DC Latch-Up Source or Sink Current	$\pm 100$ mA

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Recommended Operating Conditions**

Supply Voltage ( $V_{CC}$ )	2.0V to 3.6V
LVQ	
Input Voltage ( $V_I$ )	0V to $V_{CC}$
Output Voltage ( $V_O$ )	0V to $V_{CC}$
Operating Temperature ( $T_A$ )	-40°C to +85°C
74LVQ	
Minimum Input Edge Rate ( $\Delta V/\Delta t$ )	
$V_{IN}$ from 0.8V to 2.0V	
$V_{CC}$ @ 3.0V	125 mV/ns

**DC Characteristics**

Symbol	Parameter	V <sub>CC</sub> (V)	74LVQ151		74LVQ151		Units	Conditions
			T <sub>A</sub> = +25°C		T <sub>A</sub> = -40°C to +85°C			
			Typ	Guaranteed Limits				
V <sub>IH</sub>	Minimum High Level Input Voltage	3.0	1.5	2.0	2.0	V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V	
V <sub>IL</sub>	Maximum Low Level Input Voltage	3.0	1.5	0.8	0.8	V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V	
V <sub>OH</sub>	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I <sub>OUT</sub> = -50 μA	
		3.0		2.58	2.48	V	*V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OH</sub> = -12 mA	
V <sub>OL</sub>	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I <sub>OUT</sub> = 50 μA	
		3.0		0.36	0.44	V	*V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OL</sub> = 12 mA	
I <sub>IN</sub>	Maximum Input Leakage Current	3.6		±0.1	±1.0	μA	V <sub>I</sub> = V <sub>CC</sub> , GND	

\*All outputs loaded; thresholds on input associated with output under test.

\*All outputs loaded; thresholds on input associated with output under test.

## DC Characteristics (Continued)

Symbol	Parameter	V <sub>CC</sub> (V)	74LVQ151		74LVQ151		Units	Conditions
			T <sub>A</sub> = +25°C		T <sub>A</sub> = −40°C to +85°C			
			Typ	Guaranteed Limits				
I <sub>OLD</sub>	†Minimum Dynamic Output Current	3.6			36		mA	V <sub>OLD</sub> = 0.8V Max (Note 1)
I <sub>OHD</sub>		3.6			−25		mA	V <sub>OHD</sub> = 2.0V (Note 1)
I <sub>CC</sub>	Maximum Quiescent Supply Current	3.6		4.0		40.0	μA	V <sub>IN</sub> = V <sub>CC</sub> or GND
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	3.3		0.8			V	(Notes 2 & 3)
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	3.3		−0.8			V	(Notes 2 & 3)
V <sub>IHD</sub>	Maximum High Level Dynamic Input Voltage	3.3	1.7	2.0			V	(Notes 2 & 4)
V <sub>ILD</sub>	Maximum Low Level Dynamic Input Voltage	3.3	1.7	0.8			V	(Notes 2 & 4)

†Maximum test duration 2.0 ms, one output loaded at a time.

**Note 1:** Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed for 74LVQ.

**Note 2:** Worst case package.

**Note 3:** Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V; one output at GND.

**Note 4:** Max number of Data Inputs (n) switching. (n – 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V<sub>ILD</sub>), 0V to threshold (V<sub>IHD</sub>). f = 1 MHz.

## AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	74LVQ151			74LVQ151		Units
			T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF			T <sub>A</sub> = −40°C to +85°C C <sub>L</sub> = 50 pF		
			Min	Typ	Max	Min	Max	
t <sub>PLH</sub>	Propagation Delay S <sub>n</sub> to Z or $\bar{Z}$	2.7 3.3 ± 0.3	3.0 3.0	13.8 11.5	25.3 18.0	3.0 3.0	28.0 20.0	ns
t <sub>PHL</sub>	Propagation Delay S <sub>n</sub> to Z or $\bar{Z}$	2.7 3.3 ± 0.3	2.5 2.5	14.4 12.0	25.3 18.0	2.5 2.5	28.0 20.0	ns
t <sub>PLH</sub>	Propagation Delay E to Z or $\bar{Z}$	2.7 3.3 ± 0.3	2.5 2.5	9.6 8.0	18.3 13.0	2.0 2.0	20.0 14.0	ns
t <sub>PHL</sub>	Propagation Delay E to Z or $\bar{Z}$	2.7 3.3 ± 0.3	1.5 1.5	10.2 8.5	18.3 13.0	1.5 1.5	20.0 14.0	ns
t <sub>PLH</sub>	Propagation Delay I <sub>n</sub> to Z or $\bar{Z}$	2.7 3.3 ± 0.3	2.5 2.5	11.4 9.5	19.7 14.0	2.0 2.0	22.0 15.5	ns
t <sub>PHL</sub>	Propagation Delay I <sub>n</sub> to Z or $\bar{Z}$	2.7 3.3 ± 0.3	2.5 2.5	11.4 9.5	21.1 15.0	2.0 2.0	23.0 16.0	ns
t <sub>OSSL</sub> , t <sub>OSLH</sub>	Output to Output Skew* Data to Output	2.7 3.3 ± 0.3		1.0 1.0	1.5 1.5		1.5 1.5	ns

\*Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t<sub>OSSL</sub>) or LOW to HIGH (t<sub>OSLH</sub>). Parameter guaranteed by design.

## Capacitance

Symbol	Parameter	Typ	Units	Conditions
$C_{IN}$	Input Capacitance	4.5	pF	$V_{CC} = \text{Open}$
$C_{PD}$ (Note 1)	Power Dissipation Capacitance	45	pF	$V_{CC} = 3.3V$

Note 1:  $C_{PD}$  is measured at 10 MHz.

## Features

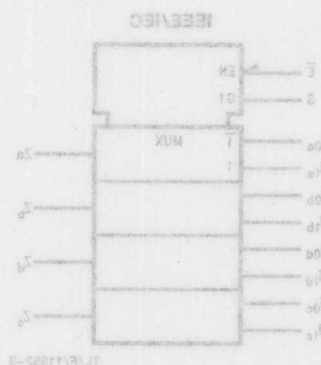
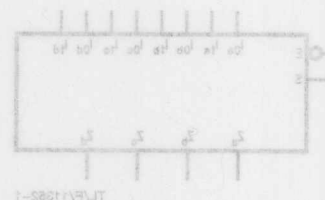
- Ideal for low power/low noise 3.3V applications
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Guaranteed incident wave switching into 75Ω
- MIL-STD-883 B4AC products are available for Military Aerospace applications

## General Description

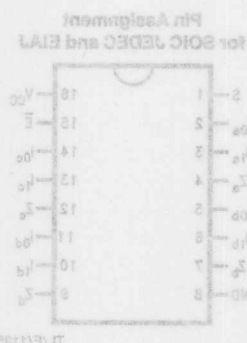
The LVQ151 is a high-speed quad 2-input multiplexer. Four bits of data from two sources can be selected using the common Select and Enable inputs. The four outputs present the selected data in the true (noninverted) form. The LVQ151 can also be used as a function generator.

Ordering Code: See Section 11

## Logic Symbols



## Connection Diagram



Pin Name	Description
1A-1B	Source 0 Data Inputs
2A-2B	Source 1 Data Inputs
3A-3B	Source 2 Data Inputs
4A-4B	Source 3 Data Inputs
1Y-4Y	Outputs
S	Select Input
E	Enable Input

Order Number	SOIC JEDEC	SOIC EIAL
74LVQ151	74LVQ151	74LVQ151
74LVQ151X	74LVQ151X	74LVQ151X
See NS Package Number	M16A	M16D

# 74LVQ157

## Low Voltage Quad 2-Input Multiplexer

### General Description

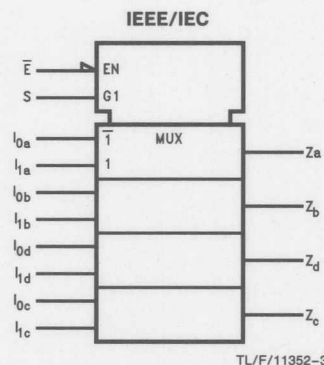
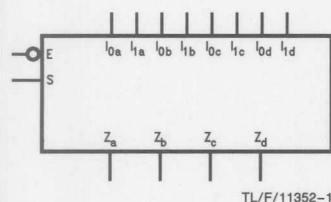
The LVQ157 is a high-speed quad 2-input multiplexer. Four bits of data from two sources can be selected using the common Select and Enable inputs. The four outputs present the selected data in the true (noninverted) form. The LVQ157 can also be used as a function generator.

### Features

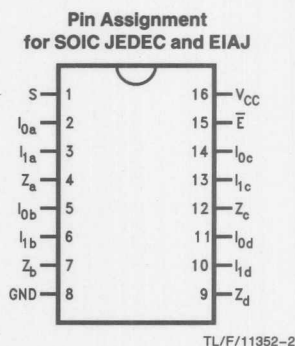
- Ideal for low power/low noise 3.3V applications
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Guaranteed incident wave switching into 75Ω.
- MIL-STD-883 54AC products are available for Military/Aerospace applications

### Ordering Code: See Section 11

### Logic Symbols



### Connection Diagram



Pin Names	Description
$I_{0a}$ – $I_{0d}$	Source 0 Data Inputs
$I_{1a}$ – $I_{1d}$	Source 1 Data Inputs
$\bar{E}$	Enable Input
$S$	Select Input
$Z_a$ – $Z_d$	Outputs

	SOIC JEDEC	SOIC EIAJ
Order Number	74LVQ157SC 74LVQ157SCX	74LVQ157SJ 74LVQ157SJX
See NS Package Number	M16A	M16D

of data from two sources under the control of a common Select input (S). The Enable input (E) is active-LOW. When  $\bar{E}$  is HIGH, all of the outputs (Z) are forced LOW regardless of all other inputs. The LVQ157 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

$$Z_a = \bar{E} \cdot (I_{1a} \cdot S + I_{0a} \cdot \bar{S})$$

$$Z_b = \bar{E} \cdot (I_{1b} \cdot S + I_{0b} \cdot \bar{S})$$

$$Z_c = \bar{E} \cdot (I_{1c} \cdot S + I_{0c} \cdot \bar{S})$$

$$Z_d = \bar{E} \cdot (I_{1d} \cdot S + I_{0d} \cdot \bar{S})$$

A common use of the LVQ157 is the moving of data from two groups of registers to four common output busses. The particular register from which the data comes is determined by the state of the Select input. A less obvious use is

of the sixteen different functions of two variables with one variable common. This is useful for implementing gating functions.

## Truth Table

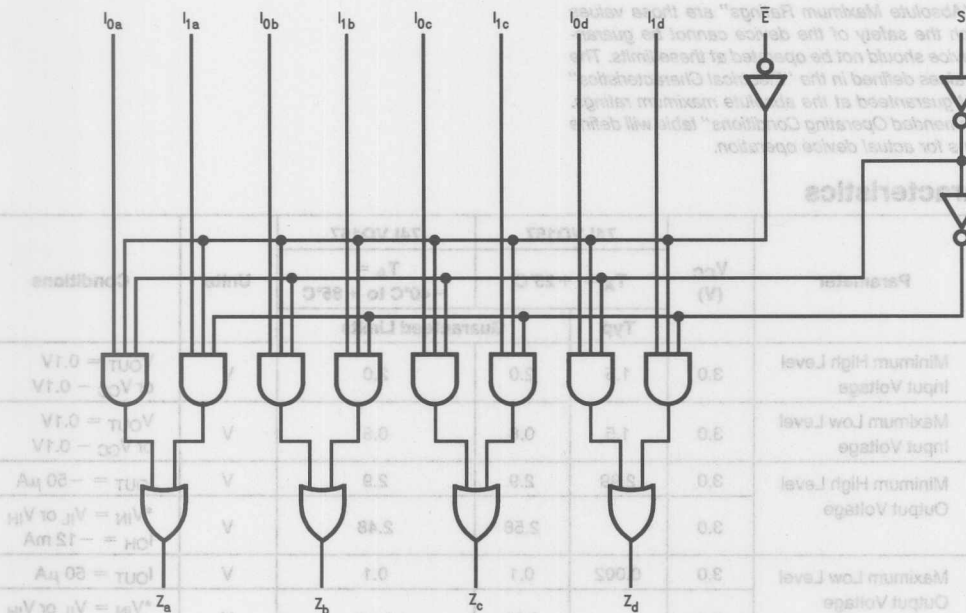
Inputs				Outputs
$\bar{E}$	S	$I_0$	$I_1$	Z
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

TL/F/11352-5

**Absolute Maximum Ratings** (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )  $-0.5V$  to  $+7.0V$

DC Input Diode Current ( $I_{IK}$ )

$V_I = -0.5V$   $-20\text{ mA}$

$V_I = V_{CC} + 0.5V$   $+20\text{ mA}$

DC Input Voltage ( $V_I$ )  $-0.5V$  to  $V_{CC} + 0.5V$

DC Output Diode Current ( $I_{OK}$ )

$V_O = -0.5V$   $-20\text{ mA}$

$V_O = V_{CC} + 0.5V$   $+20\text{ mA}$

DC Output Voltage ( $V_O$ )  $-0.5V$  to  $V_{CC} + 0.5V$

DC Output Source or Sink Current ( $I_O$ )  $\pm 50\text{ mA}$

DC  $V_{CC}$  or Ground Current ( $I_{CC}$  or  $I_{GND}$ )  $\pm 200\text{ mA}$

Storage Temperature ( $T_{STG}$ )  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$

DC Latch-Up Source or Sink Current  $\pm 100\text{ mA}$

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**DC Characteristics**

Symbol	Parameter	V <sub>CC</sub> (V)	74LVQ157		74LVQ157		Units	Conditions
			T <sub>A</sub> = +25°C		T <sub>A</sub> = −40°C to +85°C			
			Typ	Guaranteed Limits				
V <sub>IH</sub>	Minimum High Level Input Voltage	3.0	1.5	2.0	2.0	V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> − 0.1V	
V <sub>IL</sub>	Maximum Low Level Input Voltage	3.0	1.5	0.8	0.8	V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> − 0.1V	
V <sub>OH</sub>	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I <sub>OUT</sub> = −50 μA	
		3.0		2.58	2.48	V	*V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OH</sub> = −12 mA	
V <sub>OL</sub>	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I <sub>OUT</sub> = 50 μA	
		3.0		0.36	0.44	V	*V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OL</sub> = 12 mA	
I <sub>IN</sub>	Maximum Input Leakage Current	3.6		±0.1	±1.0	μA	V <sub>I</sub> = V <sub>CC</sub> , GND	

\*All outputs loaded; thresholds on input associated with output under test.

**Recommended Operating Conditions**

Supply Voltage ( $V_{CC}$ )

LVQ  $2.0V$  to  $3.6V$

Input Voltage ( $V_I$ )

$0V$  to  $V_{CC}$

Output Voltage ( $V_O$ )

$0V$  to  $V_{CC}$

Operating Temperature ( $T_A$ )

74LVQ  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$

Minimum Input Edge Rate ( $\Delta V/\Delta t$ )

$V_{IN}$  from  $0.8V$  to  $2.0V$

$V_{CC}$  @  $3.0V$

$125\text{ mV/ns}$

## DC Characteristics (Continued)

Symbol	Parameter	V <sub>CC</sub> (V)	74LVQ157		74LVQ157		Units	Conditions
			T <sub>A</sub> = +25°C		T <sub>A</sub> = −40°C to +85°C			
			Typ	Guaranteed Limits				
I <sub>OLD</sub>	†Minimum Dynamic Output Current	3.6			36	mA	V <sub>OLD</sub> = 0.8V Max (Note 1)	
I <sub>OHD</sub>		3.6			−25	mA	V <sub>OHD</sub> = 2.0V Min (Note 1)	
I <sub>CC</sub>	Maximum Quiescent Supply Current	3.6		4.0	40.0	μA	V <sub>IN</sub> = V <sub>CC</sub> or GND	
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	3.3	0.7	0.8		V	(Notes 2 & 3)	
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	3.3	−0.4	−0.8		V	(Notes 2 & 3)	
V <sub>IHD</sub>	Maximum High Level Dynamic Input Voltage	3.3	1.7	2.0		V	(Notes 2 & 4)	
V <sub>ILD</sub>	Maximum Low Level Dynamic Input Voltage	3.3	1.6	0.8		V	(Notes 2 & 4)	

†Maximum test duration 2.0 ms, one output loaded at a time.

**Note 1:** Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed for 74LVQ.

**Note 2:** Worst case package.

**Note 3:** Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V; one output at GND.

**Note 4:** Max number of Data Inputs (n) switching. (n - 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V<sub>ILD</sub>), 0V to threshold (V<sub>IHD</sub>), f = 1 MHz.

## AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	74LVQ157			74LVQ157		Units
			T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF			T <sub>A</sub> = −40°C to +85°C C <sub>L</sub> = 50 pF		
			Min	Typ	Max	Min	Max	
t <sub>PLH</sub>	Propagation Delay S to Z <sub>n</sub>	2.7 3.3 ± 0.3	1.5 1.5	84 7.0	16.2 11.5	1.5 1.5	19.0 13.0	ns
t <sub>PHL</sub>	Propagation Delay S to Z <sub>n</sub>	2.7 3.3 ± 0.3	1.5 1.5	7.8 6.5	15.5 11.0	1.5 1.5	17.0 12.0	ns
t <sub>PLH</sub>	Propagation Delay Ē to Z <sub>n</sub>	2.7 3.3 ± 0.3	1.5 1.5	8.4 7.0	16.2 11.5	1.5 1.5	19.0 13.0	ns
t <sub>PHL</sub>	Propagation Delay Ē to Z <sub>n</sub>	2.7 3.3 ± 0.3	1.5 1.5	7.8 6.5	15.5 11.0	1.5 1.5	17.0 12.0	ns
t <sub>PLH</sub>	Propagation Delay I <sub>n</sub> to Z <sub>n</sub>	2.7 3.3 ± 0.3	1.5 1.5	6.0 5.0	12.0 8.5	1.0 1.0	13.0 9.0	ns
t <sub>PHL</sub>	Propagation Delay I <sub>n</sub> to Z <sub>n</sub>	2.7 3.3 ± 0.3	1.5 1.5	6.0 5.0	11.3 8.0	1.0 1.0	13.0 9.0	ns
t <sub>OSHL</sub> , t <sub>OSLH</sub>	Output to Output Skew* Data to Output	2.7 3.3 ± 0.3		1.0 1.0	1.5 1.5		1.5 1.5	ns

\*Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t<sub>OSHL</sub>) or LOW to HIGH (t<sub>OSLH</sub>). Parameter guaranteed by design.

## Capacitance

DC Characteristics (Continued)

Symbol	Parameter	Typ	Units	Conditions
$C_{IN}$	Input Capacitance	4.5	pF	$V_{CC} = \text{Open}$
$C_{PD}$ (Note 1)	Power Dissipation Capacitance	34.0	pF	$V_{CC} = 3.3V$

Note 1:  $C_{PD}$  is measured at 10 MHz.

Maximum test duration 5.0 ms, one output loaded at a time.  
 Note 1: Incident wave switching on transition time with impedances as low as 75Ω for commercial temperature range is guaranteed for T1LVQ157.  
 Note 2: Worst case package.  
 Note 3: Max number of outputs defined as (n). Data inputs are given 0V to 3.3V; one output at GND.  
 Note 4: Max number of Data inputs (n) switching: (n-1) inputs switching 0V to 3.3V, input under test switching 3.3V to threshold ( $V_{IOP}$ ), 0V to threshold ( $V_{IOL}$ ), 1 = 1 MHz.

## AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF			T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF		Units
			Min	Typ	Max	T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF		
						Min	Max	
t <sub>PLH</sub>	Propagation Delay S to Z <sub>n</sub>	2.7 3.3 ± 0.3	1.5 1.5	8.4 7.0	16.5 11.5	1.5 1.5	ns	
t <sub>PHL</sub>	Propagation Delay S to Z <sub>n</sub>	2.7 3.3 ± 0.3	1.5 1.5	7.8 8.5	15.5 11.0	1.5 1.5	ns	
t <sub>PLH</sub>	Propagation Delay E to Z <sub>n</sub>	2.7 3.3 ± 0.3	1.5 1.5	8.4 7.0	16.5 11.5	1.5 1.5	ns	
t <sub>PHL</sub>	Propagation Delay E to Z <sub>n</sub>	2.7 3.3 ± 0.3	1.5 1.5	7.8 8.5	15.5 11.0	1.5 1.5	ns	
t <sub>PLH</sub>	Propagation Delay I <sub>n</sub> to Z <sub>n</sub>	2.7 3.3 ± 0.3	1.5 1.5	8.0 8.0	15.0 8.5	1.0 1.0	ns	
t <sub>PHL</sub>	Propagation Delay I <sub>n</sub> to Z <sub>n</sub>	2.7 3.3 ± 0.3	1.5 1.5	8.0 8.0	11.5 8.0	1.0 1.0	ns	
t <sub>OSL</sub>	Output to Output Skew*	2.7	1.0	1.0	1.5	1.5	ns	
t <sub>OCH</sub>	Data to Output	3.3 ± 0.3	1.0	1.0	1.5	1.5	ns	

\*Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW ( $t_{OCH}$ ) or LOW to HIGH ( $t_{OSL}$ ). Parameter guaranteed by design.



## 74LVQ174

# Low Voltage Hex D Flip-Flop with Master Reset

## General Description

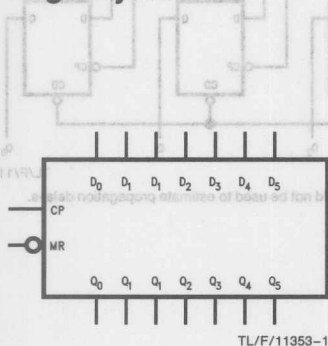
The LVQ174 is a high-speed hex D flip-flop. The device is used primarily as a 6-bit edge-triggered storage register. The information on the D inputs is transferred to storage during the LOW-to-HIGH clock transition. The device has a Master Reset to simultaneously clear all flip-flops.

## Features

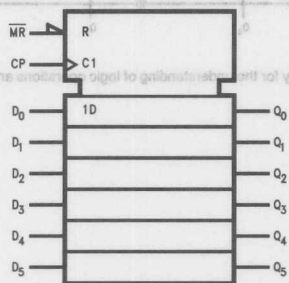
- Ideal for low power/low noise 3.3V applications
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Guaranteed incident wave switching into 75Ω
- MIL-STD-883 54AC products are available for Military/Aerospace applications

**Ordering Code:** See Section 11

## Logic Symbols

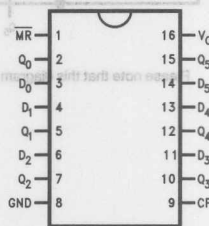


## IEEE/IEC



## Connection Diagram

### Pin Assignment for SOIC JEDEC and EIAJ



Pin Names	Description
D <sub>0</sub> -D <sub>5</sub>	Data Inputs
CP	Clock Pulse Input
MR	Master Reset Input
Q <sub>0</sub> -Q <sub>5</sub>	Outputs

	SOIC JEDEC	SOIC EIAJ
Order Number	74LVQ174SC 74LVQ174SCX	74LVQ174SJ 74LVQ174SJX
See NS Package Number	M16A	M16D

## Functional Description

The LVQ174 consists of six edge-triggered D flip-flops with individual D inputs and Q outputs. The Clock (CP) and Master Reset ( $\overline{MR}$ ) are common to all flip-flops. Each D input's state is transferred to the corresponding flip-flop's output following the LOW-to-HIGH Clock (CP) transition. A LOW input to the Master Reset ( $\overline{MR}$ ) will force all outputs LOW independent of Clock or Data inputs. The LVQ174 is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

## Truth Table

Inputs			Output
$\overline{MR}$	CP	D	Q
L	X	X	L
H	↗	H	H
H	↘	L	L
H	L	X	Q

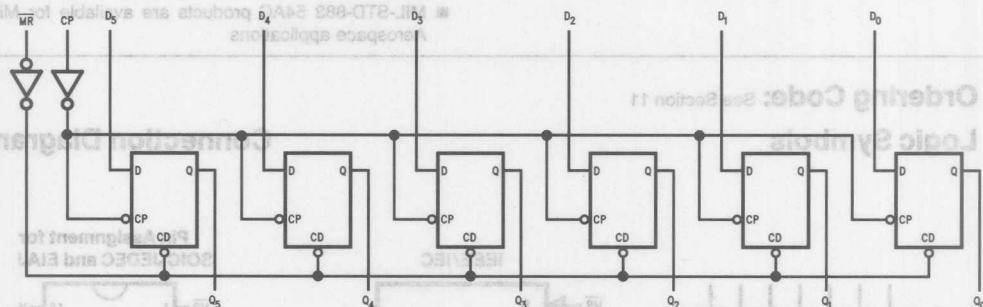
H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

↗ = LOW-to-HIGH Transition

## Logic Diagram



TL/F/11353-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Pin Number	Description
D <sub>0</sub> -D <sub>5</sub>	Data inputs
CP	Clock Pulse input
$\overline{MR}$	Master Reset input
Q <sub>0</sub> -Q <sub>5</sub>	Outputs

Order Number	See NS Package Number	M18A	M18D
LVQ174SC	LVQ174SX		
LVQ174SC	LVQ174SX		
LVQ174SC	LVQ174SX		

**Office/Distributors for availability and specifications.**

Supply Voltage ( $V_{CC}$ )  $-0.5V$  to  $+7.0V$

DC Input Diode Current ( $I_{IK}$ )

$V_I = -0.5V$

$V_I = V_{CC} + 0.5V$

DC Input Voltage ( $V_I$ )

$-0.5V$  to  $V_{CC} + 0.5V$

DC Output Diode Current ( $I_{OK}$ )

$V_O = -0.5V$

$V_O = V_{CC} + 0.5V$

DC Output Voltage ( $V_O$ )

$-0.5V$  to  $V_{CC} + 0.5V$

DC Output Source

or Sink Current ( $I_O$ )

$\pm 50$  mA

DC  $V_{CC}$  or Ground Current

( $I_{CC}$  or  $I_{GND}$ )

$\pm 200$  mA

Storage Temperature ( $T_{STG}$ )

$-65^\circ C$  to  $+150^\circ C$

DC Latch-Up Source or

Sink Current

$\pm 100$  mA

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Supply Voltage ( $V_{CC}$ )

LVQ

2.0V to 3.6V

Input Voltage ( $V_I$ )

0V to  $V_{CC}$

Output Voltage ( $V_O$ )

0V to  $V_{CC}$

Operating Temperature ( $T_A$ )

74LVQ

$-40^\circ C$  to  $+85^\circ C$

Minimum Input Edge Rate ( $\Delta V/\Delta t$ )

$V_{IN}$  from 0.8V to 2.0V

$V_{CC}$  @ 3.0V

125 mV/ns

## DC Characteristics

Symbol	Parameter	V <sub>CC</sub> (V)	74LVQ174		74LVQ174		Units	Conditions
			T <sub>A</sub> = +25°C		T <sub>A</sub> = −40°C to +85°C			
			Typ	Guaranteed Limits				
V <sub>IH</sub>	Minimum High Level Input Voltage	3.0	1.5	2.0	2.0	V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> − 0.1V	
V <sub>IL</sub>	Maximum Low Level Input Voltage	3.0	1.5	0.8	0.8	V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> − 0.1V	
V <sub>OH</sub>	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I <sub>OUT</sub> = −50 μA	
		3.0		2.58	2.48	V	*V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OH</sub> = −12 mA	
V <sub>OL</sub>	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I <sub>OUT</sub> = 50 μA	
		3.0		0.36	0.44	V	*V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OL</sub> = 12 mA	
I <sub>IN</sub>	Maximum Input Leakage Current	3.6	±0.1		±1.0		μA	V <sub>I</sub> = V <sub>CC</sub> , GND

\*All outputs loaded; thresholds on input associated with output under test.

Symbol	Parameter	(V)	$T_A = +25^\circ\text{C}$		Units	Conditions
			Typ	Guaranteed Limits		
$I_{OLD}$	† Minimum Dynamic Output Current	3.6		36	mA	$V_{OLD} = 0.8\text{V Max}$ (Note 1)
$I_{OHD}$		3.6		-25	mA	$V_{OHD} = 2.0\text{V Min}$ (Note 1)
$I_{CC}$	Maximum Quiescent Supply Current	3.6	4.0	40.0	$\mu\text{A}$	$V_{IN} = V_{CC}$ or GND
$V_{OLP}$	Quiet Output Maximum Dynamic $V_{OL}$	3.3	0.7	0.8	V	(Notes 2, 3)
$V_{OLV}$	Quiet Output Minimum Dynamic $V_{OL}$	3.3	-0.6	-0.8	V	(Notes 2, 3)
$V_{IHD}$	Maximum High Level Dynamic Input Voltage	3.3	1.8	2.0	V	(Notes 2, 4)
$V_{ILD}$	Maximum Low Level Dynamic Input Voltage	3.3	1.6	0.8	V	(Notes 2, 4)

† Maximum test duration 2.0 ms, one output loaded at a time.

**Note 1:** Incident wave switching on transmission lines with impedances as low as 75 $\Omega$  for commercial temperature range is guaranteed for 74LVQ.

**Note 2:** Worst case package.

**Note 3:** Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V; one output at GND.

**Note 4:** Max number of Data Inputs (n) switching. (n - 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold ( $V_{ILD}$ ), 0V to threshold ( $V_{IHD}$ ),  $f = 1\text{ MHz}$ .

## AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	74LVQ174			74LVQ174		Units
			T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF			T <sub>A</sub> = −40°C to +85°C C <sub>L</sub> = 50 pF		
			Min	Typ	Max	Min	Max	
f <sub>max</sub>	Maximum Clock Frequency	2.7 3.3 ± 0.3	60 90	90 100		50 70		MHz
t <sub>PLH</sub>	Propagation Delay CP to Q <sub>n</sub>	2.7 3.3 ± 0.3	2.0 2.0	10.8 9.0	16.2 11.5	1.5 1.5	18.0 12.5	ns
t <sub>PHL</sub>	Propagation Delay CP to Q <sub>n</sub>	2.7 3.3 ± 0.3	2.0 2.0	10.2 8.5	15.5 11.0	1.5 1.5	17.0 12.0	ns
t <sub>PHL</sub>	Propagation Delay MR to Q <sub>n</sub>	2.7 3.3 ± 0.3	2.5 2.5	10.8 9.0	16.2 11.5	2.0 2.0	18.0 12.5	ns
t <sub>OSHL</sub> t <sub>OSLH</sub>	Output to Output Skew*	2.7 3.3 ± 0.3		1.0 1.0	1.5 1.5		1.5 1.5	ns

\* Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW ( $t_{OSHL}$ ) or LOW to HIGH ( $t_{OSLH}$ ). Parameter guaranteed by design.

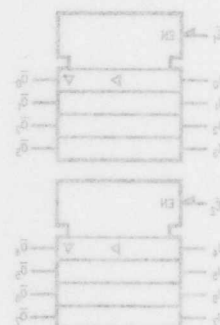
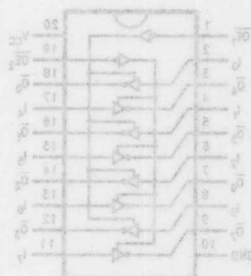
**AC Operating Requirements:** See Section 2 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	74LVQ174		74LVQ174	Units
			T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF		T <sub>A</sub> = −40°C to +85°C C <sub>L</sub> = 50 pF	
			Typ	Guaranteed Minimum		
t <sub>s</sub>	Setup Time, HIGH or LOW D <sub>n</sub> to CP	2.7 3.3 ±0.3	3.0	8.0	10.0	ns
			2.5	6.5	7.0	
t <sub>h</sub>	Hold Time, HIGH or LOW D <sub>n</sub> to CP	2.7 3.3 ±0.3	1.2	4.0	4.5	ns
			1.0	3.0	3.0	
t <sub>w</sub>	MR Pulse Width, LOW	2.7 3.3 ±0.3	1.2	7.0	10.0	ns
			1.0	5.5	7.0	
t <sub>w</sub>	CP Pulse Width	2.7 3.3 ±0.3	1.2	7.0	10.0	ns
			1.0	5.5	7.0	
t <sub>rec</sub>	Recovery Time MR to CP	2.7 3.3 ±0.3	0	3.5	3.5	ns
			0	2.5	2.5	

**Capacitance**

Symbol	Parameter	Typ	Units	Conditions
C <sub>IN</sub>	Input Capacitance	4.5	pF	V <sub>CC</sub> = Open
C <sub>PD</sub> (Note 1)	Power Dissipation Capacitance	23	pF	V <sub>CC</sub> = 3.3V

Note 1: C<sub>PD</sub> is measured at 10 MHz.



Pin Names	Description
Q0-Q7	TRISTATE Output Enable Inputs

Inputs	Outputs	
	(Pin 12, 14, 16, 18)	(Pin 13, 15, 17, 19)
H	H	H
L	L	L
X	X	X

Order Number	SOIC	SOIC	SOIC
74LVQ174C	74LVQ174C	74LVQ174C	74LVQ174C
74LVQ174D	74LVQ174D	74LVQ174D	74LVQ174D
74LVQ174E	74LVQ174E	74LVQ174E	74LVQ174E
74LVQ174F	74LVQ174F	74LVQ174F	74LVQ174F
74LVQ174G	74LVQ174G	74LVQ174G	74LVQ174G
74LVQ174H	74LVQ174H	74LVQ174H	74LVQ174H
74LVQ174J	74LVQ174J	74LVQ174J	74LVQ174J
74LVQ174K	74LVQ174K	74LVQ174K	74LVQ174K
74LVQ174L	74LVQ174L	74LVQ174L	74LVQ174L
74LVQ174M	74LVQ174M	74LVQ174M	74LVQ174M
74LVQ174N	74LVQ174N	74LVQ174N	74LVQ174N
74LVQ174P	74LVQ174P	74LVQ174P	74LVQ174P
74LVQ174Q	74LVQ174Q	74LVQ174Q	74LVQ174Q
74LVQ174R	74LVQ174R	74LVQ174R	74LVQ174R
74LVQ174S	74LVQ174S	74LVQ174S	74LVQ174S
74LVQ174T	74LVQ174T	74LVQ174T	74LVQ174T
74LVQ174U	74LVQ174U	74LVQ174U	74LVQ174U
74LVQ174V	74LVQ174V	74LVQ174V	74LVQ174V
74LVQ174W	74LVQ174W	74LVQ174W	74LVQ174W
74LVQ174X	74LVQ174X	74LVQ174X	74LVQ174X
74LVQ174Y	74LVQ174Y	74LVQ174Y	74LVQ174Y
74LVQ174Z	74LVQ174Z	74LVQ174Z	74LVQ174Z

Inputs	Outputs	
	(Pin 12, 14, 16, 18)	(Pin 13, 15, 17, 19)
H	H	H
L	L	L
X	X	X

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = tri-state  
Z = high impedance



## 74LVQ240

### Low Voltage Octal Buffer/Line Driver with TRI-STATE® Outputs

#### General Description

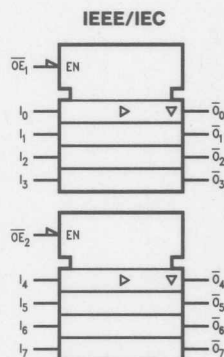
The LVQ240 is an inverting octal buffer and line driver, designed to be employed as a memory address driver, clock driver and bus oriented transmitter or receiver which provides improved PC board density.

#### Features

- Ideal for low power/low noise 3.3V applications
- Implements patented Quiet Series EMI reduction circuitry
- Available in SOIC JEDEC, SOIC EIAJ and QSOP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Improved latch-up immunity
- Guaranteed incident wave switching into 75Ω
- 4 kV minimum ESD immunity
- MIL-STD-883 54ACQ products are available for Military/Aerospace applications

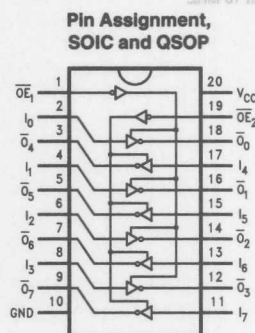
**Ordering Code:** See Section 11

#### Logic Symbol



TL/F/11611-1

#### Connection Diagram



TL/F/11611-2

#### Truth Tables

Inputs		Outputs (Pins 12, 14, 16, 18)
$\overline{OE}_1$	$I_n$	
L	L	H
L	H	L
H	X	Z

Inputs		Outputs (Pins 3, 5, 7, 9)
$\overline{OE}_2$	$I_n$	
L	L	H
L	H	L
H	X	Z

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial  
Z = High Impedance

Pin Names	Description
$\overline{OE}_1, \overline{OE}_2$	TRI-STATE Output Enable Inputs
$I_0-I_7$	Inputs
$O_0-O_7$	Outputs

	SOIC JEDEC	SOIC EIAJ	SSOP JEDEC
Order Number	74LVQ240SC 74LVQ240SCX	74LVQ240SJ 74LVQ240SJX	74LVQ240QSC 74LVQ240QSCX
See NS Package Number	M20B	M20D	MQA20

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V	Input Voltage ( $V_I$ )	0V to $V_{CC}$
DC Input Diode Current ( $I_{IK}$ )	-20 mA	Output Voltage ( $V_O$ )	0V to $V_{CC}$
$V_I = -0.5V$	-20 mA	Operating Temperature ( $T_A$ )	-40°C to +85°C
$V_I = V_{CC} + 0.5V$	+20 mA	74LVQ	
DC Input Voltage ( $V_I$ )	-0.5V to $V_{CC} + 0.5V$	Minimum Input Edge Rate $\Delta V/\Delta t$	
DC Output Diode Current ( $I_{OK}$ )	-20 mA	$V_{IN}$ 0.8V to 2.0V	125 mV/ns
$V_O = -0.5V$	-20 mA	$V_{CC}$ @ 3.0V	
$V_O = V_{CC} + 0.5V$	+20 mA		
DC Output Voltage ( $V_O$ )	-0.5V to $V_{CC} + 0.5V$		
DC Output Source or Sink Current ( $I_O$ )	$\pm 50$ mA		
DC $V_{CC}$ or Ground Current ( $I_{CC}$ or $I_{GND}$ )	$\pm 400$ mA		
Storage Temperature ( $T_{STG}$ )	-65°C to +150°C		
DC Latch-Up Source or Sink Current	$\pm 300$ mA		

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## DC Characteristics

Symbol	Parameter	V <sub>CC</sub> (V)	74LVQ240		74LVQ240		Units	Conditions
			T <sub>A</sub> = +25°C		T <sub>A</sub> = −40°C to +85°C			
			Typ	Guaranteed Limits				
V <sub>IH</sub>	Minimum High Level Input Voltage	3.0	1.5	2.0	2.0		V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> − 0.1V
V <sub>IL</sub>	Maximum Low Level Input Voltage	3.0	1.5	0.8	0.8		V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> − 0.1V
V <sub>OH</sub>	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9		V	I <sub>OUT</sub> = −50 μA
		3.0		2.58	2.48		V	*V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OH</sub> = −12 mA
V <sub>OL</sub>	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1		V	I <sub>OUT</sub> = 50 μA
		3.0		0.36	0.44		V	*V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OL</sub> = 12 mA
I <sub>IN</sub>	Maximum Input Leakage Current	3.6		±0.1	±1.0		μA	V <sub>I</sub> = V <sub>CC</sub> , GND

\*All outputs loaded; thresholds on input associated with output under test.

\*Stress is defined as the exposure of the device to conditions beyond the recommended operating conditions for a limited time. The device is not intended to be operated at these conditions. Exceeding these conditions may affect device reliability.

## DC Characteristics (Continued)

Symbol	Parameter	V <sub>CC</sub> (V)	74LVQ240		74LVQ240		Units	Conditions
			T <sub>A</sub> = +25°C		T <sub>A</sub> = −40°C to +85°C			
			Typ	Guaranteed Limits				
I <sub>OLD</sub>	†Minimum Dynamic Output Current	3.6			36		mA	V <sub>OLD</sub> = 0.8V Max (Note 1)
I <sub>OHD</sub>		3.6			−25		mA	V <sub>OHD</sub> = 2.0V Min (Note 1)
I <sub>CC</sub>	Maximum Quiescent Supply Current	3.6		4.0	40.0		μA	V <sub>IN</sub> = V <sub>CC</sub> or GND
I <sub>OZ</sub>	Maximum TRI-STATE Leakage Current	3.6		±0.25	±2.5		μA	V <sub>I</sub> (OE) = V <sub>IL</sub> , V <sub>IH</sub> V <sub>I</sub> = V <sub>CC</sub> , GND V <sub>O</sub> = V <sub>CC</sub> , GND
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	3.3	0.4	0.8			V	(Notes 2, 3)
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	3.3	−0.4	−0.8			V	(Notes 2, 3)
V <sub>IHD</sub>	Maximum High Level Dynamic Input Voltage	3.3	1.6	2.0			V	(Notes 2, 4)
V <sub>ILD</sub>	Maximum Low Level Dynamic Input Voltage	3.3	1.6	0.8			V	(Notes 2, 4)

† Maximum test duration 2.0 ms, one output loaded at a time.

**Note 1:** Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed for 74LVQ.

**Note 2:** Worst case package.

**Note 3:** Max number of outputs defined as (n). Data Inputs are driven 0V to 3.3V. One output @ GND.

**Note 4:** Max number of Data Inputs (n) switching. n – 1 Inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V<sub>ILD</sub>), 0V to threshold (V<sub>IHD</sub>), f = 1 MHz.

## AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	74LVQ240			74LVQ240		Units
			T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF			T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF		
			Min	Typ	Max	Min	Max	
t <sub>PHL</sub> , t <sub>PLH</sub>	Propagation Delay Data to Output	2.7 3.3 ± 0.3	2.0 2.0	8.4 7.0	14.0 10.0	2.0 2.0	15.0 10.5	ns
t <sub>PZL</sub> , t <sub>PZH</sub>	Output Enable Time	2.7 3.3 ± 0.3	2.5 2.5	9.6 8.0	16.9 12.0	2.5 2.5	18.0 12.5	ns
t <sub>PHZ</sub> , t <sub>PLZ</sub>	Output Disable Time	2.7 3.3 ± 0.3	1.0 1.0	10.2 8.5	19.0 13.5	1.0 1.0	20.0 14.0	ns
t <sub>OSHL</sub> , t <sub>OSLH</sub>	Output to Output Skew *Data to Output	2.7 3.3 ± 0.3		1.0 1.0	1.5 1.5		1.5 1.5	ns

\* Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t<sub>OSHL</sub>) or LOW to HIGH (t<sub>OSLH</sub>). Parameter guaranteed by design.

## Capacitance

Symbol	Parameter	Typ	Units	Conditions
$C_{IN}$	Input Capacitance	4.5	pF	$V_{CC} = \text{Open}$
$C_{PD}$ (Note 1)	Power Dissipation Capacitance	70	pF	$V_{CC} = 3.3V$

Note 1:  $C_{PD}$  is measured at 10 MHz.

### Features

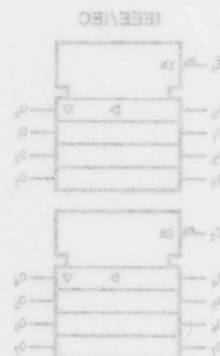
- Ideal for low power/low noise 3.3V applications
- Implements patented Quiet Series EMI reduction circuitry
- Available in SOIC JEDEC, SOIC EIA1 and QSOIP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Improved latch-up immunity
- Guaranteed incident wave switching into 75Ω
- 4 kV minimum ESD immunity
- MIL-STD-883 84AOC products are available for Mil/Aerospace applications

### General Description

The LVQ240 is an octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter or receiver which provides improved PC board density.

Ordering Code: See Section 11

### Logic Symbol



### Truth Tables

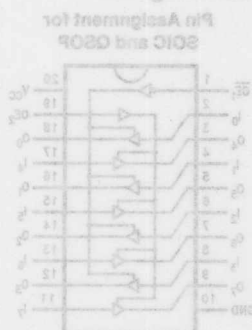
Inputs	$\overline{OE}_1$	$\overline{OE}_2$	Outputs (pins 12, 14, 16, 18)
L	L	L	L
L	L	H	H
L	X	X	Z

Inputs	$\overline{OE}_1$	$\overline{OE}_2$	Outputs (pins 2, 4, 6, 8)
L	L	L	L
L	L	H	H
L	X	X	Z

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Indeterminate  
Z = High Impedance

### Connection Diagram



LVQ240-2

LVQ240-1

Pin Names	Description
$\overline{OE}_1$ , $\overline{OE}_2$	TRI-STATE Output Enable Inputs
$I_1$ - $I_7$	Inputs
$O_1$ - $O_7$	Outputs

Order Number	SOIC JEDEC	SOIC EIA1	QSOIP JEDEC
LVQ240HSC	LVQ240HSC	LVQ240HSC	LVQ240HSC
LVQ240HSCX	LVQ240HSCX	LVQ240HSCX	LVQ240HSCX
LVQ240HSCX	LVQ240HSCX	LVQ240HSCX	LVQ240HSCX



## 74LVQ241

### Low Voltage Octal Buffer/Line Driver with TRI-STATE® Outputs

#### General Description

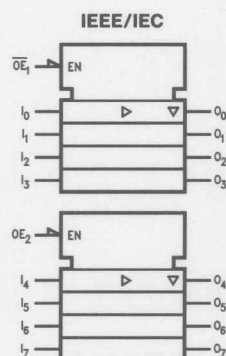
The LVQ241 is an octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter or receiver which provides improved PC board density.

#### Features

- Ideal for low power/low noise 3.3V applications
- Implements patented Quiet Series EMI reduction circuitry
- Available in SOIC JEDEC, SOIC EIAJ and QSOP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Improved latch-up immunity
- Guaranteed incident wave switching into 75Ω
- 4 kV minimum ESD immunity
- MIL-STD-883 54ACQ products are available for Military/Aerospace applications

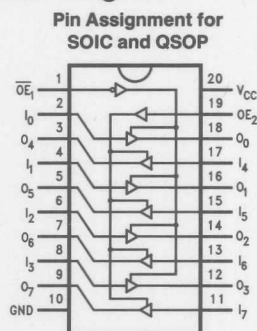
**Ordering Code:** See Section 11

#### Logic Symbol



TL/F/11355-1

#### Connection Diagram



TL/F/11355-2

#### Truth Tables

Inputs		Outputs (Pins 12, 14, 16, 18)
OE <sub>1</sub>	I <sub>n</sub>	
L	L	L
L	H	H
H	X	Z

Inputs		Outputs (Pins 3, 5, 7, 9)
OE <sub>2</sub>	I <sub>n</sub>	
L	X	Z
H	H	H
H	L	L

H = HIGH Voltage Level    L = LOW Voltage Level  
X = Immaterial                Z = High Impedance

Pin Names	Description
OE <sub>1</sub> , OE <sub>2</sub>	TRI-STATE Output Enable Inputs
I <sub>0</sub> -I <sub>7</sub>	Inputs
O <sub>0</sub> -O <sub>7</sub>	Outputs

	SOIC JEDEC	SOIC EIAJ	SSOP JEDEC
Order Number	74LVQ241SC 74LVQ241SCX	74LVQ241SJ 74LVQ241SJX	74LVQ241QSC 74LVQ241QSCX
See NS Package Number	M20B	M20D	MQA20

**Absolute Maximum Rating** (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )  $-0.5V$  to  $+7.0V$

DC Input Diode Current ( $I_{IK}$ )

$V_I = -0.5V$

$V_I = V_{CC} + 0.5V$

DC Input Voltage ( $V_I$ )

DC Output Diode Current ( $I_{OK}$ )

$V_O = -0.5V$

$V_O = V_{CC} + 0.5V$

DC Output Voltage ( $V_O$ )

DC Output Source

or Sink Current ( $I_O$ )

DC  $V_{CC}$  or Ground Current  
( $I_{CC}$  or  $I_{GND}$ )

Storage Temperature ( $T_{STG}$ )

DC Latch-Up Source or

Sink Current

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Recommended Operating Conditions**

Supply Voltage ( $V_{CC}$ )

$2.0V$  to  $3.6V$

Input Voltage ( $V_I$ )

$0V$  to  $V_{CC}$

Output Voltage ( $V_O$ )

$0V$  to  $V_{CC}$

Operating Temperature ( $T_A$ )

74LVQ

$-40^\circ C$  to  $+85^\circ C$

Minimum Input Edge Rate  $\Delta V/\Delta t$

$V_{IN}$   $0.8V$  to  $2.0V$

$V_{CC}$   $3.0V$

$125 mV/ns$

**DC Characteristics**

Symbol	Parameter	V <sub>CC</sub> (V)	74LVQ241		74LVQ241		Units	Conditions
			T <sub>A</sub> = +25°C		T <sub>A</sub> = −40°C to +85°C			
			Typ	Guaranteed Limits				
V <sub>IH</sub>	Minimum High Level Input Voltage	3.0	1.5	2.0	2.0	V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> − 0.1V	
V <sub>IL</sub>	Maximum Low Level Input Voltage	3.0	1.5	0.8	0.8	V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> + 0.1V	
V <sub>OH</sub>	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I <sub>OUT</sub> = −50 μA	
		3.0		2.58	2.48	V	*V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OH</sub> = −12 mA	
V <sub>OL</sub>	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I <sub>OUT</sub> = 50 μA	
		3.0		0.36	0.44	V	*V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OL</sub> = 12 mA	
I <sub>IN</sub>	Maximum Input Leakage Current	3.6		±0.1	±1.0	μA	V <sub>I</sub> = V <sub>CC</sub> , GND	

\*All outputs loaded; thresholds on input associated with output under test.

Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = +25°C		T <sub>A</sub> = −40°C to +85°C		Units	Conditions
			Typ	Guaranteed Limits				
I <sub>OLD</sub>	†Minimum Dynamic Output Current	3.6			36		mA	V <sub>OLD</sub> = 0.8V Max (Note 1)
I <sub>OHD</sub>		3.6			−25		mA	V <sub>OHD</sub> = 2.0V Min (Note 1)
I <sub>CC</sub>	Maximum Quiescent Supply Current	3.6		4.0	40.0		μA	V <sub>IN</sub> = V <sub>CC</sub> or GND
I <sub>OZ</sub>	Maximum TRI-STATE Leakage Current	3.6		±0.25	±2.5		μA	V <sub>I</sub> (OE) = V <sub>IL</sub> , V <sub>IH</sub> V <sub>I</sub> = V <sub>CC</sub> , GND V <sub>O</sub> = V <sub>CC</sub> , GND
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	3.3	0.4	0.8			V	(Notes 2, 3)
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	3.3	−0.4	−0.8			V	(Notes 2, 3)
V <sub>IHD</sub>	Maximum High Level Dynamic Input Voltage	3.3	1.6	2.0			V	(Notes 2, 4)
V <sub>ILD</sub>	Maximum Low Level Dynamic Input Voltage	3.3	1.6	0.8			V	(Notes 2, 4)

†Maximum test duration 2.0 ms, one output loaded at a time.

**Note 1:** Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed for 74LVQ.

**Note 2:** Worst case package.

**Note 3:** Max number of outputs defined as (n). Data Inputs are driven 0V to 3.3V. One output @ GND.

**Note 4:** Max number of Data Inputs (n) switching, n−1 Inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V<sub>ILD</sub>), 0V to threshold (V<sub>IHD</sub>), f = 1 MHz.

## AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	74LVQ241 T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF			74LVQ241 T <sub>A</sub> = −40°C to +85°C C <sub>L</sub> = 50 pF		Units
			Min	Typ	Max	Min	Max	
t <sub>PHL</sub>	Propagation Delay	2.7	2.0	7.8	12.7	2.0	14.0	ns
t <sub>PLH</sub>	Data to Output	3.3 ±0.3	2.0	6.5	9.0	2.0	9.5	
t <sub>PZL</sub>	Output Enable Time	2.7	2.5	9.6	18.3	2.5	19.0	ns
t <sub>PZH</sub>		3.3 ±0.3	2.5	8.0	13.0	2.5	13.5	
t <sub>PHZ</sub>	Output Disable Time	2.7	1.0	10.2	20.4	1.0	21.0	ns
t <sub>PLZ</sub>		3.3 ±0.3	1.0	8.5	14.5	1.0	15.0	
t <sub>OSHL</sub>	Output to Output Skew *Data to Output	2.7		1.0	1.5		1.5	ns
t <sub>OSLH</sub>		3.3 ±0.3		1.0	1.5		1.5	

\*Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t<sub>OSHL</sub>) or LOW to HIGH (t<sub>OSLH</sub>). Parameter guaranteed by design.

Symbol	Parameter	typ	Units	Conditions
C <sub>IN</sub>	Input Capacitance	4.5	pF	V <sub>CC</sub> = Open
C <sub>PD</sub> (Note 1)	Power Dissipation Capacitance	70	pF	V <sub>CC</sub> = 3.3V

Note 1: C<sub>PD</sub> is measured at 10 MHz.

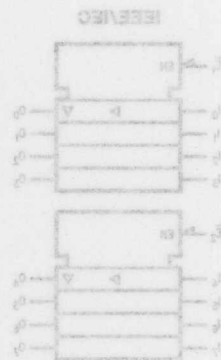
## Features

- Ideal for low power/low noise 3.3V applications
- Implements patented Output Series EMI reduction circuitry
- Available in SOIC JEDEC, SOIC EIAJ and QSOF packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Improved latch-up immunity
- Guaranteed incident wave switching into 75Ω
- 4 kV minimum ESD immunity
- MIL-STD-883 54ACD products are available for Mil/Aerospace applications

## General Description

The LV0244 is an octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter or receiver which provides improved PC board density.

## Logic Symbol

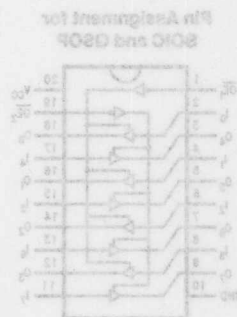


## Truth Tables

Inputs OE <sub>1</sub> (pins 12, 14, 16, 18)	I <sub>1</sub>	I <sub>2</sub>	I <sub>3</sub>	I <sub>4</sub>	I <sub>5</sub>	I <sub>6</sub>	I <sub>7</sub>	I <sub>8</sub>	Outputs (pins 3, 5, 7, 9)
L	L	L	L	L	L	L	L	L	L
L	L	L	L	L	L	L	L	L	L
L	L	L	L	L	L	L	L	L	L
L	L	L	L	L	L	L	L	L	L
L	L	L	L	L	L	L	L	L	L
L	L	L	L	L	L	L	L	L	L
L	L	L	L	L	L	L	L	L	L
L	L	L	L	L	L	L	L	L	L

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Indeterminate  
Z = High Impedance

## Connection Diagram



LV0244-1

Pin Name	Description
OE <sub>1</sub> , OE <sub>2</sub>	TRI-STATE Output Enable Inputs
I <sub>1</sub> - I <sub>8</sub>	Inputs
O <sub>1</sub> - O <sub>8</sub>	Outputs

Order Number	SOIC JEDEC	SOIC EIAJ	QSOF JEDEC
74LV0244-1	74LV0244-1	74LV0244-1	74LV0244-1
74LV0244-2	74LV0244-2	74LV0244-2	74LV0244-2
74LV0244-3	74LV0244-3	74LV0244-3	74LV0244-3
74LV0244-4	74LV0244-4	74LV0244-4	74LV0244-4
74LV0244-5	74LV0244-5	74LV0244-5	74LV0244-5
74LV0244-6	74LV0244-6	74LV0244-6	74LV0244-6
74LV0244-7	74LV0244-7	74LV0244-7	74LV0244-7
74LV0244-8	74LV0244-8	74LV0244-8	74LV0244-8
74LV0244-9	74LV0244-9	74LV0244-9	74LV0244-9
74LV0244-10	74LV0244-10	74LV0244-10	74LV0244-10
74LV0244-11	74LV0244-11	74LV0244-11	74LV0244-11
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74LV0244-84	74LV0244-84	74LV0244-84	74LV0244-84
74LV0244-85	74LV0244-85	74LV0244-85	74LV0244-85
74LV0244-86	74LV0244-86	74LV0244-86	74LV0244-86
74LV0244-87	74LV0244-87	74LV0244-87	74LV0244-87
74LV0244-88	74LV0244-88	74LV0244-88	74LV0244-88
74LV0244-89	74LV0244-89	74LV0244-89	74LV0244-89
74LV0244-90	74LV0244-90	74LV0244-90	74LV0244-90
74LV0244-91	74LV0244-91	74LV0244-91	74LV0244-91
74LV0244-92	74LV0244-92	74LV0244-92	74LV0244-92
74LV0244-93	74LV0244-93	74LV0244-93	74LV0244-93
74LV0244-94	74LV0244-94	74LV0244-94	74LV0244-94
74LV0244-95	74LV0244-95	74LV0244-95	74LV0244-95
74LV0244-96	74LV0244-96	74LV0244-96	74LV0244-96
74LV0244-97	74LV0244-97	74LV0244-97	74LV0244-97
74LV0244-98	74LV0244-98	74LV0244-98	74LV0244-98
74LV0244-99	74LV0244-99	74LV0244-99	74LV0244-99
74LV0244-100	74LV0244-100	74LV0244-100	74LV0244-100



## 74LVQ244

### Low Voltage Octal Buffer/Line Driver with TRI-STATE® Outputs

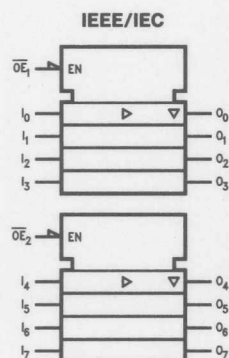
#### General Description

The LVQ244 is an octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter or receiver which provides improved PC board density.

#### Features

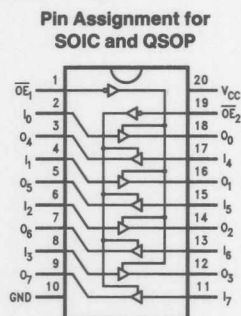
- Ideal for low power/low noise 3.3V applications
- Implements patented Quiet Series EMI reduction circuitry
- Available in SOIC JEDEC, SOIC EIAJ and QSOP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Improved latch-up immunity
- Guaranteed incident wave switching into 75Ω
- 4 kV minimum ESD immunity
- MIL-STD-883 54ACQ products are available for Military/Aerospace applications

#### Ordering Code: See Section 11 Logic Symbol



TL/F/11356-1

#### Connection Diagram



TL/F/11356-2

#### Truth Tables

Inputs		Outputs (Pins 12, 14, 16, 18)
$\overline{OE}_1$	$I_n$	
L	L	L
L	H	H
H	X	Z

Inputs		Outputs (Pins 3, 5, 7, 9)
$\overline{OE}_2$	$I_n$	
L	L	L
L	H	H
H	X	Z

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial  
Z = High Impedance

Pin Names	Description
$\overline{OE}_1, \overline{OE}_2$	TRI-STATE Output Enable Inputs
$I_0-I_7$	Inputs
$O_0-O_7$	Outputs

	SOIC JEDEC	SOIC EIAJ	SSOP JEDEC
Order Number	74LVQ244SC 74LVQ244SCX	74LVQ244SJ 74LVQ244SJX	74LVQ244QSC 74LVQ244QSCX
See NS Package Number	M20B	M20D	MQA20

**Absolute Maximum Rating** (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Input Diode Current ( $I_{IK}$ )	
$V_I = -0.5V$	-20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage ( $V_I$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Diode Current ( $I_{OK}$ )	
$V_O = -0.5V$	-20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage ( $V_O$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Source or Sink Current ( $I_O$ )	±50 mA
DC $V_{CC}$ or Ground Current ( $I_{CC}$ or $I_{GND}$ )	±400 mA
Storage Temperature ( $T_{STG}$ )	-65°C to +150°C
DC Latch-Up Source or Sink Current	±300 mA

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Recommended Operating Conditions**

Supply Voltage ( $V_{CC}$ )	2.0V to 3.6V
LVQ	
Input Voltage ( $V_I$ )	0V to $V_{CC}$
Output Voltage ( $V_O$ )	0V to $V_{CC}$
Operating Temperature ( $T_A$ )	-40°C to +85°C
74LVQ	
Minimum Input Edge Rate $\Delta V/\Delta t$	
$V_{IN}$ from 0.8V to 2.0V	
$V_{CC} @ 3.0V$	125 mV/ns

**DC Electrical Characteristics**

Symbol	Parameter	V <sub>CC</sub> (V)	74LVQ244		74LVQ244	Units	Conditions
			T <sub>A</sub> = +25°C		T <sub>A</sub> = −40°C to +85°C		
			Typ	Guaranteed Limits			
V <sub>IH</sub>	Minimum High Level Input Voltage	3.0	1.5	2.0	2.0	V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> − 0.1V
V <sub>IL</sub>	Maximum Low Level Input Voltage	3.0	1.5	0.8	0.8	V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> − 0.1V
V <sub>OH</sub>	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I <sub>OUT</sub> = −50 μA
				2.58	2.48	V	*V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OH</sub> = −12 mA
V <sub>OL</sub>	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I <sub>OUT</sub> = 50 μA
				0.36	0.44	V	*V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OL</sub> = 12 mA
I <sub>IN</sub>	Maximum Input Leakage Current	3.6		±0.1	±1.0	μA	V <sub>I</sub> = V <sub>CC</sub> , GND

\*All outputs loaded thresholds on input associated with output under test.

Symbol	Parameter	Typ	Units	Conditions
$C_{in}$	Input Capacitance	4.5	pF	$V_{CC} = \text{Open}$
$C_{pd}$	Power Dissipation Capacitance	70	pF	$V_{CC} = 3.3V$

Note:  $C_{pd}$  is measured at 10 MHz.

## DC Electrical Characteristics (Continued)

Symbol	Parameter	V <sub>CC</sub> (V)	74LVQ244		Units	Conditions	
			T <sub>A</sub> = +25°C				
			T <sub>A</sub> = −40°C to +85°C				
			Typ	Guaranteed Limits			
I <sub>OLD</sub>	†Minimum Dynamic Output Current	3.6			36	mA	V <sub>OLD</sub> = 0.8V Max (Note 1)
I <sub>OHD</sub>		3.6			−25	mA	V <sub>OHD</sub> = 2.0V Min (Note 1)
I <sub>CC</sub>	Maximum Quiescent Supply Current	3.6		4.0	−40.0	μA	V <sub>IN</sub> = V <sub>CC</sub> or GND
I <sub>OZ</sub>	Maximum TRI-STATE Leakage Current	3.6		±0.25	±2.5	μA	V <sub>I</sub> (OE) = V <sub>IL</sub> , V <sub>IH</sub> V <sub>I</sub> = V <sub>CC</sub> , GND V <sub>O</sub> = V <sub>CC</sub> , GND
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	3.3	0.4	0.8		V	(Notes 2, 3)
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	3.3	−0.4	−0.8		V	(Notes 2, 3)
V <sub>IHD</sub>	Minimum High Level Dynamic Input Voltage	3.3	1.7	2.0		V	(Notes 2, 4)
V <sub>ILD</sub>	Maximum Low Level Dynamic Input Voltage	3.3	1.7	0.8		V	(Notes 2, 4)

† Maximum test duration 2.0 ms, one output loaded at a time.

**Note 1:** Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed for 74LVQ.

**Note 2:** Worst case package.

**Note 3:** Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V; one output at GND.

**Note 4:** Max number of Data Inputs (n) switching. (n - 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V<sub>ILD</sub>), 0V to threshold (V<sub>IHD</sub>), f = 1 MHz.

## AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	74LVQ244			74LVQ244		Units
			T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF			T <sub>A</sub> = −40°C to +85°C C <sub>L</sub> = 50 pF		
			Min	Typ	Max	Min	Max	
t <sub>PHL</sub>	Propagation Delay	2.7	2.0	8.4	12.7	2.0	14.0	ns
t <sub>PLH</sub>	Data to Output	3.3 ± 0.3	2.0	7.0	9.0	2.0	9.5	
t <sub>PZL</sub>	Output Enable Time	2.7	2.5	9.6	16.9	2.5	18.0	ns
t <sub>PZH</sub>		3.3 ± 0.3	2.5	8.0	12.0	2.5	12.5	
t <sub>PHZ</sub>	Output Disable Time	2.7	1.0	10.8	19.0	1.0	20.0	ns
t <sub>PLZ</sub>		3.3 ± 0.3	1.0	9.0	13.5	1.0	14.0	
t <sub>OSSL</sub>	Output to Output	2.7		1.0	1.5		1.5	ns
t <sub>OSLH</sub>	Skew* Data to Output	3.3 ± 0.3		1.0	1.5		1.5	

\*Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t<sub>OSSL</sub>) or LOW to HIGH (t<sub>OSLH</sub>). Parameter guaranteed by design.

## Capacitance

Symbol	Parameter	Typ	Units	Conditions
C <sub>IN</sub>	Input Capacitance	4.5	pF	V <sub>CC</sub> = Open
C <sub>PD</sub>	Power Dissipation Capacitance	70	pF	V <sub>CC</sub> = 3.3V

**Note 1:** C<sub>PD</sub> is measured at 10 MHz.



## 74LVQ245

# Low Voltage Octal Bidirectional Transceiver with TRI-STATE® Inputs/Outputs

## General Description

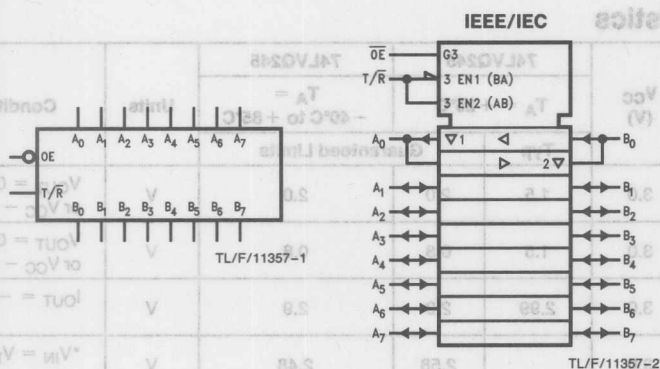
The LVQ245 contains eight non-inverting bidirectional buffers with TRI-STATE outputs and is intended for bus-oriented applications. Current sinking capability is 12 mA at both the A and B ports. The Transmit/Receive (T/R) input determines the direction of data flow through the bidirectional transceiver. Transmit (active-HIGH) enables data from A ports to B ports; Receive (active-LOW) enables data from B ports to A ports. The Output Enable input, when HIGH, disables both A and B ports by placing them in a HIGH Z condition.

## Features

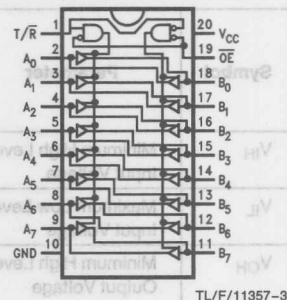
- Ideal for low power/low noise 3.3V applications
- Implements patented Quiet Series EMI reduction circuitry
- Available in SOIC JEDEC, SOIC EIAJ and QSOP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Improved latch-up immunity
- Guaranteed incident wave switching into 75Ω
- 4 kV minimum ESD immunity
- MIL-STD-883 54 ACQ products are available for Military/Aerospace applications

**Ordering Code:** See Section 11

## Logic Symbols



## Pin Assignment for SOIC and QSOP



## Truth Table

Inputs		Outputs
OE	T/R	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	HIGH-Z State

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial

Pin Names	Description
OE	Output Enable Input
T/R	Transmit/Receive Input
A <sub>0</sub> -A <sub>7</sub>	Side A TRI-STATE Inputs or TRI-STATE Outputs
B <sub>0</sub> -B <sub>7</sub>	Side B TRI-STATE Inputs or TRI-STATE Outputs

	SOIC JEDEC	SOIC EIAJ	SSOP JEDEC
Order Number	74LVQ245SC 74LVQ245SCX	74LVQ245SJ 74LVQ245SJX	74LVQ245QSC 74LVQ245QSCX
See NS Package Number	M20B	M20D	MQA20

**Absolute Maximum Ratings** (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Input Diode Current ( $I_{IK}$ )	
$V_I = -0.5V$	-20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage ( $V_I$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Diode Current ( $I_{OK}$ )	
$V_O = -0.5V$	-20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage ( $V_O$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Source or Sink Current ( $I_O$ )	±50 mA
DC $V_{CC}$ or Ground Current ( $I_{CC}$ or $I_{GND}$ )	±400 mA
Storage Temperature ( $T_{STG}$ )	-65°C to +150°C
DC Latch-Up Source or Sink Current	±300 mA

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Recommended Operating Conditions**

Supply Voltage ( $V_{CC}$ )	2.0V to 3.6V
LVQ	0V to $V_{CC}$
Input Voltage ( $V_I$ )	0V to $V_{CC}$
Output Voltage ( $V_O$ )	0V to $V_{CC}$
Operating Temperature ( $T_A$ )	-40°C to +85°C
74LVQ	
Minimum Input Edge Rate ( $\Delta V/\Delta t$ )	
$V_{IN}$ from 0.8V to 2.0V	
$V_{CC} @ 3.0V$	125 mV/ ns

**DC Electrical Characteristics**

Symbol	Parameter	V <sub>CC</sub> (V)	74LVQ245		74LVQ245		Units	Conditions
			T <sub>A</sub> = +25°C		T <sub>A</sub> = −40°C to +85°C			
			Typ	Guaranteed Limits				
V <sub>IH</sub>	Minimum High Level Input Voltage	3.0	1.5	2.0	2.0	V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> − 0.1V	
V <sub>IL</sub>	Maximum Low Level Input Voltage	3.0	1.5	0.8	0.8	V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> − 0.1V	
V <sub>OH</sub>	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I <sub>OUT</sub> = −50 μA	
		3.0		2.58	2.48	V	*V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OH</sub> = −12 mA	
V <sub>OL</sub>	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I <sub>OUT</sub> = 50 μA	
		3.0		0.36	0.44	V	*V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OL</sub> = +12 mA	
I <sub>IN</sub>	Maximum Input Leakage Current	3.6		±0.1	±1.0	μA	V <sub>I</sub> = V <sub>CC</sub> , GND	

\*All outputs loaded; thresholds on input associated with output under test.

Order Number	74LVQ245C	74LVQ245S	74LVQ245D
See NS Package Number	M20B	M20D	M20C

## DC Electrical Characteristics (Continued)

Symbol	Parameter	V <sub>CC</sub> (V)	74LVQ245		74LVQ245		Units	Conditions
			T <sub>A</sub> = +25°C		T <sub>A</sub> = −40°C to +85°C			
			Typ	Guaranteed Limits				
I <sub>OLD</sub>	†Minimum Dynamic Output Current	3.6			36	mA	V <sub>OLD</sub> = 0.8V Max (Note 1)	
I <sub>OHD</sub>		3.6			−25	mA	V <sub>OHD</sub> = 2.0V Min (Note 1)	
I <sub>CC</sub>	Maximum Quiescent Supply Current	3.6		4.0	40.0	μA	V <sub>IN</sub> = V <sub>CC</sub> or GND	
I <sub>OZT</sub>	Maximum I/O Leakage Current	3.6		±0.3	±3.0	μA	V <sub>I</sub> (OE) = V <sub>IL</sub> , V <sub>IH</sub> V <sub>I</sub> = V <sub>CC</sub> , GND V <sub>O</sub> = V <sub>CC</sub> , GND	
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	3.3	0.5	0.8		V	(Notes 2, 3)	
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	3.3	−0.5	−0.8		V	(Notes 2, 3)	
V <sub>IHD</sub>	Maximum High Level Dynamic Input Voltage	3.3	1.6	2.0		V	(Notes 2, 4)	
V <sub>ILD</sub>	Maximum Low Level Dynamic Input Voltage	3.3	1.7	0.8		V	(Notes 2, 4)	

†Maximum test duration 2.0 ms, one output loaded at a time.

**Note 1:** Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed for 74LVQ.

**Note 2:** Worst case package.

**Note 3:** Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V; one output at GND.

**Note 4:** Max number of Data Inputs (n) switching. (n – 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V<sub>ILD</sub>), 0V to threshold (V<sub>IHD</sub>). f = 1 MHz.

## AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	74LVQ245			74LVQ245		Units
			T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF			T <sub>A</sub> = −40°C to +85°C C <sub>L</sub> = 50 pF		
			Min	Typ	Max	Min	Max	
t <sub>PHL</sub> , t <sub>PLH</sub>	Propagation Delay	2.7 3.3 ±0.3	2.0 2.0	9.0 7.5	14.0 10.0	2.0 2.0	15.0 10.5	ns
t <sub>PZL</sub> , t <sub>PZH</sub>	Output Enable Time	2.7 3.3 ±0.3	3.0 3.0	10.2 8.5	18.3 13.0	3.0 3.0	19.0 13.5	ns
t <sub>PHZ</sub> , t <sub>PLZ</sub>	Output Disable Time	2.7 3.3 ±0.3	1.0 1.0	10.2 8.5	20.4 14.5	1.0 1.0	21.0 15.0	ns
t <sub>OSHL</sub> , t <sub>OSLH</sub>	Output to Output Skew*	2.7 3.3 ±0.3		1.0 1.0	1.5 1.5		1.5 1.5	ns

\*Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t<sub>OSHL</sub>) or LOW to HIGH (t<sub>OSLH</sub>). Parameter guaranteed by design.

## Capacitance

Symbol	Parameter	Typ	Units	Conditions
$C_{IN}$	Input Capacitance	4.5	pF	$V_{CC} = \text{Open}$
$C_{I/O}$	Input/Output Capacitance	15	pF	$V_{CC} = 3.3V$
$C_{PD}$ (Note 1)	Power Dissipation Capacitance	67	pF	$V_{CC} = 3.3V$

Note 1:  $C_{PD}$  is measured at 10 MHz.

Symbol	Parameter	Typ	Units	Conditions
$V_{OH}$	Maximum High Level Dynamic Input Voltage	3.3	V	(Notes 2, 4)
$V_{OL}$	Maximum Low Level Dynamic Input Voltage	1.7	V	(Notes 2, 4)
$V_{IH}$	Maximum High Level Static Input Voltage	3.3	V	(Notes 2, 4)
$V_{IL}$	Maximum Low Level Static Input Voltage	0.8	V	(Notes 2, 4)
$I_{OZ}$	Maximum Leakage Current	$\pm 0.3$	$\mu A$	$V_I = V_{OH}$ or $V_{OL}$ , $V_O = V_{CC}$ or $GND$
$I_{CC}$	Maximum Quiescent Supply Current	4.0	$\mu A$	$V_{IN} = V_{CC}$ or $GND$
$I_{OH}$	Maximum Sink Current	—	mA	(Note 1)

Maximum test duration 5.0 ms, one output loaded at a time.  
 Note 1: Incident wave reflection on transmission lines with impedances as low as 75  $\Omega$  for commercial temperature range is guaranteed for LVQ245.  
 Note 2: Worst case packaging.  
 Note 3: Max number of outputs driven on (n). Data inputs are driven 0V to 3.3V, one output at GND.  
 Note 4: Max number of data inputs (n) switching (n - 1) inputs switching 0V to 3.3V, input-order-test switching: 3.3V to threshold ( $V_{IH}$ ), 0V to threshold ( $V_{IL}$ ), 1 = 1 MHz.

## AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	$V_{CC}$ (V)	Units	Typ	Min	Max
$t_{PHL}$	Propagation Delay	3.3	ns	2.0	1.0	3.0
$t_{PLH}$	Output Enable Time	3.3	ns	2.0	1.0	3.0
$t_{PZL}$	Output Disable Time	3.3	ns	2.0	1.0	3.0
$t_{OSH}$	Output to Output Skew*	3.3	ns	1.0	0.5	1.5

\*Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (faster) or LOW to HIGH (faster). Parameter guaranteed by design.



## 74LVQ273 Low Voltage Octal D Flip-Flop

### General Description

The LVQ273 has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset (MR) input load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output.

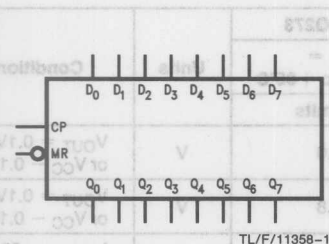
All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the MR input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

### Features

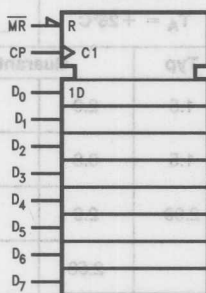
- Ideal for low power/low noise 3.3V applications
- Implements patented Quiet Series EMI reduction circuitry
- Available in SOIC JEDEC, SOIC EIAJ and QSOP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Improved latch-up immunity
- Guaranteed incident wave switching into 75Ω
- 4 kV minimum ESD immunity
- MIL-STD-883 54ACQ products are available for Military/Aerospace applications

**Ordering Code:** See Section 11

### Logic Symbols

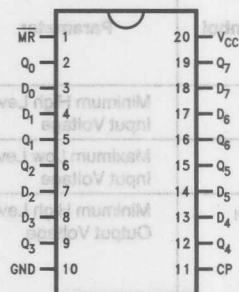


IEEE/IEC



### Connection Diagram

Pin Assignment for  
SOIC and QSOP



Pin Names	Description
D <sub>0</sub> -D <sub>7</sub>	Data Inputs
MR	Master Reset
CP	Clock Pulse Input
Q <sub>0</sub> -Q <sub>7</sub>	Data Outputs

	SOIC JEDEC	SOIC EIAJ	SSOP JEDEC
Order Number	74LVQ273SC 74LVQ273SCX	74LVQ273SJ 74LVQ273SJX	74LVQ273QSC 74LVQ273QSCX
See NS Package Number	M20B	M20D	MQA20

**Absolute Maximum Ratings** (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )  $-0.5V$  to  $+7.0V$

DC Input Diode Current ( $I_{IK}$ )

$V_I = -0.5V$   $-20\text{ mA}$

$V_I = V_{CC} + 0.5V$   $+20\text{ mA}$

DC Input Voltage ( $V_I$ )  $-0.5V$  to  $V_{CC} + 0.5V$

DC Output Diode Current ( $I_{OK}$ )

$V_O = -0.5V$   $-20\text{ mA}$

$V_O = V_{CC} + 0.5V$   $+20\text{ mA}$

DC Output Voltage ( $V_O$ )  $-0.5V$  to  $V_{CC} + 0.5V$

DC Output Source

or Sink Current ( $I_O$ )  $\pm 50\text{ mA}$

DC  $V_{CC}$  or Ground Current

( $I_{CC}$  or  $I_{GND}$ )  $\pm 400\text{ mA}$

Storage Temperature ( $T_{STG}$ )  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$

DC Latch-up Source or

Sink Current  $\pm 300\text{ mA}$

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Recommended Operating Conditions**

Supply Voltage ( $V_{CC}$ )

LVQ  $2.0V$  to  $3.6V$

Input Voltage ( $V_I$ )

$0V$  to  $V_{CC}$

Output Voltage ( $V_O$ )

$0V$  to  $V_{CC}$

Operating Temperature ( $T_A$ )

74LVQ  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$

Minimum Input Edge Rate  $\Delta V/\Delta t$

$V_{IN}$  from  $0.8V$  to  $2.0V$

$V_{CC} @ 3.0V$   $125\text{ mV/ns}$

**DC Characteristics**

Symbol	Parameter	V <sub>CC</sub> (V)	74LVQ273		74LVQ273	Units	Conditions
			T <sub>A</sub> = +25°C		T <sub>A</sub> = −40°C to +85°C		
			Typ	Guaranteed Limits			
V <sub>IH</sub>	Minimum High Level Input Voltage	3.0	1.5	2.0	2.0	V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> − 0.1V
V <sub>IL</sub>	Maximum Low Level Input Voltage	3.0	1.5	0.8	0.8	V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> − 0.1V
V <sub>OH</sub>	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I <sub>OUT</sub> = −50 μA
		3.0		2.58	2.48	V	*V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OH</sub> = −12 mA
V <sub>OL</sub>	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I <sub>OUT</sub> = 50 μA
		3.0		0.36	0.44	V	*V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OL</sub> = 12 mA
I <sub>IN</sub>	Maximum Input Leakage Current	3.6		±0.1	±1.0	μA	V <sub>I</sub> = V <sub>CC</sub> , GND

\*All outputs loaded; thresholds on input associated with output under test.

Order Number	74LVQ273C	74LVQ273J	74LVQ273S
See NS Package Number	M20B	M20D	M20A

Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = +25°C		T <sub>A</sub> = −40°C to +85°C		Units	Conditions
			Typ	Guaranteed Limits				
I <sub>OLD</sub>	†Minimum Dynamic Output Current	3.6			36		mA	V <sub>OLD</sub> = 0.8V Max (Note 1)
I <sub>OHD</sub>		3.6			−25		mA	V <sub>OHD</sub> = 2.0V Min (Note 1)
I <sub>CC</sub>	Maximum Quiescent Supply Current	3.6		4.0	40.0		μA	V <sub>IN</sub> = V <sub>CC</sub> or GND
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	3.3	0.4	0.8			V	(Notes 2, 3)
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	3.3	−0.3	−0.8			V	(Notes 2, 3)
V <sub>IHD</sub>	Maximum High Level Dynamic Input Voltage	3.3	1.7	2.0			V	(Notes 2, 4)
V <sub>ILD</sub>	Maximum Low Level Dynamic Input Voltage	3.3	1.6	0.8			V	(Notes 2, 4)

†Maximum test duration 2.0 ms, one output loaded at a time.

**Note 1:** Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed for 74LVQ.

**Note 2:** Worst case package.

**Note 3:** Max number of outputs defined as (n). Data Inputs are driven 0V to 3.3V; one output at GND.

**Note 4:** Max number of Data Inputs (n) switching. (n − 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V<sub>ILD</sub>), 0V to threshold (V<sub>IHD</sub>), f = 1 MHz.

## AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	74LVQ273			74LVQ273		Units
			T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF			T <sub>A</sub> = −40°C to +85°C C <sub>L</sub> = 50 pF		
			Min	Typ	Max	Min	Max	
f <sub>max</sub>	Maximum Clock Frequency	2.7 3.3 ± 0.3	50 90			45 75		MHz
t <sub>PLH</sub>	Propagation Delay CP to Q <sub>n</sub>	2.7 3.3 ± 0.3	4.0 4.0	9.6 8.0	17.6 12.5	3.0 3.0	20.0 14.0	ns
t <sub>PHL</sub>	Propagation Delay CP to Q <sub>n</sub>	2.7 3.3 ± 0.3	4.0 4.0	10.2 8.5	18.3 13.0	3.5 3.5	20.5 14.5	ns
t <sub>PHL</sub>	Propagation Delay MR to Q <sub>n</sub>	2.7 3.3 ± 0.3	4.0 4.0	10.2 8.5	18.3 13.0	3.5 3.5	20.0 14.0	ns
t <sub>OSHL</sub> , t <sub>OSLH</sub>	Output to Output Skew*	2.7 3.3 ± 0.3		1.0 1.0	1.5 1.5		1.5 1.5	ns

\*Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs within the same packaged device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t<sub>OSHL</sub>) or LOW to HIGH (t<sub>OSLH</sub>). Parameter guaranteed by design. Not tested.

**AC Operating Requirements:** See Section 2 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	74LVQ273		74LVQ273	Units
			T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF		T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF	
			Typ	Guaranteed Minimum		
t <sub>s</sub>	Setup Time, HIGH or LOW D <sub>n</sub> to CP	2.7 3.3 ± 0.3		6.5 5.0	8.5 6.0	ns
t <sub>h</sub>	Hold Time, HIGH or LOW D <sub>n</sub> to CP	2.7 3.3 ± 0.3		0.0 0.0	0.0 0.0	ns
t <sub>w</sub>	Clock Pulse Width HIGH or LOW	2.7 3.3 ± 0.3		7.0 5.5	8.5 6.0	ns
t <sub>w</sub>	MR Pulse Width HIGH or LOW	2.7 3.3 ± 0.3		7.0 5.5	8.5 6.0	ns
t <sub>w</sub>	Recovery Time MR to CP	2.7 3.3 ± 0.3		5.0 4.0	6.5 4.5	ns

**Capacitance**

Symbol	Parameter	Typ	Units	Conditions
C <sub>IN</sub>	Input Capacitance	4.5	pF	V <sub>CC</sub> = Open
C <sub>PD</sub> (Note 1)	Power Dissipation Capacitance	35	pF	V <sub>CC</sub> = 3.3V

Note 1: C<sub>PD</sub> is measured at 10 MHz.

**AC Electrical Characteristics:** See Section 2 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF		T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF		Units
			Min	Typ	Max	Max	
f <sub>max</sub>	Maximum Clock Frequency	2.7 3.3 ± 0.3	50 80		45 75		MHz
t <sub>PLH</sub>	Propagation Delay CP to Q <sub>n</sub>	2.7 3.3 ± 0.3	4.0 4.0	8.8 8.0	17.8 12.5	3.0 3.0	ns
t <sub>PHL</sub>	Propagation Delay CP to Q <sub>n</sub>	2.7 3.3 ± 0.3	4.0 4.0	10.2 8.5	18.3 13.0	3.5 3.5	ns
t <sub>PHL</sub>	Propagation Delay MR to Q <sub>n</sub>	2.7 3.3 ± 0.3	4.0 4.0	10.2 8.5	18.3 13.0	3.5 3.5	ns
t <sub>skew</sub>	Output to Output Skew*	2.7 3.3 ± 0.3		1.0 1.0	1.5 1.5	1.5 1.5	ns

\*Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs within the same packaged device. This specification applies to any output switching in the same direction, either HIGH to LOW (t<sub>skewH</sub>) or LOW to HIGH (t<sub>skewL</sub>). Parameter guaranteed by design, not tested.



## 74LVQ373

# Low Voltage Octal Transparent Latch with TRI-STATE® Outputs

## General Description

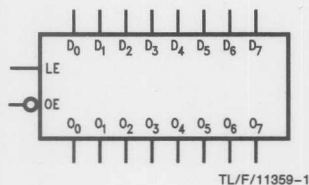
The LVQ373 consists of eight latches with TRI-STATE outputs for bus organized system applications. The latches appear transparent to the data when Latch Enable (LE) is HIGH. When LE is low, the data satisfying the input timing requirements is latched. Data appears on the bus when the Output Enable (OE) is LOW. When OE is HIGH, the bus output is in the high impedance state.

## Features

- Ideal for low power/low noise 3.3V applications
- Implements patented Quiet Series EMI reduction circuitry
- Available in SOIC JEDEC, SOIC EIAJ and QSOP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Improved latch-up immunity
- Guaranteed incident wave switching into 75Ω
- 4 kV minimum ESD immunity
- MIL-STD-883 54ACQ products are available for Military/Aerospace applications

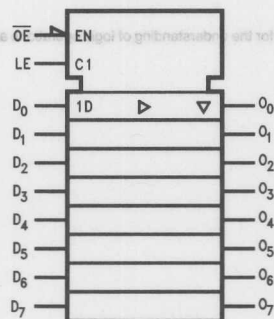
**Ordering Code:** See Section 11

## Logic Symbols



TL/F/11359-1

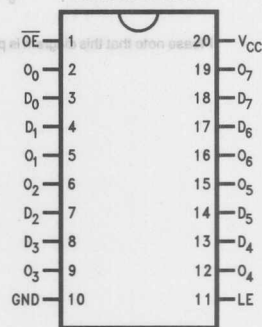
IEEE/IEC



TL/F/11359-2

## Connection Diagram

Pin Assignment for SOIC and QSOP



TL/F/11359-3

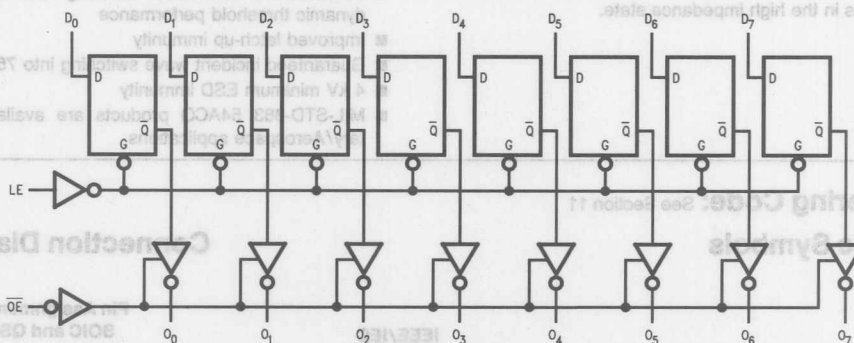
Pin Names	Description
D <sub>0</sub> -D <sub>7</sub>	Data Inputs
LE	Latch Enable Input
OE	Output Enable Input
Q <sub>0</sub> -Q <sub>7</sub>	TRI-STATE Latch Outputs

	SOIC JEDEC	SOIC EIAJ	SSOP JEDEC
Order Number	74LVQ373SC 74LVQ373SCX	74LVQ373SJ 74LVQ373SJX	74LVQ373QSC 74LVQ373QSCX
See NS Package Number	M20B	M20D	MQA20

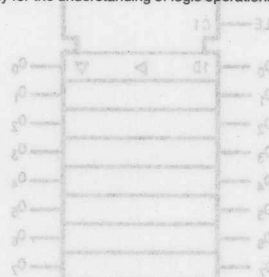
## Functional Description

The LVQ373 contains eight D-type latches with TRI-STATE standard outputs. When the Latch Enable (LE) input is HIGH, data on the  $D_n$  inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE standard outputs are controlled by the Output Enable ( $\overline{OE}$ ) input. When  $\overline{OE}$  is LOW, the standard outputs are in the 2-state mode. When  $\overline{OE}$  is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.



TL/F/11359-5

## Truth Table

Inputs			Outputs
LE	$\overline{OE}$	$D_n$	$O_n$
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	$O_0$

H = HIGH Voltage Level

L = LOW Voltage Level

Z = High Impedance

X = Immaterial

$O_0$  = Previous  $O_0$  before HIGH to Low transition of Latch Enable

Pin Number	Description
$O_0$ – $O_7$	TRI-STATE Latch Outputs
$\overline{OE}$	Output Enable Input
LE	Latch Enable Input
$D_0$ – $D_7$	Data Inputs

Order Number	SOIC JEDEC	SOIC EIA1	SOIC JEDEC
74LVQ373SC	74LVQ373SC	74LVQ373S1	74LVQ373SC
74LVQ373SCX	74LVQ373SCX	74LVQ373S1X	74LVQ373SCX
See NS Package Number	M209	M209	M209

## Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )	$-0.5V$ to $+7.0V$
DC Input Diode Current ( $I_{IK}$ )	$-20$ mA
$V_I = -0.5V$	$+20$ mA
$V_I = V_{CC} + 0.5V$	
DC Input Voltage ( $V_I$ )	$-0.5V$ to $V_{CC} + 0.5V$
DC Output Diode Current ( $I_{OK}$ )	$-20$ mA
$V_O = -0.5V$	$+20$ mA
$V_O = V_{CC} + 0.5V$	
DC Output Voltage ( $V_O$ )	$-0.5V$ to $V_{CC} + 0.5V$
DC Output Source or Sink Current ( $I_O$ )	$\pm 50$ mA
DC $V_{CC}$ or Ground Current ( $I_{CC}$ or $I_{GND}$ )	$\pm 400$ mA
Storage Temperature ( $T_{STG}$ )	$-65^\circ\text{C}$ to $+150^\circ\text{C}$
DC Latch-Up Source or Sink Current	$\pm 300$ mA

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## Recommended Operating Conditions

Supply Voltage ( $V_{CC}$ )	LVQ	$2.0V$ to $3.6V$
Input Voltage ( $V_I$ )		$0V$ to $V_{CC}$
Output Voltage ( $V_O$ )		$0V$ to $V_{CC}$
Operating Temperature ( $T_A$ )	74LVQ	$-40^\circ\text{C}$ to $+85^\circ\text{C}$
Minimum Input Edge Rate ( $\Delta V/\Delta t$ )		$V_{IN}$ from $0.8V$ to $2.0V$
$V_{CC} @ 3.0V$		$125$ mV/ns

## DC Characteristics

Symbol	Parameter	V <sub>CC</sub> (V)	74LVQ373		74LVQ373		Units	Conditions
			T <sub>A</sub> = +25°C		T <sub>A</sub> = −40°C to +85°C			
			Typ	Guaranteed Limits				
V <sub>IH</sub>	Minimum High Level Input Voltage	3.0	1.5	2.0	2.0	V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> − 0.1V	
V <sub>IL</sub>	Maximum Low Level Input Voltage	3.0	1.5	0.8	0.8	V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> − 0.1V	
V <sub>OH</sub>	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I <sub>OUT</sub> = −50 μA	
		3.0		2.58	2.48	V	*V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OH</sub> = −12 mA	
V <sub>OL</sub>	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I <sub>OUT</sub> = 50 μA	
		3.0		0.36	0.44	V	*V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OL</sub> = 12 mA	
I <sub>IN</sub>	Maximum Input Leakage Current	3.6		±0.1	±1.0	μA	V <sub>I</sub> = V <sub>CC</sub> , GND	

\*All outputs loaded; thresholds on input associated with output under test.

		(V)			Units	Conditions
		to +85°C				
		Typ	Guaranteed Limits			
I <sub>OLD</sub>	†Minimum Dynamic Output Current	3.6		36	mA	V <sub>OLD</sub> = 0.8V Max (Note 1)
I <sub>OHD</sub>		3.6		25	mA	V <sub>OHD</sub> = 2.0V Min (Note 1)
I <sub>CC</sub>	Maximum Quiescent Supply Current	3.6	4.0	40.0	μA	V <sub>IN</sub> = V <sub>CC</sub> or GND
I <sub>OZ</sub>	Maximum TRI-STATE Leakage Current	3.6	±0.25	±2.5	μA	V <sub>I</sub> (OE) = V <sub>IL</sub> , V <sub>IH</sub> V <sub>I</sub> = V <sub>CC</sub> , GND V <sub>O</sub> = V <sub>CC</sub> , GND
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	3.3	0.4	0.8	V	(Notes 2, 3)
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	3.3	−0.3	−0.8	V	(Notes 2, 3)
V <sub>IHD</sub>	Maximum High Level Dynamic Input Voltage	3.3	1.7	2.0	V	(Notes 2, 4)
V <sub>ILD</sub>	Maximum Low Level Dynamic Input Voltage	3.3	1.6	0.8	V	(Notes 2, 4)

† Maximum test duration 2.0 ms, one output loaded at a time.

**Note 1:** Incident wave switching on transmission lines with impedances as low as 75 $\Omega$  for commercial temperature range is guaranteed for 74LVQ.

**Note 2:** Worst case package.

**Note 3:** Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V; one output at GND.

**Note 4:** Max number of Data Inputs (n) switching. (n - 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold ( $V_{ILD}$ ), 0V to threshold ( $V_{IHD}$ ). f = 1 MHz.

## AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	74LVQ373			74LVQ373		Units
			T <sub>A</sub> = + 25°C C <sub>L</sub> = 50 pF			T <sub>A</sub> = − 40°C to + 85°C C <sub>L</sub> = 50 pF		
			Min	Typ	Max	Min	Max	
t <sub>PHL</sub> , t <sub>PLH</sub>	Propagation Delay D <sub>n</sub> to O <sub>n</sub>	2.7 3.3 ± 0.3	2.5	9.6	14.8	2.5	16.0	ns
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay LE to O <sub>n</sub>	2.7 3.3 ± 0.3	2.5	9.6	16.9	2.5	18.0	
t <sub>PZL</sub> , t <sub>PZH</sub>	Output Enable Time	2.7 3.3 ± 0.3	2.5	10.2	18.3	2.5	19.0	ns
t <sub>PHZ</sub> , t <sub>PLZ</sub>	Output Disable Time	2.7 3.3 ± 0.3	1.0	10.8	20.4	1.0	21.0	
t <sub>OSHL</sub> , t <sub>OSLH</sub>	Output to Output Skew*	2.7 3.3 ± 0.3	1.0	1.5	1.5	1.5	1.5	ns

\*Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW ( $t_{OSHL}$ ) or LOW to HIGH ( $t_{OSLH}$ ). Parameter guaranteed by design.

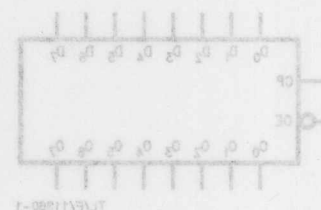
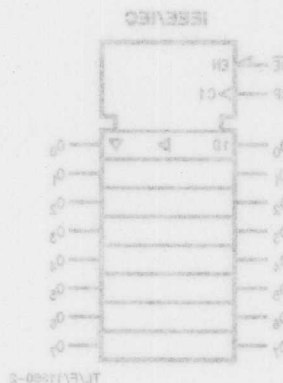
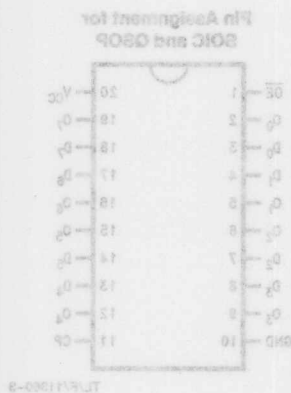
**AC Operating Requirements:** See Section 2 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	74LVQ373		74LVQ373	Units
			T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF		T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF	
			Typ	Guaranteed Minimum		
t <sub>S</sub>	Setup Time, HIGH or LOW	2.7 3.3 ± 0.3	0 0	4.0 3.0	4.5 3.0	ns
t <sub>H</sub>	Hold Time, HIGH or LOW	2.7 3.3 ± 0.3	0 0	1.5 1.5	1.5 1.5	ns
t <sub>W</sub>	LE Pulse Width, HIGH	2.7 3.3 ± 0.3	2.4 2.0	5.0 4.0	6.0 4.0	ns

**Capacitance**

Symbol	Parameter	Typ	Units	Conditions
C <sub>IN</sub>	Input Capacitance	4.5	pF	V <sub>CC</sub> = Open
C <sub>PD</sub> (Note 1)	Power Dissipation Capacitance	39	pF	V <sub>CC</sub> = 3.3V

Note 1: C<sub>PD</sub> is measured at 10 MHz.

**Connection Diagram**

Pin Names	Description
D <sub>0</sub> -D <sub>7</sub>	Data Inputs
CP	Clock Pulse Input
CE	TRI-STATE Output Enable Input
O <sub>0</sub> -O <sub>7</sub>	TRI-STATE Outputs

Order Number	SOIC JEDEC	SOIC SIA	SOIC JEDEC
TJLVQ373BC	TJLVQ373A	TJLVQ373A	TJLVQ373A
TJLVQ373CX	TJLVQ373A	TJLVQ373A	TJLVQ373A
See NS Package Number	M20B	M20D	M20A



## 74LVQ374

### Low Voltage Octal D Flip-Flop with TRI-STATE® Outputs

#### General Description

The LVQ374 is a high-speed, low-power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and TRI-STATE outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable ( $\overline{OE}$ ) are common to all flip-flops.

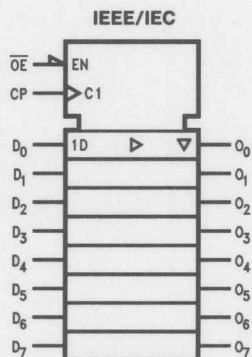
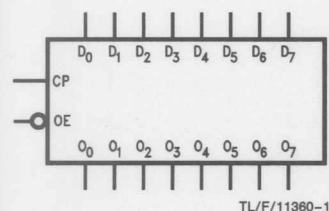
#### Features

- Ideal for low power/low noise 3.3V applications
- Implements patented Quiet Series EMI reduction circuitry
- Available in SOIC JEDEC, SOIC EIAJ and QSOP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Improved latch-up immunity
- Guaranteed incident wave switching into 75Ω
- 4 kV minimum ESD immunity
- Buffered positive edge-triggered clock
- TRI-STATE outputs drive bus lines or buffer memory address registers
- MIL-STD-883 54ACQ Products are available for Military/Aerospace Applications

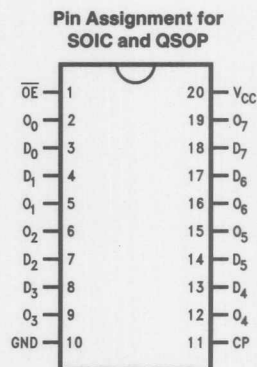
Conditions	Units
$V_{CC} = 3.3V$	pp
$V_{CC} = 3.3V$	pp

**Ordering Code:** See Section 11

#### Logic Symbols



#### Connection Diagram



Pin Names	Description
D <sub>0</sub> -D <sub>7</sub>	Data Inputs
CP	Clock Pulse Input
$\overline{OE}$	TRI-STATE Output Enable Input
Q <sub>0</sub> -Q <sub>7</sub>	TRI-STATE Outputs

	SOIC JEDEC	SOIC EIAJ	SOIC JEDEC
Order Number	74LVQ374SC 74LVQ374SCX	74LVQ374SJ 74LVQ374SJX	74LVQ374QSC 74LVQ374QSCX
See NS Package Number	M20B	M20D	MQA20

## Functional Description

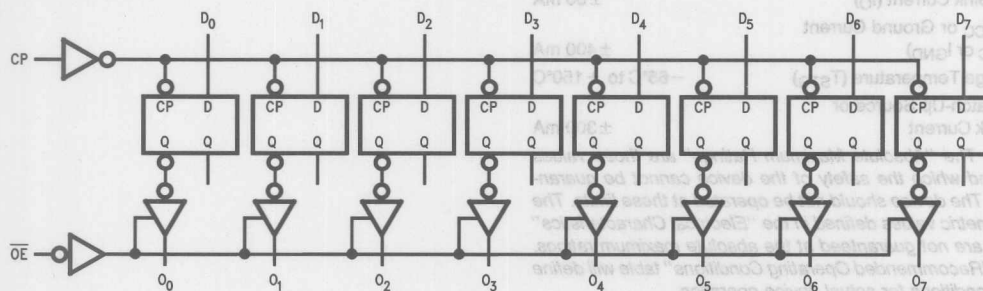
The LVQ374 consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ( $\overline{OE}$ ) LOW, the contents of the eight flip-flops are available at the outputs. When the  $\overline{OE}$  is HIGH, the outputs go to the high impedance state. Operation of the  $\overline{OE}$  input does not affect the state of the flip-flops.

## Truth Table

Inputs		$\overline{OE}$	Outputs
$D_n$	CP		$O_n$
H	—	L	H
L	—	L	L
X	X	H	Z

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 Z = High Impedance  
 — = LOW-to-HIGH Transition

## Logic Diagram



TL/F/11360-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = +25°C		Units	Conditions
			T <sub>A</sub> = -40°C to +85°C			
			Guaranteed Limits			
V <sub>IH</sub>	Minimum High Level Input Voltage	3.0	1.8	2.0	V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V
V <sub>IL</sub>	Maximum Low Level Input Voltage	3.0	1.2	0.8	V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V
V <sub>OH</sub>	Minimum High Level Output Voltage	3.0	2.88	2.9	V	I <sub>OUT</sub> = -80 μA
		3.0	2.88	2.98	V	V <sub>IH</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OH</sub> = -12 mA
V <sub>OL</sub>	Maximum Low Level Output Voltage	3.0	0.005	0.1	V	I <sub>OUT</sub> = 80 μA
		3.0	0.38	0.44	V	V <sub>IH</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OL</sub> = 12 mA
I <sub>IN</sub>	Maximum Input Leakage Current	3.8	±0.1	±1.0	μA	V <sub>I</sub> = V <sub>CC</sub> or GND

\*All outputs loaded; thresholds on input associated with output under test.

**Absolute Maximum Ratings** (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Input Diode Current ( $I_{IK}$ )	
$V_I = -0.5V$	-20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage ( $V_I$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Diode Current ( $I_{OK}$ )	
$V_O = -0.5V$	-20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage ( $V_O$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Source or Sink Current ( $I_O$ )	$\pm 50$ mA
DC $V_{CC}$ or Ground Current ( $I_{CC}$ or $I_{GND}$ )	$\pm 400$ mA
Storage Temperature ( $T_{STG}$ )	-65°C to +150°C
DC Latch-Up Source or Sink Current	$\pm 300$ mA

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**DC Electrical Characteristics**

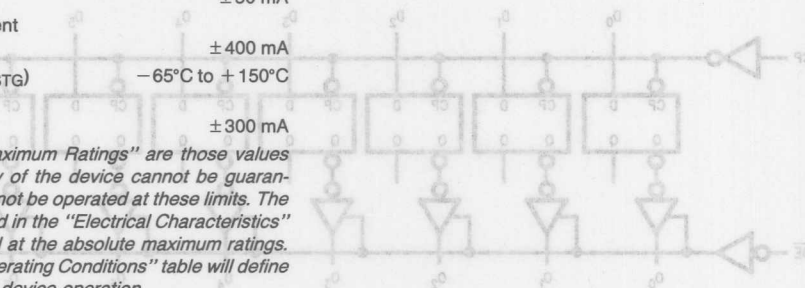
Symbol	Parameter	V <sub>CC</sub> (V)	74LVQ374		74LVQ374	Units	Conditions
			T <sub>A</sub> = +25°C		T <sub>A</sub> = −40°C to +85°C		
			Typ	Guaranteed Limits			
V <sub>IH</sub>	Minimum High Level Input Voltage	3.0	1.5	2.0	2.0	V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> − 0.1V
V <sub>IL</sub>	Maximum Low Level Input Voltage	3.0	1.5	0.8	0.8	V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> − 0.1V
V <sub>OH</sub>	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I <sub>OUT</sub> = −50 μA
		3.0		2.58	2.48	V	*V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OH</sub> = −12 mA
V <sub>OL</sub>	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I <sub>OUT</sub> = 50 μA
		3.0		0.36	0.44	V	*V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OL</sub> = 12 mA
I <sub>IN</sub>	Maximum Input Leakage Current	3.6		±0.1	±1.0	μA	V <sub>I</sub> = V <sub>CC</sub> , GND

\*All outputs loaded; thresholds on input associated with output under test.

**Recommended Operating Conditions**

Supply Voltage ( $V_{CC}$ )	2.0V to 3.6V
LVQ	
Input Voltage ( $V_I$ )	0V to $V_{CC}$
Output Voltage ( $V_O$ )	0V to $V_{CC}$
Operating Temperature ( $T_A$ )	-40°C to +85°C
74LVQ	
Minimum Input Edge Rate ( $\Delta V/\Delta t$ )	$V_{IN}$ from 0.8V to 2.0V
$V_{CC}$ @ 3.0V	125 mV/ns

Logic Diagram



# DC Electrical Characteristics (Continued)

Symbol	Parameter	V <sub>CC</sub> (V)	74LVQ374		74LVQ374		Units	Conditions
			T <sub>A</sub> = +25°C		T <sub>A</sub> = −40°C to +85°C			
			Typ	Guaranteed Limits				
I <sub>OLD</sub>	†Minimum Dynamic Output Current	3.6			36		mA	V <sub>OLD</sub> = 0.8V Max (Note 1)
I <sub>OHD</sub>		3.6			−25		mA	V <sub>OHD</sub> = 2.0V Min (Note 1)
I <sub>CC</sub>	Maximum Quiescent Supply Current	3.6		4.0	40.0		μA	V <sub>IN</sub> = V <sub>CC</sub> or GND
I <sub>OZ</sub>	Maximum TRI-STATE Leakage Current	3.6		±0.25	±2.5		μA	V <sub>I</sub> (OE) = V <sub>IL</sub> , V <sub>IH</sub> V <sub>I</sub> = V <sub>CC</sub> , GND V <sub>O</sub> = V <sub>CC</sub> , GND
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	3.3	0.5	0.8			V	(Notes 2, 3)
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	3.3	−0.3	−0.8			V	(Notes 2, 3)
V <sub>IHD</sub>	Maximum High Level Dynamic Input Voltage	3.3	1.7	2.0			V	(Notes 2, 4)
V <sub>ILD</sub>	Maximum Low Level Dynamic Input Voltage	3.3	1.6	0.8			V	(Notes 2, 4)

†Maximum test duration 2.0 ms, one output loaded at a time.

**Note 1:** Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed for 74LVQ.

**Note 2:** Worst case package.

**Note 3:** Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V; one output at GND.

**Note 4:** Max number of Data Inputs (n) switching. (n − 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V<sub>ILD</sub>), 0V to threshold (V<sub>IHD</sub>), f = 1 MHz.

## AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	74LVQ374			74LVQ374		Units
			T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF			T <sub>A</sub> = −40°C to +85°C C <sub>L</sub> = 50 pF		
			Min	Typ	Max	Min	Max	
f <sub>max</sub>	Maximum Clock Frequency	2.7 3.3 ± 0.3	55 75			50 70		MHz
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay CP to O <sub>n</sub>	2.7 3.3 ± 0.3	3.0 3.0	11.4 9.5	18.3 13.0	3.0 3.0	19.0 13.5	ns
t <sub>PZL</sub> , t <sub>PZH</sub>	Output Enable Time	2.7 3.3 ± 0.3	3.0 3.0	11.4 9.5	18.3 13.0	3.0 3.0	19.0 13.5	ns
t <sub>PHZ</sub> , t <sub>PLZ</sub>	Output Disable Time	2.7 3.3 ± 0.3	1.0 1.0	11.4 9.5	20.4 14.5	1.0 1.0	21.0 15.0	ns
t <sub>OSHL</sub> , t <sub>OSLH</sub>	Output to Output Skew* CP to O <sub>n</sub>	2.7 3.3 ± 0.3		1.0 1.0	1.5 1.5		1.5 1.5	ns

\*Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t<sub>OSHL</sub>) or LOW to HIGH (t<sub>OSLH</sub>). Parameter guaranteed by design.

Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF		T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF		Units
			Typ	Guaranteed Minimum			
t <sub>S</sub>	Setup Time, HIGH or LOW	2.7	0	4.0	4.5	ns	
	D <sub>n</sub> to CP	3.3 ±0.3	0	3.0	3.0		
t <sub>H</sub>	Hold Time, HIGH or LOW	2.7	0	1.5	1.5	ns	
	D <sub>n</sub> to CP	3.3 ±0.3	0	1.5	1.5		
t <sub>W</sub>	CP Pulse Width, HIGH or LOW	2.7	2.4	5.0	6.0	ns	
		3.3 ±0.3	2.0	4.0	4.0		

## Capacitance

Symbol	Parameter	Typ	Units	Conditions
C <sub>IN</sub>	Input Capacitance	4.5	pF	V <sub>CC</sub> = Open
C <sub>PD</sub> (Note 1)	Power Dissipation Capacitance	39	pF	V <sub>CC</sub> = 3.3V

Note 1: C<sub>PD</sub> is measured at 10 MHz.

AC Electrical Characteristics: See Section 2 for Test Methodology							
Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF			T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF	
			Min	Typ	Max	Min	Max
			Units			Units	
f <sub>max</sub>	Maximum Clock Frequency	2.7	2.7	2.7	2.7	2.7	2.7
t <sub>PLH</sub>	Propagation Delay CP to Q <sub>n</sub>	2.7	2.7	2.7	2.7	2.7	2.7
t <sub>PLZ</sub>	Output Enable Time	2.7	2.7	2.7	2.7	2.7	2.7
t <sub>HLZ</sub>	Output Disable Time	2.7	2.7	2.7	2.7	2.7	2.7
t <sub>OSK</sub>	Output to Output Skew*	2.7	2.7	2.7	2.7	2.7	2.7



## 74LVQ573

# Low Voltage Octal Latch with TRI-STATE® Outputs

## General Description

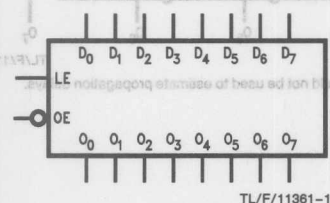
The LVQ573 is a high-speed octal latch with buffered common Latch Enable (LE) and buffered common Output Enable ( $\overline{OE}$ ) inputs. The LVQ573 is functionally identical to the LVQ373 but with inputs and outputs on opposite sides of the package.

## Features

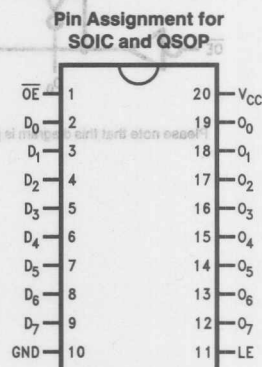
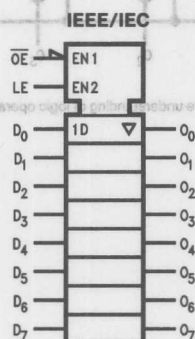
- Ideal for low power/low noise 3.3V applications
- Implements patented Quiet Series EMI reduction circuitry
- Available in SOIC JEDEC, SOIC EIAJ and QSOP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Improved latch-up immunity
- Guaranteed incident wave switching into 75 $\Omega$
- 4 kV minimum ESD immunity
- MIL-STD-883 54ACQ products are available for Military/Aerospace applications

**Ordering Code:** See Section 11

## Logic Symbols



## Connection Diagram



Pin Names	Description
D <sub>0</sub> -D <sub>7</sub>	Data Inputs
LE	Latch Enable Input
$\overline{OE}$	TRI-STATE Output Enable Input
O <sub>0</sub> -O <sub>7</sub>	TRI-STATE Latch Outputs

	SOIC JEDEC	SOIC EIAJ	SSOP JEDEC
Order Number	74LVQ573SC 74LVQ573SCX	74LVQ573SJ 74LVQ573SJX	74LVQ573QSC 74LVQ573QSCX
See NS Package Number	M20B	M20D	MQA20

## Functional Description

The LVQ573 contains eight D-type latches with TRI-STATE output buffers. When the Latch Enable (LE) input is HIGH, data on the  $D_n$  inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE buffers are controlled by the Output Enable ( $\overline{OE}$ ) input. When  $\overline{OE}$  is LOW, the buffers are enabled. When  $\overline{OE}$  is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches.

## Truth Table

Inputs			Outputs
$\overline{OE}$	LE	D	$O_n$
L	H	H	H
L	H	L	L
L	L	X	$O_0$
H	X	X	Z

H = HIGH Voltage

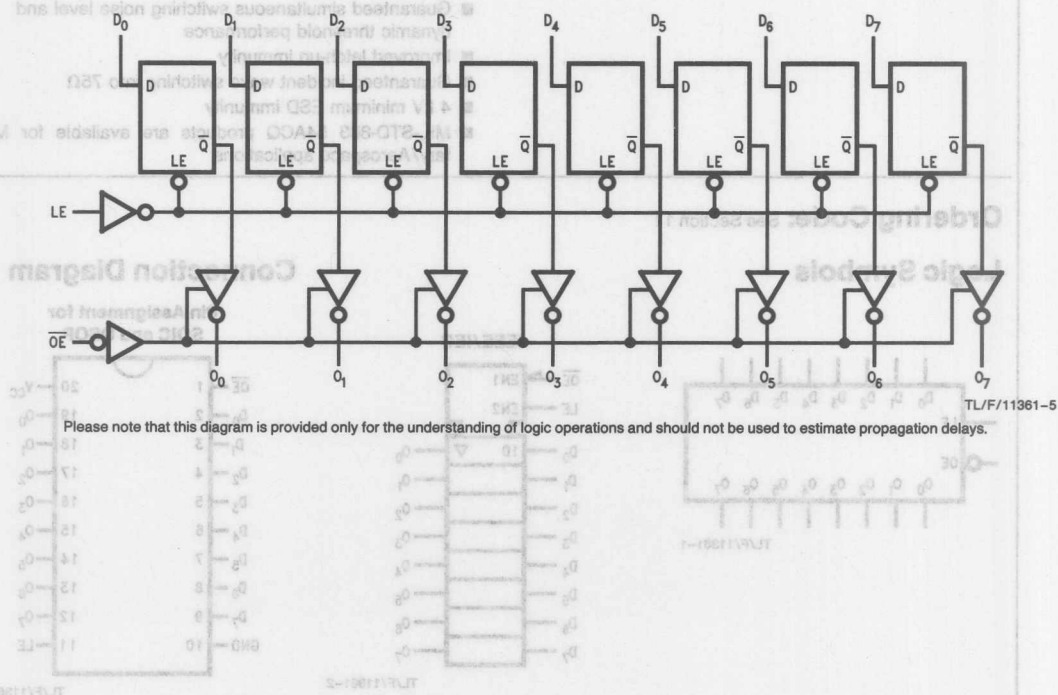
L = LOW Voltage

Z = High Impedance

X = Immaterial

$O_0$  = Previous  $O_0$  before HIGH-to-LOW transition of Latch Enable

## Logic Diagram



Pin Name	Description
$D_0-D_7$	Data Inputs
LE	Latch Enable Input
$\overline{OE}$	TRI-STATE Output Enable Input
$Q_0-Q_7$	TRI-STATE Latch Outputs

Order Number	SOIC JEDEC	SOIC EIA1	SSOP JEDEC
74LVQ573SC	74LVQ573SLX	74LVQ573SLX	74LVQ573SCX
See NS Package Number	MS08	MS08	MS08

please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Input Diode Current ( $I_{IK}$ )	-20 mA
$V_I = -0.5V$	-20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage ( $V_I$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Diode Current ( $I_{OK}$ )	-20 mA
$V_O = -0.5V$	-20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage ( $V_O$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Source or Sink Current ( $I_O$ )	$\pm 50$ mA
DC $V_{CC}$ or Ground Current ( $I_{CC}$ or $I_{GND}$ )	$\pm 400$ mA
Storage Temperature ( $T_{STG}$ )	-65°C to +150°C
DC Latch-Up Source or Sink Current	$\pm 300$ mA

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Supply Voltage ( $V_{CC}$ )	2.0V to 3.6V
LVQ	
Input Voltage ( $V_I$ )	0V to $V_{CC}$
Output Voltage ( $V_O$ )	0V to $V_{CC}$
Operating Temperature ( $T_A$ )	-40°C to +85°C
74LVQ	
Minimum Input Edge Rate ( $\Delta V/\Delta t$ )	
$V_{IN}$ from 0.8V to 2.0V	
$V_{CC}$ @ 3.0V	125 mV/ns

## DC Electrical Characteristics

Symbol	Parameter	V <sub>CC</sub> (V)	74LVQ573		74LVQ573		Units	Conditions
			T <sub>A</sub> = +25°C		T <sub>A</sub> = −40°C to +85°C			
			Typ	Guaranteed Limits				
V <sub>IH</sub>	Minimum High Level Input Voltage	3.0	1.5	2.0	2.0	V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> − 0.1V	
V <sub>IL</sub>	Maximum Low Level Input Voltage	3.0	1.5	0.8	0.8	V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> − 0.1V	
V <sub>OH</sub>	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I <sub>OUT</sub> = −50 μA	
		3.0		2.58	2.48	V	*V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OH</sub> = −12 mA	
V <sub>OL</sub>	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I <sub>OUT</sub> = 50 μA	
		3.0		0.36	0.44	V	*V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OL</sub> = 12 mA	
I <sub>IN</sub>	Maximum Input Leakage Current	3.6		±0.1	±1.0	μA	V <sub>I</sub> = V <sub>CC</sub> , GND	

\*All outputs loaded; thresholds on input associated with output under test.

Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = +25°C		T <sub>A</sub> = −40°C to +85°C		Units	Conditions
			Typ	Guaranteed Limits				
I <sub>OLD</sub>	†Minimum Dynamic Output Current	3.6			36		mA	V <sub>OLD</sub> = 0.8 V <sub>Max</sub> (Note 1)
I <sub>OHD</sub>		3.6			−25		mA	V <sub>OHD</sub> = 2.0V V <sub>Min</sub> (Note 1)
I <sub>CC</sub>	Maximum Quiescent Supply Current	3.6		4.0	40.0		μA	V <sub>IN</sub> = V <sub>CC</sub> or GND
I <sub>OZ</sub>	Maximum TRI-STATE Leakage Curent	3.6		±0.25	±2.5		μA	V <sub>I</sub> (OE) = V <sub>IL</sub> , V <sub>IH</sub> V <sub>I</sub> = V <sub>CC</sub> , GND V <sub>O</sub> = V <sub>CC</sub> , GND
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	3.3	0.4	0.8			V	(Notes 2, 3)
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	3.3	−0.4	−0.8			V	(Notes 2, 3)
V <sub>IHD</sub>	Maximum High Level Dynamic Input Voltage	3.3	1.6	2.0			V	(Notes 2, 4)
V <sub>ILD</sub>	Maximum Low Level Dynamic Input Voltage	3.3	1.6	0.8			V	(Notes 2, 4)

† Maximum test duration 2.0 ms, one output loaded at a time.

**Note 1:** Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed for 74LVQ.

**Note 2:** Worst case package.

**Note 3:** Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V; one output at GND.

**Note 4:** Max number of Data Inputs (n) switching. (n - 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V<sub>ILD</sub>), 0V to threshold (V<sub>IHD</sub>), f = 1 MHz.

## AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	74LVQ573			74LVQ573		Units
			T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF			T <sub>A</sub> = −40°C to +85°C C <sub>L</sub> = 50 pF		
			Min	Typ	Max	Min	Max	
t <sub>PHL</sub> , t <sub>PLH</sub>	Propagation Delay D <sub>n</sub> to O <sub>n</sub>	2.7 3.3 ± 0.3	2.5	10.2	14.8	2.5	16.0	ns
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay LE to O <sub>n</sub>	2.7 3.3 ± 0.3	2.5	10.2	16.9	2.5	18.0	
t <sub>PZL</sub> , t <sub>PZH</sub>	Output Enable Time	2.7 3.3 ± 0.3	2.5	10.2	18.3	2.5	19.0	ns
t <sub>PHZ</sub> , t <sub>PLZ</sub>	Output Disable Time	2.7 3.3 ± 0.3	1.0	10.8	20.4	1.0	21.0	
t <sub>OSHL</sub> , t <sub>OSLH</sub>	Output to Output Skew* D <sub>n</sub> to O <sub>n</sub>	2.7 3.3 ± 0.3		1.0	1.5		1.5	ns
				1.0	1.5		1.5	

\*Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t<sub>OSHL</sub>) or LOW to HIGH (t<sub>OSLH</sub>). Parameter guaranteed by design.

**AC Operating Requirements:** See Section 2 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	74LVQ573		74LVQ573	Units
			T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF		T <sub>A</sub> = −40°C to +85°C C <sub>L</sub> = 50 pF	
			Typ	Guaranteed Minimum		
t <sub>S</sub>	Setup Time, HIGH or LOW D <sub>n</sub> to LE	2.7 3.3 ± 0.3	0 0	4.0 3.0	4.5 3.0	ns
t <sub>H</sub>	Hold Time, HIGH or LOW D <sub>n</sub> to LE	2.7 3.3 ± 0.3	0 0	1.5 1.5	1.5 1.5	ns
t <sub>W</sub>	LE Pulse Width, HIGH	2.7 3.3 ± 0.3	2.4 2.0	5.0 4.0	6.0 4.0	ns

**Capacitance**

Symbol	Parameter	Typ	Units	Conditions
C <sub>IN</sub>	Input Capacitance	4.5	pF	V <sub>CC</sub> = Open
C <sub>PD</sub> (Note 1)	Power Dissipation Capacitance	37	pF	V <sub>CC</sub> = 3.3V

**Note 1:** C<sub>PD</sub> is measured at 10 MHz.

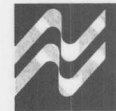
AC Operating Requirements: See Section 5 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	74V0573		Units
			Typ	Guaranteed Minimum	
t <sub>S</sub>	Setup Time, HIGH or LOW D <sub>n</sub> to LE	2.7 3.3 ± 0.3	0 0	4.0 3.0	ns
t <sub>H</sub>	Hold Time, HIGH or LOW D <sub>n</sub> to LE	2.7 3.3 ± 0.3	0 0	1.5 1.5	ns
t <sub>W</sub>	LE Pulse Width, HIGH	2.7 3.3 ± 0.3	2.4 2.0	2.0 4.0	ns

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C <sub>in</sub>	Input Capacitance	4.5	pf	V <sub>CC</sub> = Open
C <sub>PD</sub> (Note 1)	Power Dissipation Capacitance	37	pf	V <sub>CC</sub> = 3.3V

Note 1: C<sub>PD</sub> is measured at 10 MHz.



## Section 10 Contents

10-3	LVT Family Features
10-4	74LV125 3.3V ABT Quad Buffer with TRI-STATE Outputs
10-5	74LV124 3.3V ABT Octal Buffer/Line Driver with TRI-STATE Outputs
10-6	74LV124 3.3V ABT Octal Buffer/Line Driver with TRI-STATE Outputs
10-10	74LV124 3.3V ABT Octal Bidirectional Transceiver with TRI-STATE Inputs/Outputs
10-14	74LV123 3.3V ABT Octal Transparent Latch with TRI-STATE Outputs
10-16	74LV124 3.3V ABT Octal D Flip-Flop with TRI-STATE Outputs
10-18	74LV124 3.3V ABT Octal Transceiver/Register with TRI-STATE Outputs
10-20	74LV125 3.3V ABT Octal Transceiver/Register with TRI-STATE Outputs
10-23	74LV124 3.3V ABT 16-Bit Inverting Buffer/Line Driver with TRI-STATE Outputs
10-25	74LV124 3.3V ABT 16-Bit Inverting Buffer/Line Driver with TRI-STATE Outputs
10-27	74LV124 3.3V ABT 16-Bit Transceiver with TRI-STATE Outputs
10-29	74LV123 3.3V ABT 16-Bit Transparent Latch with TRI-STATE Outputs
10-31	74LV123 3.3V ABT 16-Bit D Flip-Flop with TRI-STATE Outputs
10-33	74LV124 3.3V ABT 16-Bit Transceiver/Register with TRI-STATE Outputs
10-36	74LV125 3.3V ABT 16-Bit Transceiver/Register with TRI-STATE Outputs

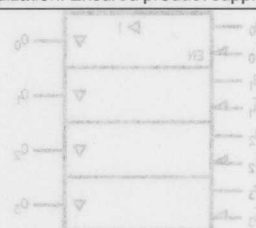
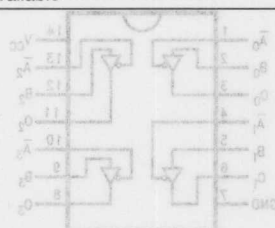
## Section 10 LVT Family

## Section 10 Contents

LVT Family Features .....	10-3
74LVT125 3.3V ABT Quad Buffer with TRI-STATE Outputs .....	10-4
74LVT240 3.3V ABT Octal Buffer/Line Driver with TRI-STATE Outputs .....	10-5
74LVT244 3.3V ABT Octal Buffer/Line Driver with TRI-STATE Outputs .....	10-6
74LVT245 3.3V ABT Octal Bidirectional Transceiver with TRI-STATE Inputs/Outputs .....	10-10
74LVT373 3.3V ABT Octal Transparent Latch with TRI-STATE Outputs .....	10-14
74LVT374 3.3V ABT Octal D Flip-Flop with TRI-STATE Outputs .....	10-16
74LVT646 3.3V ABT Octal Transceiver/Register with TRI-STATE Outputs .....	10-18
74LVT652 3.3V ABT Octal Transceiver/Register with TRI-STATE Outputs .....	10-20
74LVT16240 3.3V ABT 16-Bit Inverting Buffer/Line Driver with TRI-STATE Outputs .....	10-23
74LVT16244 3.3V ABT 16-Bit Buffer/Line Driver with TRI-STATE Outputs .....	10-25
74LVT16245 3.3V ABT 16-Bit Transceiver with TRI-STATE Outputs .....	10-27
74LVT16373 3.3V ABT 16-Bit Transparent Latch with TRI-STATE Outputs .....	10-29
74LVT16374 3.3V ABT 16-Bit D Flip-Flop with TRI-STATE Outputs .....	10-31
74LVT16646 3.3V ABT 16-Bit Transceiver/Register with TRI-STATE Outputs .....	10-33
74LVT16652 3.3V ABT 16-Bit Transceiver/Register with TRI-STATE Outputs .....	10-36

## LVT Family Low Voltage High Speed BiCMOS Logic

Features	Advantages
Extended $V_{CC}$ range from 2.7V to 3.6V, compatible with JEDEC Std. No. 8-1B	Fully characterized for unregulated battery operation
State-of-the-Art sub-micron BiCMOS process with special low voltage enhancements	3.3V logic family with equivalent performance of 5V ABT logic family; Propagation delays as fast as 4 ns
Mixed-Voltage circuitry	5V tolerant inputs and outputs provide direct interface with standard 5V buses and 5V devices
+ 64 mA / - 32 mA drive current	Drives large loads, buses, or memory arrays
Bus-hold circuitry	Eliminates external pullup or pulldown resistors on I/O pins that are being unused or floating
Power Up/Down TRI-STATE®	Guaranteed glitch-free bus interface during Power Up/Down cycle; Guaranteed Live (Hot) Insertion
SOIC, EIAJ-SOIC, and TSSOP packaging	Saves board space and weight; TSSOP compatible with PCMCIA standards
Alternate source available	Product standardization. Ensured product supply



Truth Table

Output	Inputs
$\bar{A}_n$	$A_n$
L	L
L	H
H	X

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = HIGH Impedance  
Z = Immaterial

Pin Name	Description
$\bar{A}_n$ , $B_n$	Inputs
$O_n$	TRI-STATE Outputs

Order Number	SOIC JEDEC	SOIC EIAJ	TSSOP
74VLT152M	74VLT152M	74VLT152M	74VLT152M
74VLT152MX	74VLT152MX	74VLT152MX	74VLT152MX
See NS Package Number	M14A	M14D	M14N



## 74LVT125

### 3.3V ABT Quad Buffer with TRI-STATE® Outputs

#### General Description

The LVT125 contains four independent non-inverting buffers with TRI-STATE outputs.

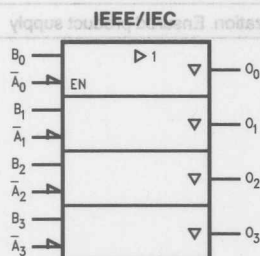
These buffers are designed for low-voltage (3.3V)  $V_{CC}$  applications, but with the capability to provide a TTL interface to a 5V environment. The LVT125 is fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

#### Features

- Input and output interface capability to systems at 5V  $V_{CC}$
- Bus-Hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink – 32 mA/ + 64 mA
- Available in SOIC JEDEC, SOIC EIAJ and TSSOP
- Functionally compatible with the 74 series 125
- Latch-up performance exceeds 500 mA

#### Ordering Code: See Section 11

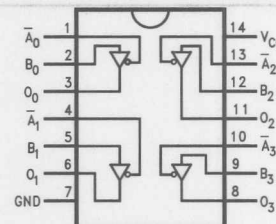
#### Logic Symbol



TL/F/12011-1

#### Connection Diagram

##### Pin Assignment for SOIC and TSSOP



TL/F/12011-2

#### Truth Table

Pin Names	Description
$\bar{A}_n, B_n$	Inputs
$O_n$	TRI-STATE Outputs

Inputs		Output
$A_n$	$B_n$	$O_n$
L	L	L
L	H	H
H	X	Z

H = HIGH Voltage Level  
L = LOW Voltage Level  
Z = HIGH Impedance  
X = Immaterial

	SOIC JEDEC	SOIC EIAJ	TSSOP
Order Number	74LVT125M 74LVT125MX	74LVT125SJ 74LVT125SJX	74LVT125MTCX
See NS Package Number	M14A	M14D	MTC14

# 74LVT240

## 3.3V ABT Octal Buffer/Line Driver with TRI-STATE® Outputs

### General Description

The LVT240 is an inverting octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter or receiver, which provides improved PC board density.

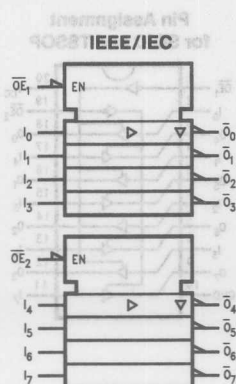
These octal buffers and line drivers are designed for low-voltage (3.3V)  $V_{CC}$  applications, but with the capability to provide a TTL interface to a 5V environment. The LVT240 is fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

### Features

- Input and output interface capability to systems at 5V  $V_{CC}$
- Bus-Hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink  $-32\text{ mA}/+64\text{ mA}$
- Available in SOIC JEDEC, SOIC EIAJ and TSSOP
- Functionally compatible with the 74 series 240
- Latch-up performance exceeds 500 mA

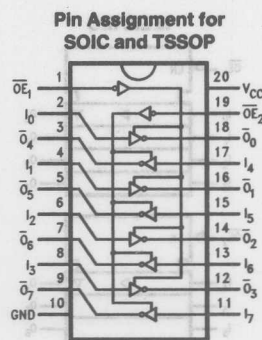
**Ordering Code:** See Section 11

### Logic Symbol



TL/F/12012-1

### Connection Diagram



TL/F/12012-2

### Truth Tables

Inputs		Outputs (Pins 12, 14, 16, 18)	
$\overline{OE}_1$	$I_n$		
L	L	L	H
L	H	L	L
H	X	X	Z

Inputs		Outputs (Pins 3, 5, 7, 9)	
$\overline{OE}_2$	$I_n$		
L	L	L	H
L	H	L	L
H	X	X	Z

H = HIGH Voltage Level L = LOW Voltage Level X = Immaterial Z = High Impedance

Pin Names	Description	SOIC JEDEC	SOIC EIAJ	TSSOP
$\overline{OE}_1, \overline{OE}_2$	TRI-STATE Output Enable Inputs	74LVT240WM	74LVT240SJ	74LVT240MTCX
$I_0-I_7$	Inputs	M20B	M20D	MTC20
$O_0-O_7$	TRI-STATE Outputs			

# 74LVT244

## 3.3V ABT Octal Buffer/Line Driver with TRI-STATE® Outputs

### General Description

The LVT244 is an octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter or receiver which provides improved PC board density.

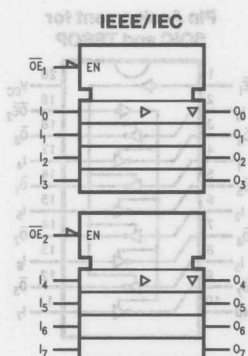
These octal buffers and line drivers are designed for low-voltage (3.3V)  $V_{CC}$  applications, but with the capability to provide a TTL interface to a 5V environment. The LVT244 is fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

### Features

- Input and output interface capability to systems at 5V  $V_{CC}$
- Bus-Hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink  $-32\text{ mA} / +64\text{ mA}$
- Available in SOIC JEDEC, SOIC EIAJ and TSSOP
- Functionally compatible with the 74 series 244
- Latch-up performance exceeds 500 mA

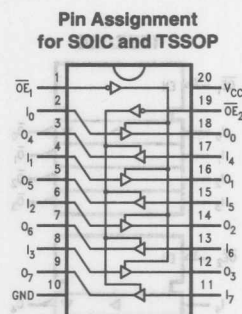
**Ordering Code:** See Section 11

### Logic Symbol



TL/F/12014-1

### Connection Diagram



TL/F/12014-2

### Truth Tables

Inputs		Outputs (Pins 12, 14, 16, 18)	
$\overline{OE}_1$	$I_n$		
L	L	L	L
L	H	H	H
H	X	Z	Z

H = HIGH Voltage Level

L = LOW Voltage Level

Inputs		Outputs (Pins 3, 5, 7, 9)	
$\overline{OE}_2$	$I_n$		
L	L	L	L
L	H	H	H
H	X	Z	Z

X = Immaterial

Z = High Impedance

Pin Names	Description	Order Number	SOIC JEDEC	SOIC EIAJ	TSSOP JEDEC
$\overline{OE}_1, \overline{OE}_2$	TRI-STATE Output Enable Inputs	74LVT244WM	74LVT244SJ	74LVT244SJJ	74LVT244MTCX
$I_0-I_7$	Inputs	See NS Package Number	M20B	M20D	MTC20
$O_0-O_7$	Outputs				

**Absolute Maximum Ratings** (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Input Voltage ( $V_I$ )	-0.5V to +7.0V
Output Voltage ( $V_O$ )	
Outputs Tri-stated	-0.5V to +7.0V
Outputs Active	-0.5V to $V_{CC}$
DC Output Current ( $I_O$ )	
Output in LOW State	128 mA
Output in HIGH State, $V_O > V_{CC}$	64 mA
DC Input Diode Current ( $I_{IK}$ ) $V_I < 0$	-50 mA
DC Output Diode Current ( $I_{OK}$ ) $V_O < 0$	-50 mA
Storage Temperature Range ( $T_{STG}$ )	-65°C to +150°C

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Recommended Operating Conditions**

Supply Voltage	2.7V to 3.6V
Operating	
Input Voltage ( $V_I$ )	0V to 5.5V
Output Voltage ( $V_O$ )	
Output in Active State	0V to $V_{CC}$
Output in "OFF" State	0V to 5.5V
Minimum Input Edge Rate ( $\Delta t/\Delta V$ )	
$V_{IN} = 0.8V - 2.0V$ , $V_{CC} = 3.0V$	10 ns/V
Free Air Operating Temperature ( $T_A$ )	-40°C to +85°C

**DC Electrical Characteristics**

Symbol	Parameter	$V_{CC}$ (V)	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$			Units	Conditions
			Min	Typ (Note 1)	Max		
$V_{IK}$	Input Clamp Diode Voltage	2.7			-1.2	V	$I_I = -18 \text{ mA}$
$V_{IH}$	Input HIGH Voltage	2.7-3.6	2.0			V	$V_O \leq 0.1V$ or $V_O \geq V_{CC} - 0.1V$
$V_{IL}$	Input LOW Voltage	2.7-3.6			0.8		
$V_{OH}$	Output HIGH Voltage	2.7-3.6	$V_{CC} - 0.2$			V	$I_{OH} = -100 \mu\text{A}$
		2.7	2.4			V	$I_{OH} = -8 \text{ mA}$
		3.0	2.0			V	$I_{OH} = -32 \text{ mA}$
$V_{OL}$	Output LOW Voltage	2.7			0.2	V	$I_{OL} = 100 \mu\text{A}$
		2.7			0.5	V	$I_{OL} = 24 \text{ mA}$
		3.0			0.4	V	$I_{OL} = 16 \text{ mA}$
		3.0			0.5	V	$I_{OL} = 32 \text{ mA}$
		3.0			0.55	V	$I_{OL} = 64 \text{ mA}$
$I_{I(HOLD)}$	Bus-Held Input Minimum Drive	3.0	75			$\mu\text{A}$	$V_I = 0.8V$
			-75			$\mu\text{A}$	$V_I = 2.0V$
$I_{I(OD)}$	Bus-Held Input Over-Drive Current to Change State	3.0	500			$\mu\text{A}$	(Note 2)
			-500			$\mu\text{A}$	(Note 3)
$I_I$	Input Current	0 or 3.6			10	$\mu\text{A}$	$V_I = 5.5V$
		Control Pins	3.6		$\pm 1$	$\mu\text{A}$	$V_I = 0V$ or $V_{CC}$
		Data Pins	3.6		-5	$\mu\text{A}$	$V_I = 0V$
					1	$\mu\text{A}$	$V_I = V_{CC}$
$I_{IH}^+$	Control Pin Input Current	3.6			10	$\mu\text{A}$	$V_{CC} \leq V_I \leq 5.5V$
$I_{OFF}$	Input or Output Current	0			$\pm 100$	$\mu\text{A}$	$0V \leq V_I$ or $V_O \leq 5.5V$
$I_{OZL}$	TRI-STATE Output Leakage Current	3.6			-5	$\mu\text{A}$	$V_O = 0V$

# DC Electrical Characteristics (Continued)

Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = -40°C to +85°C			Units	Conditions
			Min	Typ (Note 1)	Max		
I <sub>OZH</sub>	TRI-STATE Output Leakage Current	3.6		5		μA	V <sub>O</sub> = V <sub>CC</sub>
I <sub>OZH</sub> <sup>+</sup>	TRI-STATE Output Leakage Current	3.6		10		μA	V <sub>CC</sub> ≤ V <sub>O</sub> ≤ 5.5V
I <sub>CC</sub> H	Power Supply Current	3.6		0.19		mA	V <sub>I</sub> = GND or V <sub>CC</sub> , Outputs High
I <sub>CC</sub> L	Power Supply Current	3.6		12		mA	V <sub>I</sub> = GND or V <sub>CC</sub> , Outputs Low
I <sub>CC</sub> Z	Power Supply Current	3.6		0.19		mA	V <sub>I</sub> = GND or V <sub>CC</sub> , Outputs Disabled
I <sub>CCZH</sub> <sup>+</sup>	Power Supply Current	3.6		0.19		mA	V <sub>I</sub> = GND or V <sub>CC</sub> , V <sub>CC</sub> ≤ V <sub>O</sub> ≤ 5.5V, Outputs Disabled
ΔI <sub>CC</sub>	Increase in Power Supply Current (Note 4)	3.6		0.2		mA	One Input at V <sub>CC</sub> - 0.6V Other Inputs at V <sub>CC</sub> or GND

Note 1: All typical values are at V<sub>CC</sub> = 3.3V, T<sub>A</sub> = 25°C.

Note 2: An external driver must source at least the specified current to switch from LOW to HIGH.

Note 3: An external driver must sink at least the specified current to switch from HIGH to LOW.

Note 4: This is the increase in supply current for each input that is at the specified voltage level rather than V<sub>CC</sub> or GND.

## Dynamic Switching Characteristics: See Section 2 for Test Methodology (Note 1)

Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = 25°C			Units	Conditions C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500Ω
			Min	Typ	Max		
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	3.3		0.8		V	(Note 2)
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	3.3		-0.8		V	(Note 2)
V <sub>IHD</sub>	Minimum High Level Dynamic Input Voltage	3.3				V	(Note 3)
V <sub>ILD</sub>	Maximum Low Level Dynamic Input Voltage	3.3				V	(Note 3)

Note 1: Characterized in SOIC package. Guaranteed parameter, but not tested.

Note 2: Max number of outputs defined as (n). n - 1 data inputs are driven 0V to 3V. Output at LOW.

Note 3: Max number of data inputs (n) switching. n - 1 inputs switching 0V to 3V. Input-under-test switching: 3V to threshold (V<sub>ILD</sub>), 0V to threshold (V<sub>IHD</sub>).

## AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	$T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $C_L = 50\text{ pF, } R_L = 500\Omega$					Units
		$V_{CC} = 3.3\text{V} \pm 0.3\text{V}$			$V_{CC} = 2.7\text{V}$		
		Min	Typ (Note 1)	Max	Min	Max	
t <sub>PLH</sub>	Propagation Delay Data to Output	1.0		4.1	1.0	5.0	ns
t <sub>PHL</sub>		1.0		4.1	1.0	5.0	
t <sub>PZH</sub>	Output Enable Time	1.0		5.2	1.0	6.3	ns
t <sub>PZL</sub>		1.0		5.2	1.0	6.3	
t <sub>PHZ</sub>	Output Disable Time	1.8		5.1	1.8	5.6	ns
t <sub>PLZ</sub>		1.8		5.1	1.8	5.6	
t <sub>OSHL</sub>	Output to Output Skew			1.0			ns
t <sub>OSLH</sub>	(Note 2)						

Note 1: All typical values are at V<sub>CC</sub> = 3.3V, T<sub>A</sub> = 25°C.

Note 2: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t<sub>OSHL</sub>) or LOW to HIGH (t<sub>OSLH</sub>). Parameter guaranteed by design.

## Capacitance (Note 1)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
$C_{IN}$	Input Capacitance		4		pF	$V_{CC} = 0V, V_I = 0V$ or $V_{CC}$
$C_{OUT}$	Output Capacitance		8		pF	$V_{CC} = 3.0V, V_O = 0V$ or $V_{CC}$

Note 1: Capacitance is measured at frequency  $f = 1$  MHz, per MIL-STD-883B, Method 3012.

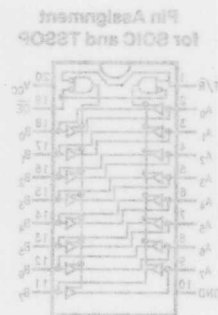
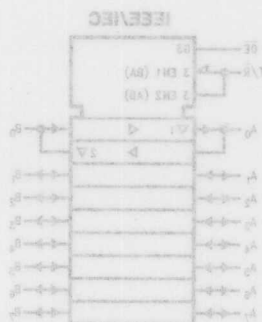
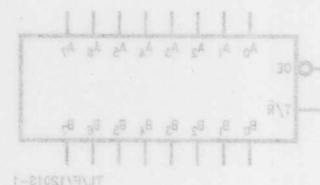
## General Description

The LVT244 contains eight non-inverting bidirectional buffers with TRI-STATE outputs and is intended for bus-oriented applications. Current sinking capability is 64 mA at both the A and B ports. The Transceiver/Receiver (T/R) input determines the direction of data flow through the bidirectional transceiver. Transmitt (active-HIGH) enables data from A ports to B ports; Receive (active-LOW) enables data from B ports to A ports. The Output Enable input, when HIGH, disables both A and B ports by placing them in a HIGH-Z condition.

These transceivers are designed for low-voltage (3.3V) VCC applications, but with the capability to provide a TTL interface to a 5V environment. The LVT244 is fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

## Logic Symbols

Ordering Code: See Section 11



## Truth Table

Outputs	Inputs		Description	Pin Names
	T/R	OE		
Bus B Data to Bus A	L	L	Output Enable Input	OE
Bus A Data to Bus B	H	L	Transceiver/Receiver Input	T/R
HIGH-Z State	X	H	Side A Inputs or TRI-STATE Outputs	A0-A7
			Side B Inputs or TRI-STATE Outputs	B0-B7

H = HIGH Voltage Level, L = LOW Voltage Level, X = Indeterminate

Order Number	SOIC JEDEC	SOIC EIAJ	TSSOP JEDEC
74LVT244WMX	74LVT244SM	74LVT244SJ	74LVT244J
74LVT244WMX	74LVT244SM	74LVT244SJ	74LVT244J
74LVT244WMX	74LVT244SM	74LVT244SJ	74LVT244J

# 74LVT245

## 3.3V ABT Octal Bidirectional Transceiver with TRI-STATE® Inputs/Outputs

### General Description

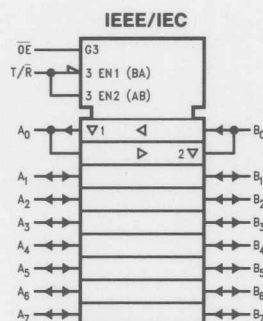
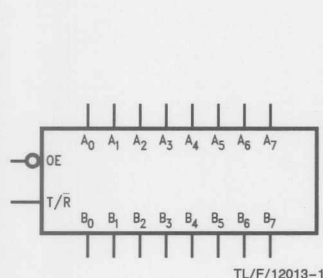
The LVT245 contains eight non-inverting bidirectional buffers with TRI-STATE outputs and is intended for bus-oriented applications. Current sinking capability is 64 mA at both the A and B ports. The Transmit/Receive (T/R) input determines the direction of data flow through the bidirectional transceiver. Transmit (active-HIGH) enables data from A ports to B ports; Receive (active-LOW) enables data from B ports to A ports. The Output Enable input, when HIGH, disables both A and B ports by placing them in a HIGH Z condition.

These transceivers are designed for low-voltage (3.3V) V<sub>CC</sub> applications, but with the capability to provide a TTL interface to a 5V environment. The LVT245 is fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

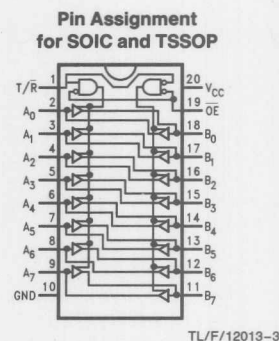
### Features

- Input and output interface capability to systems at 5V V<sub>CC</sub>
- Bus-Hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink -32 mA/+64 mA
- Available in SOIC JEDEC, SOIC EIAJ and TSSOP
- Functionally compatible with the 74 series 245
- Latch-up performance exceeds 500 mA

### Ordering Code: See Section 11 Logic Symbols



### Connection Diagram



### Truth Table

Pin Names	Description
OE	Output Enable Input
T/R	Transmit/Receive Input
A <sub>0</sub> -A <sub>7</sub>	Side A Inputs or TRI-STATE Outputs
B <sub>0</sub> -B <sub>7</sub>	Side B Inputs or TRI-STATE Outputs

Inputs		Outputs
OE	T/R	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	HIGH-Z State

H = HIGH Voltage Level L = LOW Voltage Level X = Immaterial

	SOIC JEDEC	SOIC EIAJ	TSSOP JEDEC
Order Number	74LVT245WM 74LVT245WMX	74LVT245SJ 74LVT245SJX	74LVT245MTCX
See NS Package Number	M20B	M20D	MTC20

**Absolute Maximum Ratings** (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Input Voltage ( $V_I$ )	-0.5V to +7.0V
Output Voltage ( $V_O$ )	
Outputs in TRI-STATE	-0.5V to +7.0V
Outputs Active	-0.5V to $V_{CC}$
DC Output Current ( $I_O$ )	
Output in LOW State	128 mA
Output in HIGH State, $V_O > V_{CC}$	64 mA
DC Input Diode Current ( $I_{IK}$ ) $V_I < 0$	-50 mA
DC Output Diode Current ( $I_{OK}$ ) $V_O < 0$	-50 mA
Storage Temperature ( $T_{STG}$ )	-65°C to +150°C

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Recommended Operating Conditions**

Supply Voltage	2.7V to 3.6V
Operating	
Input Voltage ( $V_I$ )	0V to 5.5V
Output Voltage ( $V_O$ )	
Output in Active State	0V to $V_{CC}$
Output in "OFF" State	0V to 5.5V
Minimum Input Edge Rate ( $\Delta t/\Delta V$ )	10 ns/V
$V_{IN} = 0.8V - 2.0V, V_{CC} = 3.0V$	
Free Air Operating Temperature ( $T_A$ )	-40°C to +85°C

**DC Electrical Characteristics**

Symbol	Parameter	$V_{CC}$ (V)	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		Units	Conditions
			Min	Typ (Note 1)		
$V_{IK}$	Input Clamp Diode Voltage	2.7		-1.2	V	$I_I = -18 \text{ mA}$
$V_{IH}$	Input HIGH Voltage	2.7-3.6	2.0		V	$V_O \leq 0.1V$ or $V_O \geq V_{CC} - 0.1V$
$V_{IL}$	Input LOW Voltage	2.7-3.6		0.8	V	
$V_{OH}$	Output HIGH Voltage	2.7-3.6	$V_{CC} - 0.2$		V	$I_{OH} = -100 \mu\text{A}$
		2.7	2.4		V	$I_{OH} = -8 \text{ mA}$
		3.0	2.0		V	$I_{OH} = -32 \text{ mA}$
					V	
$V_{OL}$	Output LOW Voltage	2.7		0.2	V	$I_{OL} = 100 \mu\text{A}$
		2.7		0.5	V	$I_{OL} = 24 \text{ mA}$
		3.0		0.4	V	$I_{OL} = 16 \text{ mA}$
		3.0		0.5	V	$I_{OL} = 32 \text{ mA}$
		3.0		0.55	V	$I_{OL} = 64 \text{ mA}$
$I_{I(HOLD)}$	Bus-Held Input Minimum Drive	3.0	75		$\mu\text{A}$	$V_I = 0.8V$
			-75		$\mu\text{A}$	$V_I = 2.0V$
$I_{I(OD)}$	Bus-Held Input Over-Drive Current to Change State	3.0	500		$\mu\text{A}$	(Note 2)
			-500		$\mu\text{A}$	(Note 3)
$I_I$	Input Current	0 or 3.6		10	$\mu\text{A}$	$V_I = 5.5V$
	Control Pins	3.6		$\pm 1$	$\mu\text{A}$	$V_I = 0V$ or $V_{CC}$
	Data Pins	3.6		-5	$\mu\text{A}$	$V_I = 0V$
$I_{IH}^+$	Control Pin Input Current	3.6		1	$\mu\text{A}$	$V_I = V_{CC}$
$I_{OFF}$	Input or Output Current	0		$\pm 100$	$\mu\text{A}$	$V_{CC} \leq V_I \leq 5.5V$ $0V \leq (V_I \text{ or } V_O) \leq 5.5V$

**DC Electrical Characteristics** (Continued)

Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = -40°C to +85°C			Units	Conditions
			Min	Typ (Note 1)	Max		
I <sub>OZL</sub>	TRI-STATE Output Leakage Current	3.6			-1	μA	V <sub>O</sub> = 0V
I <sub>OZH</sub>	TRI-STATE Output Leakage Current	3.6			1	μA	V <sub>O</sub> = V <sub>CC</sub>
I <sub>OZH</sub> <sup>+</sup>	TRI-STATE Output Leakage Current	3.6			10	μA	V <sub>CC</sub> ≤ V <sub>O</sub> ≤ 5.5V
I <sub>CCH</sub>	Power Supply Current	3.6			0.19	mA	V <sub>I</sub> = GND or V <sub>CC</sub> , Outputs High
I <sub>CCL</sub>	Power Supply Current	3.6			12	mA	V <sub>I</sub> = GND or V <sub>CC</sub> , Outputs Low
I <sub>CCZ</sub>	Power Supply Current	3.6			0.19	mA	V <sub>I</sub> = GND or V <sub>CC</sub> , Outputs Disabled
I <sub>CCZH</sub> <sup>+</sup>	Power Supply Current	3.6			0.19	mA	V <sub>I</sub> = GND or V <sub>CC</sub> , V <sub>CC</sub> ≤ V <sub>O</sub> ≤ 5.5V, Outputs Disabled
ΔI <sub>CC</sub>	Increase in Power Supply Current (Note 4)	3.6			0.2	mA	One Input at V <sub>CC</sub> = 0.6V Other Inputs at V <sub>CC</sub> or GND

**Note 1:** All typical values are at V<sub>CC</sub> = 3.3V, T<sub>A</sub> = 25°C.

**Note 2:** An external driver must source at least the specified current to switch from LOW to HIGH.

**Note 3:** An external driver must sink at least the specified current to switch from HIGH to LOW.

**Note 4:** This is the increase in supply current for each input that is at the specified voltage level rather than V<sub>CC</sub> or GND.

**Dynamic Switching Characteristics** : See Section 2 for Test Methodology

Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = 25°C			Units	Conditions C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500Ω
			Min	Typ	Max		
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	3.3		0.8		V	(Note 2)
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	3.3		-0.8		V	(Note 2)
V <sub>IHD</sub>	Minimum High Level Dynamic Input Voltage	3.3				V	(Note 3)
V <sub>ILD</sub>	Maximum Low Level Dynamic Input Voltage	3.3				V	(Note 3)

**Note 1:** Characterized in SOIC package. Guaranteed parameter, but not tested.

**Note 2:** Max number of outputs defined as (n). n-1 data inputs are driven 0V to 3V. Output at LOW.

**Note 3:** Max number of data inputs (n) switching. n-1 inputs switching 0V to 3V. Input-under-test switching: 3V to threshold (V<sub>ILD</sub>), 0V to threshold (V<sub>IHD</sub>).

**AC Electrical Characteristics:** See Section 2 for Test Methodology

Symbol	Parameter	T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500Ω					Units
		V <sub>CC</sub> = 3.3V ±0.3V			V <sub>CC</sub> = 2.7V		
		Min	Typ (Note 1)	Max	Min	Max	
t <sub>PLH</sub>	Propagation Delay Data to Output	1.0		4.0	1.0	4.7	ns
t <sub>PHL</sub>		1.0		4.0	1.0	4.6	
t <sub>PZH</sub>	Output Enable Time	1.1		5.5	1.1	7.1	ns
t <sub>PZL</sub>		1.5		5.5	1.5	6.5	
t <sub>PHZ</sub>	Output Disable Time	2.2		5.9	2.2	6.5	ns
t <sub>PLZ</sub>		2.0		4.8	2.0	4.8	
t <sub>OSHL</sub>	Output to Output Skew (Note 2)			1.0			ns
t <sub>OSLH</sub>							

**Note 1:** All typical values are at V<sub>CC</sub> = 3.3V, T<sub>A</sub> = 25°C.

**Note 2:** Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t<sub>OSHL</sub>) or LOW to HIGH (t<sub>OSLH</sub>). Parameter guaranteed by design.

**Capacitance** (Note 1)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
C <sub>IN</sub>	Input Capacitance		4		pF	V <sub>CC</sub> = 0V, V <sub>I</sub> = 0V or V <sub>CC</sub>
C <sub>I/O</sub>	I/O Capacitance		8		pF	V <sub>CC</sub> = 3V, V <sub>I/O</sub> = 0V or V <sub>CC</sub>

**Note 1:** Capacitance is measured at frequency  $f = 1$  MHz, per MIL-STD-883B, Method 3012.

## 74LVT373

3.3V ABT Octal Transparent Latch  
with TRI-STATE® Outputs

## General Description

The LVT373 consists of eight latches with TRI-STATE outputs for bus organized system applications. The latches appear transparent to the data when Latch Enable (LE) is HIGH. When LE is low, the data satisfying the input timing requirements is latched. Data appears on the bus when the Output Enable (OE) is LOW. When OE is HIGH, the bus output is in the high impedance state.

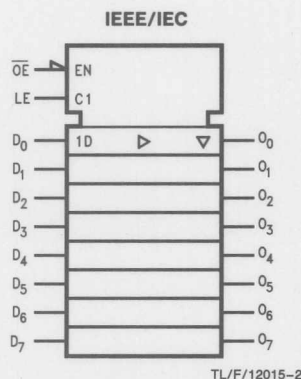
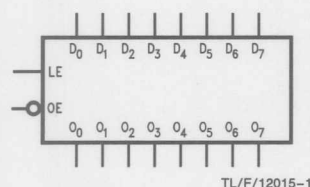
These octal latches are designed for low-voltage (3.3V)  $V_{CC}$  applications, but with the capability to provide a TTL interface to a 5V environment. The LVT373 is fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

## Features

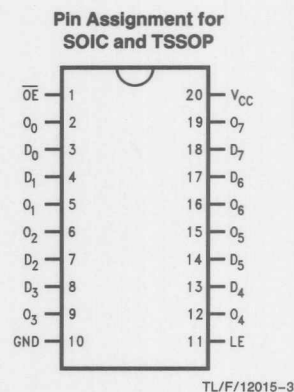
- Input and output interface capability to systems at 5V  $V_{CC}$
- Bus-Hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink  $-32\text{ mA}/+64\text{ mA}$
- Available in SOIC JEDEC, SOIC EIAJ and TSSOP
- Functionally compatible with the 74 series 373
- Latch-up performance exceeds 500 mA

**Ordering Code:** See Section 11

## Logic Symbols



## Connection Diagram



Pin Names	Description
$D_0-D_7$	Data Inputs
LE	Latch Enable Input
$\overline{OE}$	Output Enable Input
$O_0-O_7$	TRI-STATE Latch Outputs

	SOIC JEDEC	SOIC EIAJ	TSSOP JEDEC
Order Number	74LVT373WM 74LVT373WMX	74LVT373SJ 74LVT373SJX	74LVT373MTCX
See NS Package Number	M20B	M20D	MTC20

The LV7374 contains eight D-type latches with TRI-STATE standard outputs. When the Latch Enable (LE) input is HIGH, data on the  $D_n$  inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE standard outputs are controlled by the Output Enable ( $\overline{OE}$ ) input. When  $\overline{OE}$  is LOW, the standard outputs are in the 2-state mode. When  $\overline{OE}$  is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

Inputs			Outputs
LE	$\overline{OE}$	$D_n$	$O_n$
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	$O_0$

H = HIGH Voltage Level

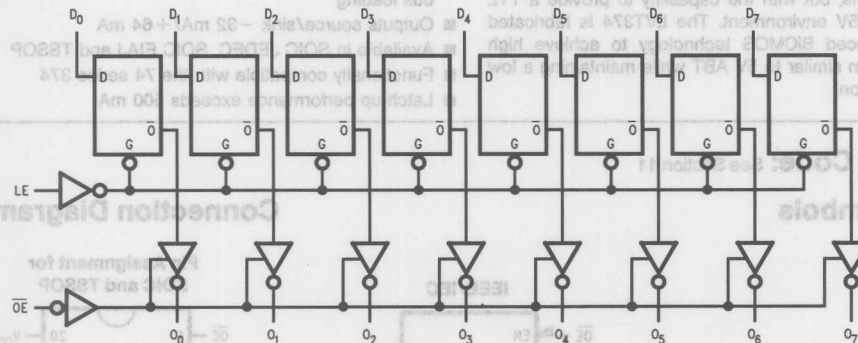
L = LOW Voltage Level

Z = High Impedance

X = Immaterial

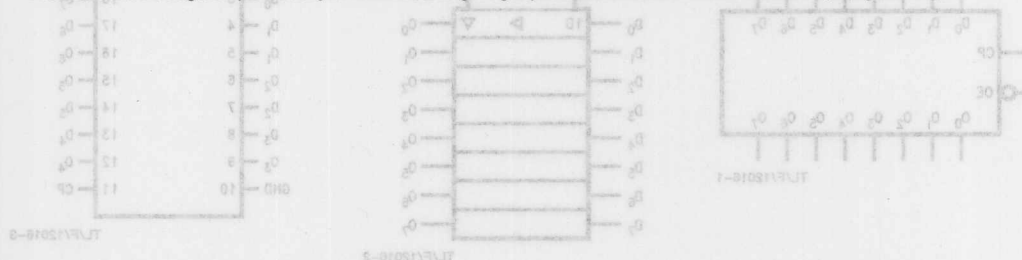
$O_0$  = Previous  $O_0$  before HIGH to LOW transition of Latch Enable

## Logic Diagram



TL/F/12015-4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.



Pin Number	Description
$D_0$ - $D_7$	Data Inputs
$\overline{CP}$	Clock Pulse Input
$\overline{OE}$	TRI-STATE Output Enable Input
$O_0$ - $O_7$	TRI-STATE Outputs

Order Number	SOIC JEDEC	SOIC EIAJ	TSOP JEDEC
74LV7374WMX	74LV7374WJ	74LV7374WJ	74LV7374WJ
74LV7374MTCX	74LV7374MT	74LV7374MT	74LV7374MT
See NS Package Number	MS08	MS08	MS08



## 74LVT374

### 3.3V ABT Octal D Flip-Flop with TRI-STATE® Outputs

#### General Description

The LVT374 is a high-speed, low-power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and TRI-STATE outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable ( $\overline{OE}$ ) are common to all flip-flops.

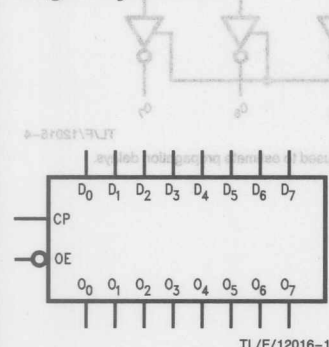
These octal flip-flops are designed for low-voltage (3.3V)  $V_{CC}$  applications, but with the capability to provide a TTL interface to a 5V environment. The LVT374 is fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

#### Features

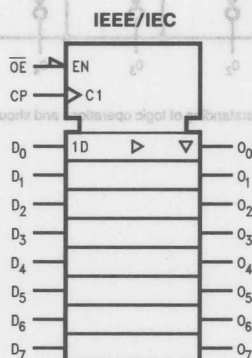
- Input and output interface capability to systems at 5V  $V_{CC}$
- Bus-Hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink  $-32\text{ mA}/+64\text{ mA}$
- Available in SOIC JEDEC, SOIC EIAJ and TSSOP
- Functionally compatible with the 74 series 374
- Latch-up performance exceeds 500 mA

**Ordering Code:** See Section 11

#### Logic Symbols

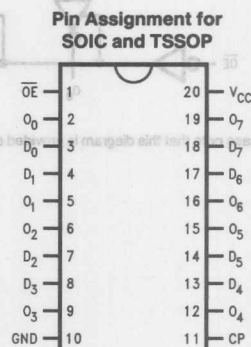


TL/F/12016-1



TL/F/12016-2

#### Connection Diagram



TL/F/12016-3



Pin Names	Description
$D_0$ – $D_7$	Data Inputs
CP	Clock Pulse Input
$\overline{OE}$	TRI-STATE Output Enable Input
$Q_0$ – $Q_7$	TRI-STATE Outputs

	SOIC JEDEC	SOIC EIAJ	TSSOP JEDEC
Order Number	74LVT374WM 74LVT374WMX	74LVT374SJ 74LVT374SJX	74LVT374MTCX
See NS Package Number	M20B	M20D	MTC20

## Functional Description

The LVT374 consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ( $\overline{OE}$ ) LOW, the contents of the eight flip-flops are available at the outputs. When the  $\overline{OE}$  is HIGH, the outputs go to the high impedance state. Operation of the  $\overline{OE}$  input does not affect the state of the flip-flops.

## Truth Table


Inputs			Outputs
$D_n$	CP	$\overline{OE}$	$O_n$
H		L	H
L		L	L
X	L	L	$O_o$
X	X	H	Z

H = HIGH Voltage Level

L = LOW Voltage Level

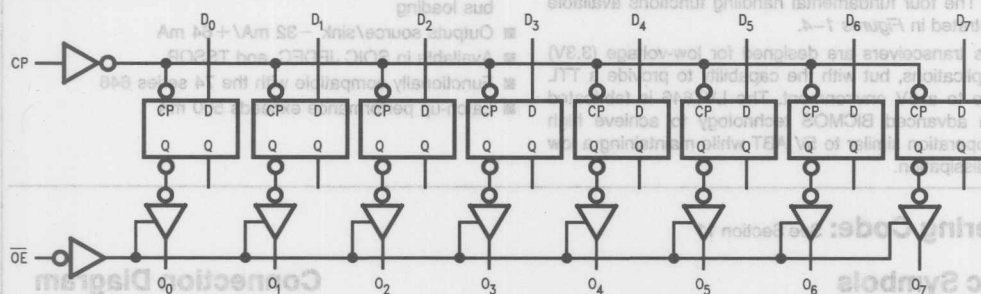
X = Immaterial

Z = High Impedance

 = LOW-to-HIGH Transition

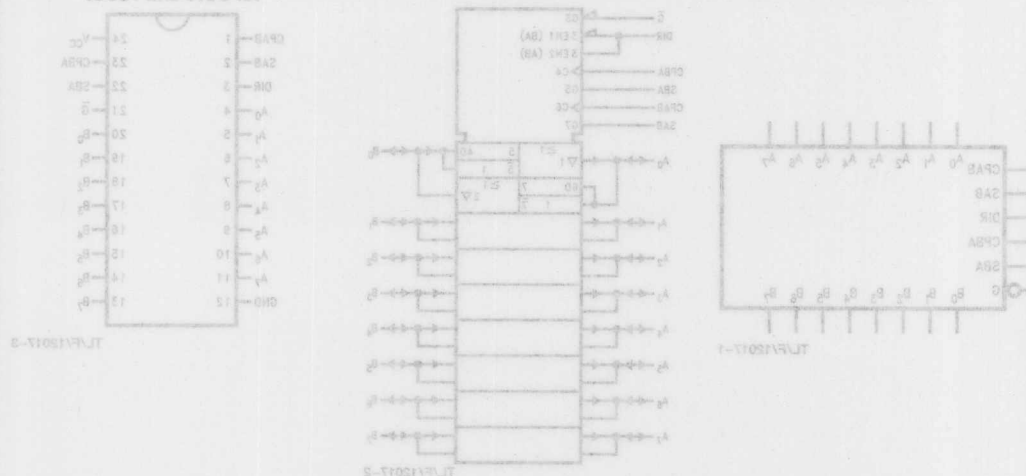
$O_o$  = Previous  $O_o$  before HIGH to LOW of CP

## Logic Diagram



TL/F/12016-4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.



Order Number	Package Number	See NS
74LVT374WMX	M24B	
74LVT374MTX	M20C4	

Pin Name	Description
A0-A7	Data Register A Inputs
A0-A7	Data Register A Outputs
B0-B7	Data Register B Inputs
B0-B7	Data Register B Outputs
CPAB, CPBA	Clock Pulse Inputs
SAB, SBA	Transceiver Inputs
$\overline{OE}$	Output Enable Input
DIR	Direction Control Input

# 74LVT646

## 3.3V ABT Octal Transceiver/Register

### with TRI-STATE® Outputs

#### General Description

The LVT646 consist of registered bus transceiver circuits, with outputs, D-type flip-flops, and control circuitry providing multiplexed transmission of data directly from the input bus or from the internal storage registers. Data on the A or B bus will be loaded into the respective registers on the LOW-to-HIGH transition of the appropriate clock pin (CPAB or CPBA). The four fundamental handling functions available are illustrated in *Figures 1-4*.

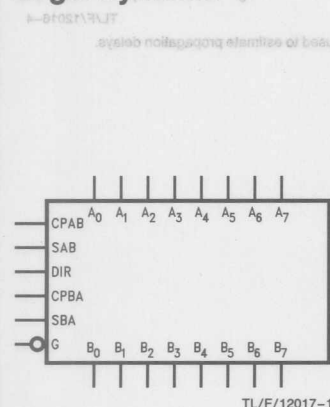
The bus transceivers are designed for low-voltage (3.3V)  $V_{CC}$  applications, but with the capability to provide a TTL interface to a 5V environment. The LVT646 is fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

#### Features

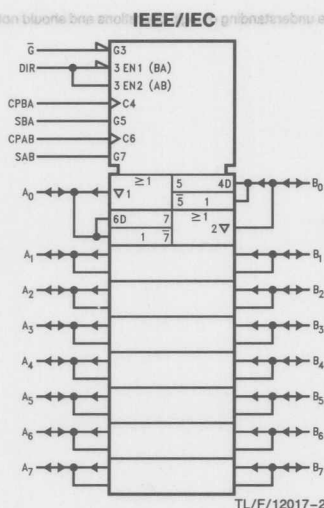
- Input and output interface capability to systems at 5V  $V_{CC}$
- Bus-Hold data inputs eliminate the need for external pull-up resistors to hold unused input
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink  $-32\text{ mA}/+64\text{ mA}$
- Available in SOIC JEDEC, and TSSOP
- Functionally compatible with the 74 series 646
- Latch-up performance exceeds 500 mA

**Ordering Code:** See Section 11

#### Logic Symbols

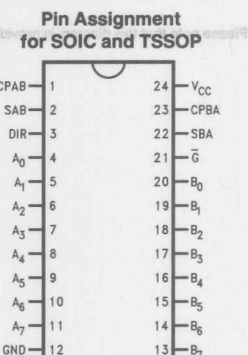


TL/F/12017-1



TL/F/12017-2

#### Connection Diagram

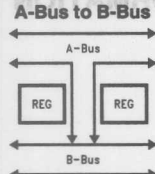


TL/F/12017-3

Pin Names	Description
A0-A7	Data Register A Inputs
	Data Register A Outputs
B0-B7	Data Register B Inputs
	Data Register B Outputs
CPAB, CPBA	Clock Pulse Inputs
SAB, SBA	Transmit/Receive Inputs
G	Output Enable Input
DIR	Direction Control Input

	SOIC JEDEC	TSSOP JEDEC
Order Number	74LVT646WM 74LVT646WMX	74LVT646MTCX
See NS Package Number	M24B	MTC24

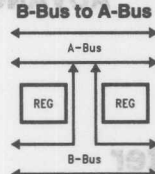
Real Time Transfer



TL/F/12017-4

FIGURE 1

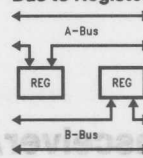
Real Time Transfer



TL/F/12017-5

FIGURE 2

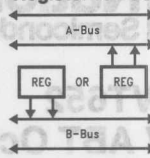
Storage from



TL/F/12017-6

FIGURE 3

Transfer from



TL/F/12017-7

FIGURE 4

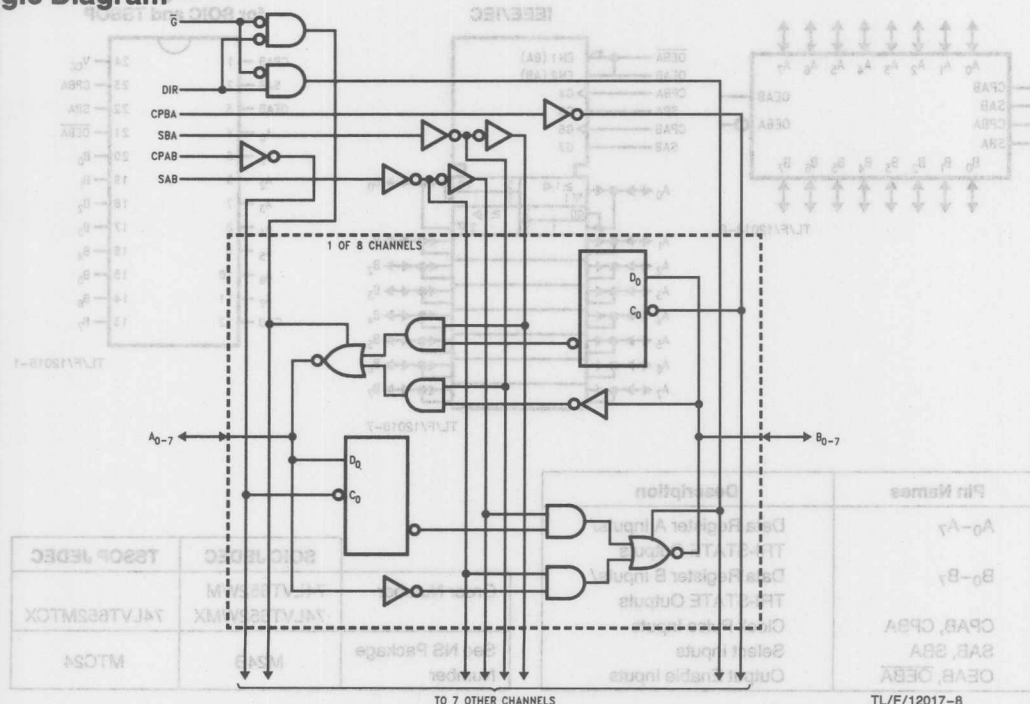
Truth Table (Note)

Inputs						Data I/O		Function
$\bar{G}$	DIR	CPAB	CPBA	SAB	SBA	A <sub>0</sub> -A <sub>7</sub>	B <sub>0</sub> -B <sub>7</sub>	
H	X	H or L	H or L	X	X	Input	Input	Isolation
H	X	X	X	X	X			Clock A <sub>n</sub> Data into A Register
H	X	X	X	X	X			Clock B <sub>n</sub> Data into B Register
L	H	X	X	L	X	Input	Output	A <sub>n</sub> to B <sub>n</sub> —Real Time (Transparent Mode)
L	H	X	X	X	X			Clock A <sub>n</sub> Data into A Register
L	H	H or L	X	H	X			A Register to B <sub>n</sub> (Stored Mode)
L	H	X	X	H	X			Clock A <sub>n</sub> Data into A Register and Output to B <sub>n</sub>
L	L	X	X	X	L	Output	Input	B <sub>n</sub> to A <sub>n</sub> —Real Time (Transparent Mode)
L	L	X	X	X	X			Clock B <sub>n</sub> Data into B Register
L	L	X	H or L	X	H			B Register to A <sub>n</sub> (Stored Mode)
L	L	X	X	X	H			Clock B <sub>n</sub> Data into B Register and Output to A <sub>n</sub>

**Note:** The data output functions may be enabled or disabled by various signals at the  $\bar{G}$  and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the appropriate clock inputs.

H = HIGH Voltage Level L = LOW Voltage Level X = Immaterial / = LOW-to-HIGH Transition

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.



## 74LVT652

### 3.3V ABT Octal Transceiver/Register with TRI-STATE® Outputs

#### General Description

The LVT652 consists of bus transceiver circuits with D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to HIGH logic level. Output Enable pins (OEAB,  $\overline{\text{OEBA}}$ ) are provided to control the transceiver function.

These bus/octal buffers and line drivers is/are designed for low-voltage (3.3V)  $V_{CC}$  applications, but with the capability to provide a TTL interface to a 5V environment. The LVT652 is fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

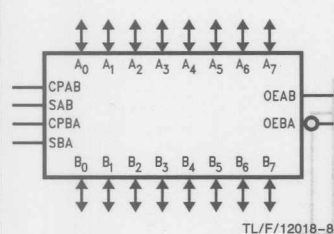
#### ADVANCE INFORMATION

#### Features

- Input and output interface capability to systems at 5V  $V_{CC}$
- Bus-Hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink  $-32 \text{ mA} / +64 \text{ mA}$
- Available in SOIC JEDEC and TSSOP
- Functionally compatible with the 74 series 652
- Latch-up performance exceeds 500 mA

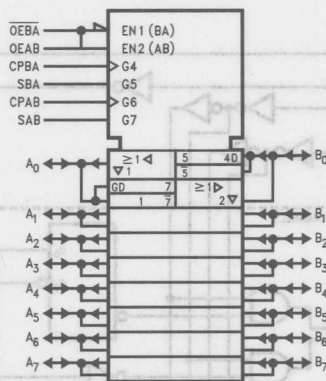
**Ordering Code:** See Section 11

#### Logic Symbols



TL/F/12018-8

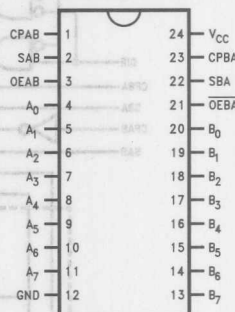
#### IEEE/IEC



TL/F/12018-7

#### Connection Diagram

##### Pin Assignment for SOIC and TSSOP

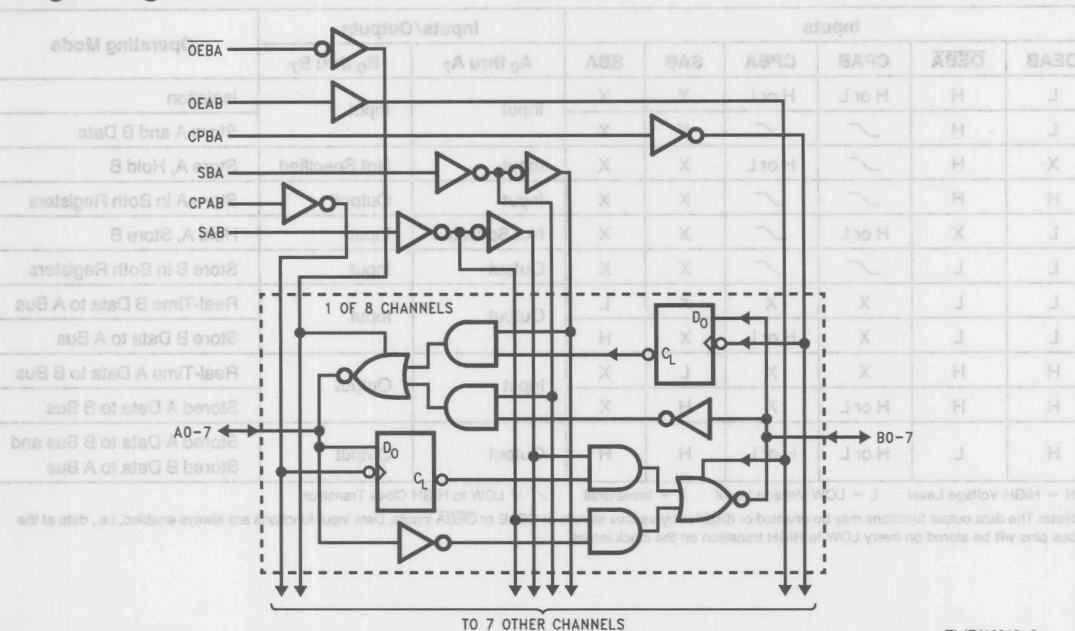


TL/F/12018-1

Pin Names	Description
A <sub>0</sub> -A <sub>7</sub>	Data Register A Inputs/ TRI-STATE Outputs
B <sub>0</sub> -B <sub>7</sub>	Data Register B Inputs/ TRI-STATE Outputs
CPAB, CPBA	Clock Pulse Inputs
SAB, SBA	Select Inputs
OEAB, $\overline{\text{OEBA}}$	Output Enable Inputs

	SOIC JEDEC	TSSOP JEDEC
Order Number	74LVT652WM 74LVT652WMX	74LVT652MTCX
See NS Package Number	M24B	MTC24

## Logic Diagram



TL/F/12018-2

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Functional Description

In the transceiver mode, data present at the HIGH impedance port may be stored in either the A or B register or both. The select (SAB, SBA) controls can multiplex stored and real-time.

The examples in Figure 1 demonstrate the four fundamental bus-management functions that can be performed with the LVT652.

Data on the A or B data bus, or both can be stored in the internal D flip-flop by LOW to HIGH transitions at the appro-

prate Clock Inputs (CPAB, CPBA) regardless of the Select or Output Enable Inputs. When SAB and SBA are in the real time transfer mode, it is also possible to store data without using the internal D flip-flops by simultaneously enabling OEAB and OEBA. In this configuration each Output reinforces its Input. Thus when all other data sources to the two sets of bus lines are in a HIGH impedance state, each set of bus lines will remain at its last state.

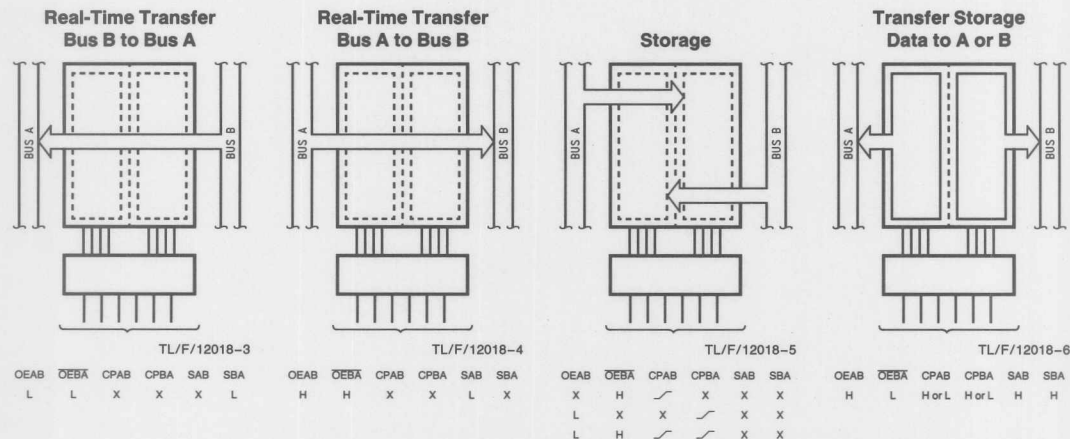








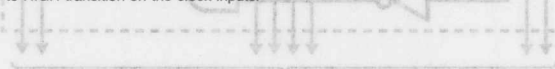


FIGURE 1

OEAB	OEBA	CPAB	CPBA	SAB	SBA	A <sub>0</sub> thru A <sub>7</sub>	B <sub>0</sub> thru B <sub>7</sub>	Operating Mode
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H			X	X			Store A and B Data
X	H		H or L	X	X	Input	Not Specified	Store A, Hold B
H	H			X	X	Input	Output	Store A in Both Registers
L	X	H or L		X	X	Not Specified	Input	Hold A, Store B
L	L			X	X	Output	Input	Store B in Both Registers
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus
L	L	X	H or L	X	H			Store B Data to A Bus
H	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus
H	H	H or L	X	H	X			Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored A Data to B Bus and Stored B Data to A Bus

H = HIGH Voltage Level L = LOW Voltage Level X = Immaterial ↗ = LOW to HIGH Clock Transition

**Note:** The data output functions may be enabled or disabled by various signals at OEAB or OEBA inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW to HIGH transition on the clock inputs.



TLV12018-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

plate Clock Inputs (CPAB, CPBA) regardless of the Select or Output Enable inputs. When SAB and SBA are in the real time transfer mode, it is also possible to store data without using the internal D flip-flops by simultaneously enabling OEAB and OEBA. In this configuration each Output register as its input. Thus when all other data sources to the two sets of bus lines are in a HIGH impedance state, each set of bus lines will remain at its last state.

## Functional Description

in the transceiver mode, data present at the HIGH impedance port may be stored in either the A or B register or both. The select (SAB, SBA) controls can multiplex stored and real-time.

The examples in Figure 1 demonstrate the four fundamental bus-management functions that can be performed with the TLV12018-5.

Data on the A or B data bus, or both can be stored in the internal D flip-flop by LOW to HIGH transitions at the appropriate

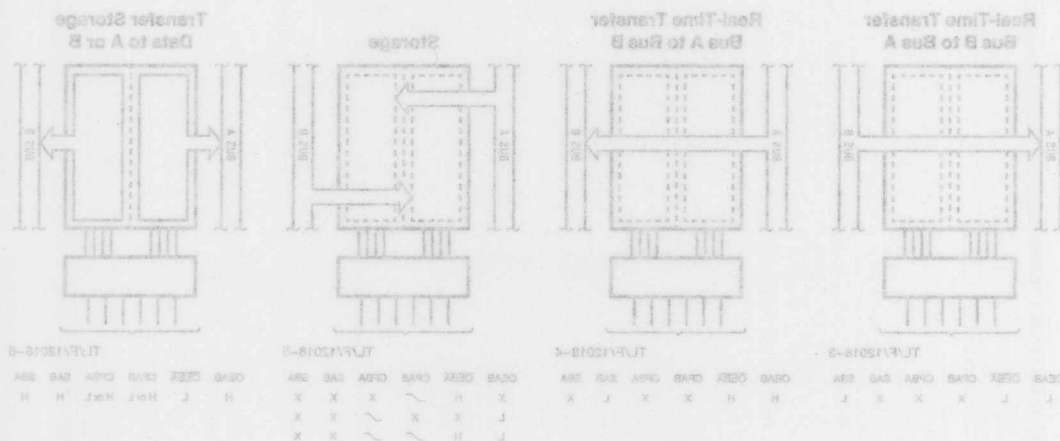


FIGURE 1



## 74LVT16240

### 3.3V ABT 16-Bit Inverting Buffer/Line Driver with TRI-STATE® Outputs

#### General Description

The LVT16240 contains sixteen inverting buffers with TRI-STATE outputs designed to be employed as a memory and address driver, clock driver, or bus-oriented transmitter/receiver. The device is nibble controlled.

Individual TRI-STATE control inputs can be shorted together for 8-bit or 16-bit operation.

These buffers and line drivers are designed for low-voltage (3.3V)  $V_{CC}$  applications, but with the capability to provide a TTL interface to a 5V environment. The LVT16240 is fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

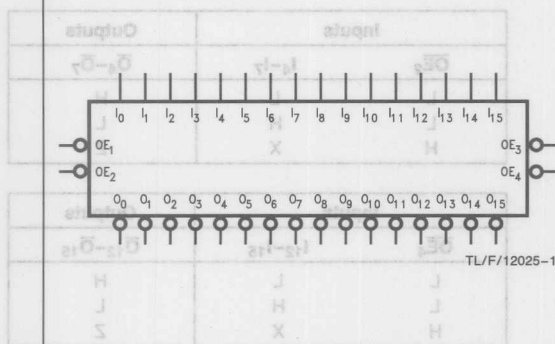
#### ADVANCE INFORMATION

#### Features

- Input and output interface capability to systems at 5V  $V_{CC}$
- Bus-Hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink  $-32\text{ mA}/+64\text{ mA}$
- Available in SSOP and TSSOP
- Functionally compatible with the 74 series 16240
- Latch-up performance exceeds 500 mA

**Ordering Code:** See Section 11

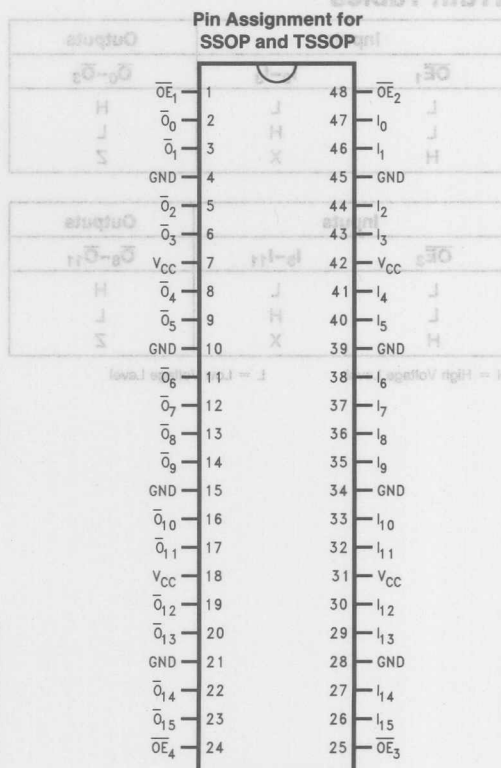
#### Logic Symbol



Pin Names	Description
$\overline{OE}_n$	Output Enable Inputs (Active Low)
$I_0-I_{15}$	Inputs
$O_0-O_{15}$	TRI-STATE Outputs

	SSOP	TSSOP JEDEC
Order Number	74LVT16240MEA 74LVT16240MEAX	74LVT16240MTD 74LVT16240MTDX
See NS Package Number	MS48A	MTD48

#### Connection Diagram



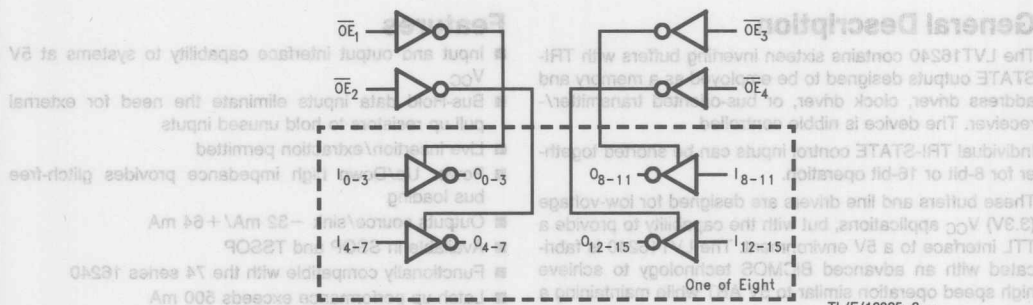
LVT16240

## Functional Description

The LVT16240 contains sixteen inverting buffers with TRI-STATE standard outputs. The device is nibble (4 bits) controlled with each nibble functioning identically, but independent of the other. The control pins may be shorted together to obtain full 16-bit operation. The TRI-STATE out-

puts are controlled by an Output Enable ( $\overline{OE}_n$ ) input for each nibble. When  $\overline{OE}_n$  is LOW, the outputs are in 2-state mode. When  $\overline{OE}_n$  is HIGH, the outputs are in the high impedance mode, but this does not interfere with entering new data into the inputs.

## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Truth Tables

Inputs		Outputs
$\overline{OE}_1$	$I_0-I_3$	$\overline{O}_0-\overline{O}_3$
L	L	H
L	H	L
H	X	Z

Inputs		Outputs
$\overline{OE}_3$	$I_8-I_{11}$	$\overline{O}_8-\overline{O}_{11}$
L	L	H
L	H	L
H	X	Z

H = High Voltage Level

L = Low Voltage Level

Inputs		Outputs
$\overline{OE}_2$	$I_4-I_7$	$\overline{O}_4-\overline{O}_7$
L	L	H
L	H	L
H	X	Z

Inputs		Outputs
$\overline{OE}_4$	$I_{12}-I_{15}$	$\overline{O}_{12}-\overline{O}_{15}$
L	L	H
L	H	L
H	X	Z

X = Immaterial

Z = High Impedance

Pin	Function
$\overline{OE}_n$	Output Enable Input (Active Low)
$I_0-I_{15}$	Inputs
$\overline{O}_0-\overline{O}_{15}$	TRI-STATE Outputs

Order Number	Part Number	Package
74VLT16240MEA	74VLT16240MTD	MS48A
74VLT16240MAX	74VLT16240MTDX	MTD48



## ADVANCE INFORMATION

LVT16244

# 74LVT16244

## 3.3V ABT 16-Bit Buffer/Line Driver

### with TRI-STATE® Outputs

### General Description

The LVT16244 contains sixteen non-inverting buffers with TRI-STATE outputs designed to be employed as a memory and address driver, clock driver, or bus oriented transmitter/receiver. The device is nibble controlled. Individual TRI-STATE control inputs can be shorted together for 8-bit or 16-bit operation.

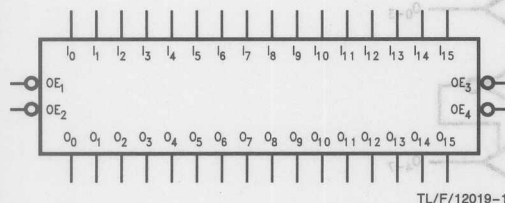
These bus buffers and line drivers are designed for low-voltage (3.3V)  $V_{CC}$  applications, but with the capability to provide a TTL interface to a 5V environment. The LVT16244 is fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

### Features

- Input and output interface capability to systems at 5V  $V_{CC}$
- Bus-Hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink  $-32\text{ mA}/+64\text{ mA}$
- Available in SSOP and TSSOP
- Functionally compatible with the 74 series 16244
- Latch-up performance exceeds 500 mA

**Ordering Code:** See Section 11

### Logic Symbol



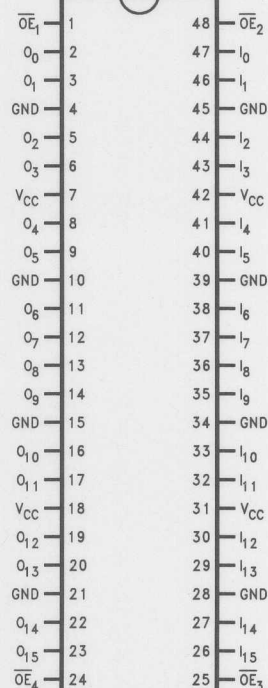
TL/F/12019-1

Pin Names	Description
$\overline{OE}_n$	Output Enable Inputs (Active Low)
$I_0-I_{15}$	Inputs
$O_0-O_{15}$	Outputs

	SSOP	TSSOP JEDEC
Order Number	74LVT16244MEA 74LVT16244MEAX	74LVT16244MTD 74LVT16244MTDX
See NS Package Number	MS48A	MTD48

### Connection Diagram

Pin Assignment for SSOP and TSSOP



TL/F/12019-2

TRI-STATE outputs. The device is nibble (4 bits) controlled with each nibble functioning identically, but independent of the other. The control pins can be shorted together to obtain full 16-bit operation.

## Truth Tables

Inputs		Outputs
$\overline{OE}_1$	$I_0-I_3$	$O_0-O_3$
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
$\overline{OE}_3$	$I_8-I_{11}$	$O_8-O_{11}$
L	L	L
L	H	H
H	X	Z

H = High Voltage Level

L = Low Voltage Level

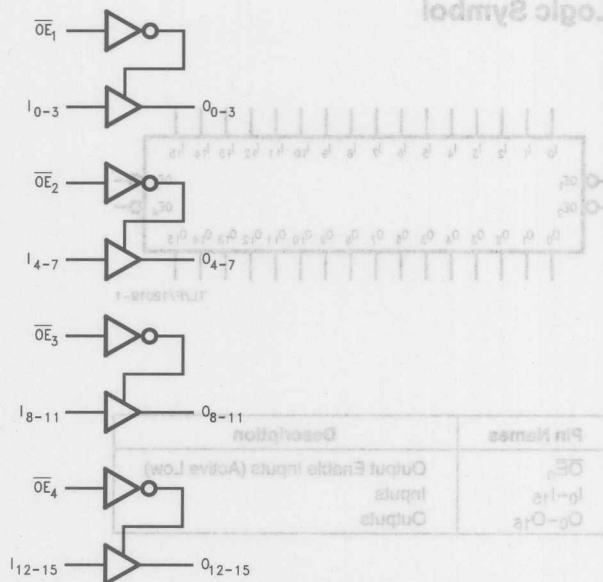
Inputs		Outputs
$\overline{OE}_2$	$I_4-I_7$	$O_4-O_7$
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
$\overline{OE}_4$	$I_{12}-I_{15}$	$O_{12}-O_{15}$
L	L	L
L	H	H
H	X	Z

X = Immaterial

Z = High Impedance

## Logic Diagram



TL/F/12019-3

Order Number	MS46A	MS46B
74V1624MEX	74V1624MTD	74V1624MTD
74V1624MEX	74V1624MTD	74V1624MTD



## 74LVT16245

### 3.3V ABT 16-Bit Transceiver with TRI-STATE® Outputs

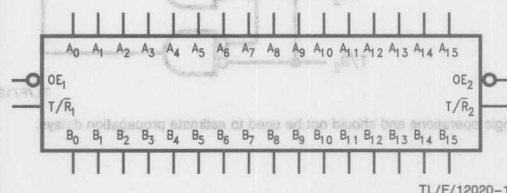
#### General Description

The LVT16245 contains sixteen non-inverting bidirectional buffers with TRI-STATE outputs and is intended for bus oriented applications. The device is byte controlled. Each byte has separate control inputs which can be shorted together for full 16-bit operation. The  $T/\bar{R}$  inputs determine the direction of data flow through the device. The  $\bar{OE}$  inputs disable both the A and B ports by placing them in a high impedance state.

This non-inverting transceiver is designed for low-voltage (3.3V)  $V_{CC}$  applications, but with the capability to provide a TTL interface to a 5V environment. The LVT16245 is fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

**Ordering Code:** See Section 11

#### Logic Symbol



Pin Names	Description
$\bar{OE}_n$	Output Enable Input (Active Low)
$T/\bar{R}_n$	Transmit/Receive Input
$A_0-A_{15}$	Side A Inputs/TRI-STATE Outputs
$B_0-B_{15}$	Side B Inputs/TRI-STATE Outputs

	SSOP	TSSOP JEDEC
Order Number	74LVT16245MEA 74LVT16245MEAX	74LVT16245MTD 74LVT16245MTDX
See NS Package Number	MS48A	MTD48

#### ADVANCE INFORMATION

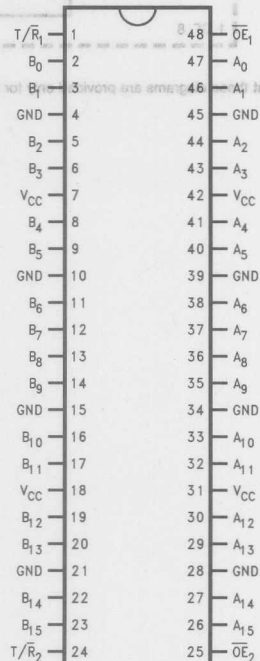
The LVT16245 contains sixteen non-inverting bidirectional buffers with TRI-STATE outputs. The device is byte controlled with each byte functioning identically, but independent of the other. The control pins can be shorted together to obtain full 16-bit operation.

#### Features

- Input and output interface capability to systems at 5V  $V_{CC}$
- Bus-Hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink  $-32\text{ mA}/+64\text{ mA}$
- Available in SSOP and TSSOP
- Functionally compatible with the 74 series 16245
- Latch-up performance exceeds 500 mA

#### Connection Diagram

Pin Assignment for SSOP and TSSOP



TL/F/12020-2

## Functional Description

The LVT16245 contains sixteen non-inverting bidirectional buffers with TRI-STATE outputs. The device is byte controlled with each byte functioning identically, but independent of the other. The control pins can be shorted together to obtain full 16-bit operation.

## Truth Tables

Inputs		Outputs
$\overline{OE}_1$	$T/\overline{R}_1$	
L	L	Bus B <sub>0</sub> -B <sub>7</sub> Data to Bus A <sub>0</sub> -A <sub>7</sub>
L	H	Bus A <sub>0</sub> -A <sub>7</sub> Data to Bus B <sub>0</sub> -B <sub>7</sub>
H	X	HIGH-Z State on A <sub>0</sub> -A <sub>7</sub> , B <sub>0</sub> -B <sub>7</sub>

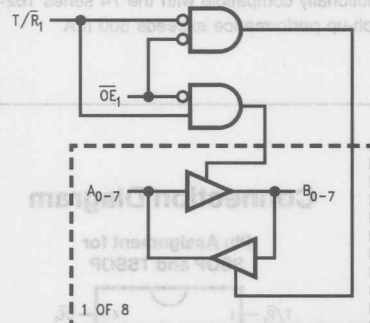
H = High Voltage Level L = Low Voltage Level

Inputs		Outputs
$\overline{OE}_2$	$T/\overline{R}_2$	
L	L	Bus B <sub>8</sub> -B <sub>15</sub> Data to Bus A <sub>8</sub> -A <sub>15</sub>
L	H	Bus A <sub>8</sub> -A <sub>15</sub> Data to Bus B <sub>8</sub> -B <sub>15</sub>
H	X	HIGH-Z State on A <sub>8</sub> -A <sub>15</sub> , B <sub>8</sub> -B <sub>15</sub>

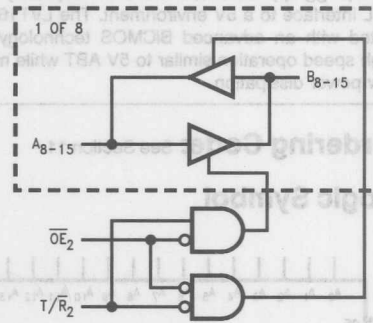
X = Immaterial

Z = High Impedance

## Logic Diagrams



TL/F/12020-3



TL/F/12020-4

Please note that these diagrams are provided only for the understanding of logic operations and should not be used to estimate propagation delays.



TL/F/12020-5

Pin Name	Description
B <sub>0</sub> -B <sub>7</sub>	Side B Input/TRI-STATE Output
A <sub>0</sub> -A <sub>7</sub>	Side A Input/TRI-STATE Output
T/R <sub>n</sub>	Transmit/Receive Input
$\overline{OE}_n$	Output Enable Input (Active Low)

Order Number	820P	T820P JEDEC
74LVT16245MEA		74LVT16245MTD
74LVT16245MAX		74LVT16245MTDX
See NS Package Number	M248A	MTD48

# 74LVT16373

## 3.3V ABT 16-Bit Transparent Latch with TRI-STATE® Outputs

### General Description

The LVT16373 contains sixteen non-inverting latches with TRI-STATE outputs and is intended for bus oriented applications. The device is byte controlled. The flip-flops appear transparent to the data when the Latch Enable (LE) is HIGH. When LE is low, the data that meets the setup time is latched. Data appears on the bus when the Output Enable (OE) is LOW. When OE is HIGH, the outputs are in high Z state.

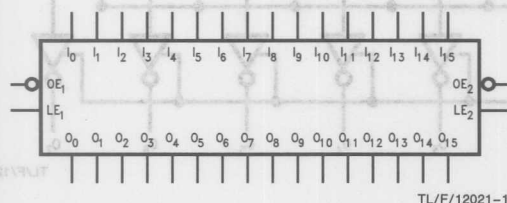
These latches are designed for low-voltage (3.3V)  $V_{CC}$  applications, but with the capability to provide a TTL interface to a 5V environment. The LVT16373 is fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

### Features

- Input and output interface capability to systems at 5V  $V_{CC}$
- Bus-Hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink  $-32\text{ mA}/+64\text{ mA}$
- Available in SSOP and TSSOP
- Functionally compatible with the 74 series 16373
- Latch-up performance exceeds 500 mA

**Ordering Code:** See Section 11

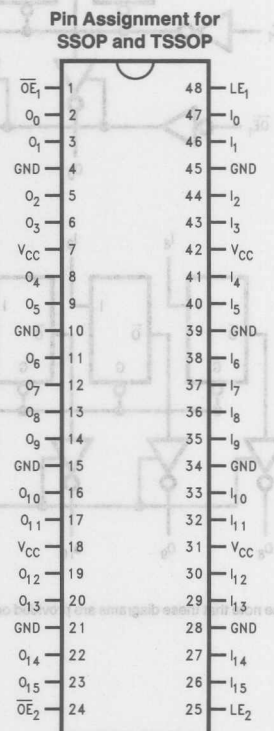
### Logic Symbol



Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active Low)
$LE_n$	Latch Enable Input
$I_0-I_{15}$	Inputs
$O_0-O_{15}$	TRI-STATE Outputs

	SSOP	TSSOP JEDEC
Order Number	74LVT16373MEA 74LVT16373MEAX	74LVT16373MTD 74LVT16373MTDX
See NS Package Number	MS48A	MTD48

### Connection Diagram



TL/F/12021-2

16-bit operation. The following description applies to each byte. When the Latch Enable ( $LE_n$ ) input is HIGH, data on the  $D_n$  enters the latches. In this condition the latches are transparent, i.e., a latch output will change states each time its D input changes. When  $LE_n$  is LOW, the latches store information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of  $LE_n$ . The TRI-STATE standard outputs are controlled by the Output Enable ( $OE_n$ ) input. When  $OE_n$  is LOW, the standard outputs are in the 2-state mode. When  $OE_n$  is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	$O_0$

Inputs			Outputs
$LE_2$	$OE_2$	$I_8-I_{15}$	$O_8-O_{15}$
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	$O_0$

H = High Voltage Level

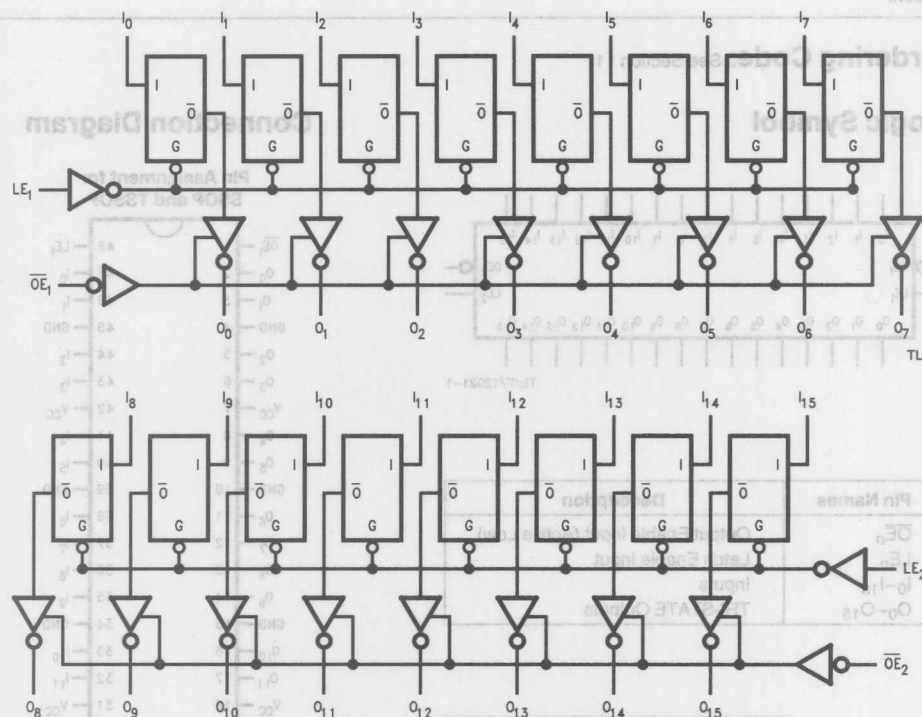
L = Low Voltage Level

X = Immaterial

Z = High Impedance

$O_0$  = Previous output prior to HIGH to LOW transition of  $LE$

## Logic Diagrams



TL/F/12021-3

TL/F/12021-4

Please note that these diagrams are provided only for the understanding of logic operations and should not be used to estimate propagation delays.



**74LVT16374**

## 3.3V ABT 16-Bit D Flip-Flop with TRI-STATE® Outputs

### General Description

The LVT16374 contains sixteen non-inverting D flip-flops with TRI-STATE outputs and is intended for bus oriented applications. The device is byte controlled. A buffered clock (CP) and Output Enable (OE) are common to each byte and can be shorted together for full 16-bit operation.

These flip-flops are designed for low-voltage (3.3V)  $V_{CC}$  applications, but with the capability to provide a TTL interface to a 5V environment. The LVT16374 is fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

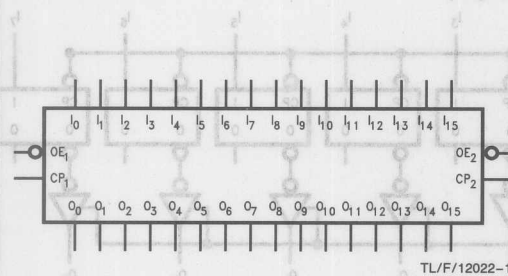
### ADVANCE INFORMATION

### Features

- Input and output interface capability to systems at 5V  $V_{CC}$
- Bus-Hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink -32 mA/+64 mA
- Available in SSOP and TSSOP
- Functionally compatible with the 74 series 16374
- Latch-up performance exceeds 500 mA

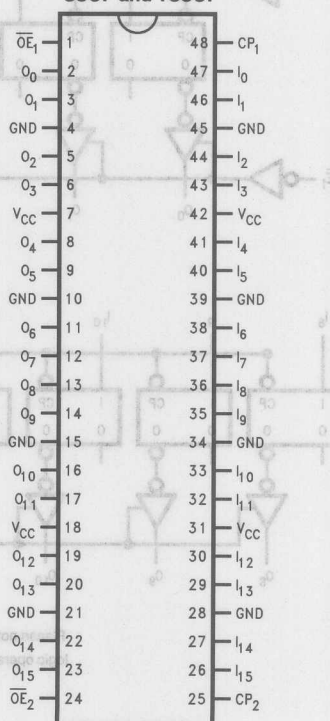
**Ordering Code:** See Section 11

### Logic Symbol



### Connection Diagram

Pin Assignment for SSOP and TSSOP



Pin Names	Description
$\overline{OE}_n$	TRI-STATE Output Enable Input (Active Low)
$CP_n$	Clock Pulse Input
$I_0-I_{15}$	Data Inputs
$O_0-O_{15}$	TRI-STATE Outputs

	SSOP	TSSOP JEDEC
Order Number	74LVT16374MEA 74LVT16374MEAX	74LVT16374MTD 74LVT16374MTDX
See NS Package Number	MS48A	MTD48

TL/F/12022-2

LVT16374

## Functional Description

The LVT16374 consists of sixteen edge-triggered flip-flops with individual D-type inputs and TRI-STATE true outputs. The device is byte controlled with each byte functioning identically, but independent of the other. The control pins can be shorted together to obtain full 16-bit operation. Each byte has a buffered clock and buffered Output Enable common to all flip-flops within that byte. The description which follows applies to each byte. Each flip-flop will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP<sub>n</sub>) transition. With the Output Enable ( $\overline{OE}_n$ ) LOW, the contents of the flip-flops are available at the outputs. When  $\overline{OE}_n$  is HIGH, the outputs go to the high impedance state. Operation of the  $\overline{OE}_n$  input does not affect the state of the flip-flops.

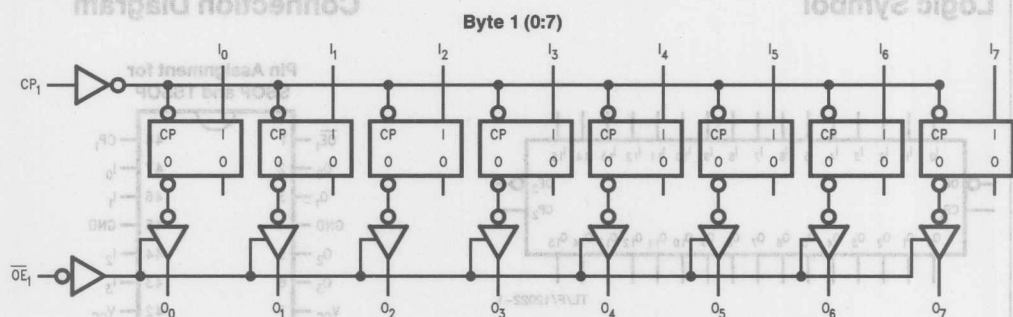
## Truth Tables

Inputs			Outputs
CP <sub>1</sub>	$\overline{OE}_1$	I <sub>0</sub> -I <sub>7</sub>	O <sub>0</sub> -O <sub>7</sub>
	L	H	H
	L	L	L
	L	X	O <sub>0</sub>
X	H	X	Z

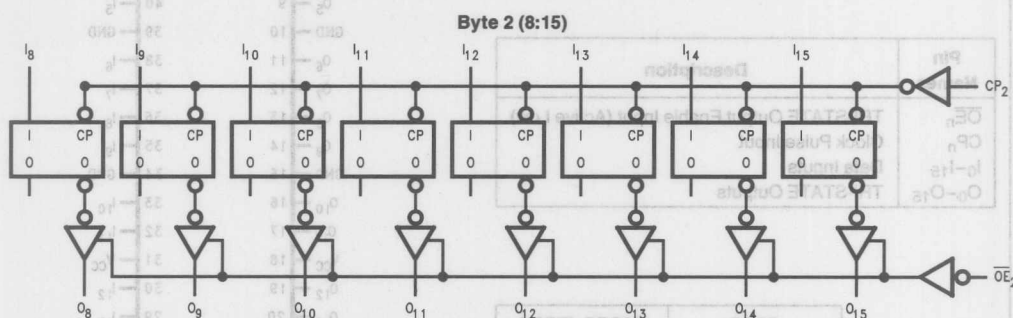
Inputs			Outputs
CP <sub>2</sub>	$\overline{OE}_2$	I <sub>8</sub> -I <sub>15</sub>	O <sub>8</sub> -O <sub>15</sub>
	L	H	H
	L	L	L
	L	X	O <sub>0</sub>
X	H	X	Z

H = High Voltage Level  
 L = Low Voltage Level  
 X = Immaterial  
 Z = High Impedance  
 O<sub>0</sub> = Previous O<sub>0</sub> before HIGH to LOW of CP

## Logic Diagrams



TL/F/12022-3



TL/F/12022-4

Please note that these diagrams are provided for the understanding of logic operation and should not be used to estimate propagation delays.



## ADVANCE INFORMATION

LVT16646

74LVT16646

# 3.3V ABT 16-Bit Transceiver/Register with TRI-STATE® Outputs

## General Description

The LVT16646 contains sixteen non-inverting bidirectional registered bus transceivers providing multiplexed transmission of data directly from the input bus or from the internal storage registers. Each byte has separate control inputs which can be shorted together for full 16-bit operation. The DIR inputs determine the direction of data flow through the device. The CPAB and CPBA inputs load data into the registers on the LOW-to-HIGH transition.

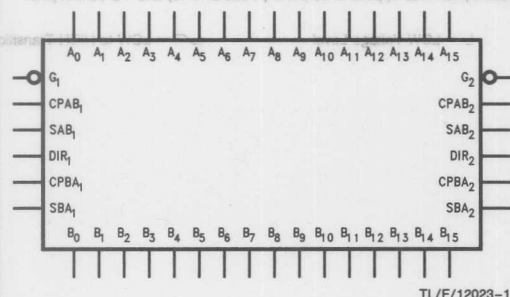
These transceivers are designed for low-voltage (3.3V)  $V_{CC}$  applications, but with the capability to provide a TTL interface to a 5V environment. The LVT16646 is fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

## Features

- Input and output interface capability to systems at 5V  $V_{CC}$
- Bus-Hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink  $\pm 32$  mA /  $\pm 64$  mA
- Available in SSOP and TSSOP
- Functionally compatible with the 74 series 16646
- Latch-up performance exceeds 500 mA

**Ordering Code:** See Section 11

## Logic Symbol



TL/F/12023-1

## Connection Diagram

### Pin Assignment for SSOP and TSSOP

DIR <sub>1</sub>	1	56	G <sub>1</sub>
CPAB <sub>1</sub>	2	55	CPBA <sub>1</sub>
SAB <sub>1</sub>	3	54	SBA <sub>1</sub>
GND	4	53	GND
A <sub>0</sub>	5	52	B <sub>0</sub>
A <sub>1</sub>	6	51	B <sub>1</sub>
V <sub>CC</sub>	7	50	V <sub>CC</sub>
A <sub>2</sub>	8	49	B <sub>2</sub>
A <sub>3</sub>	9	48	B <sub>3</sub>
A <sub>4</sub>	10	47	B <sub>4</sub>
GND	11	46	GND
A <sub>5</sub>	12	45	B <sub>5</sub>
A <sub>6</sub>	13	44	B <sub>6</sub>
A <sub>7</sub>	14	43	B <sub>7</sub>
A <sub>8</sub>	15	42	B <sub>8</sub>
A <sub>9</sub>	16	41	B <sub>9</sub>
A <sub>10</sub>	17	40	B <sub>10</sub>
GND	18	39	GND
A <sub>11</sub>	19	38	B <sub>11</sub>
A <sub>12</sub>	20	37	B <sub>12</sub>
A <sub>13</sub>	21	36	B <sub>13</sub>
V <sub>CC</sub>	22	35	V <sub>CC</sub>
A <sub>14</sub>	23	34	B <sub>14</sub>
A <sub>15</sub>	24	33	B <sub>15</sub>
GND	25	32	GND
SAB <sub>2</sub>	26	31	SBA <sub>2</sub>
CPAB <sub>2</sub>	27	30	CPBA <sub>2</sub>
DIR <sub>2</sub>	28	29	G <sub>2</sub>

TL/F/12023-2

	SSOP	TSSOP JEDEC
Order Number	74LVT16646MEA 74LVT16646MEAX	74LVT16646MTD 74LVT16646MTDX
See NS Package Number	MS56A	MTD56

Preliminary Data: National Semiconductor reserves the right to make changes at any time without notice.

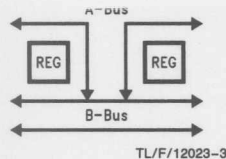


FIGURE 1

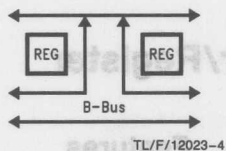


FIGURE 2

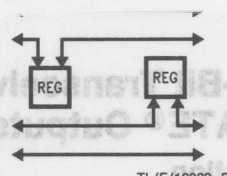


FIGURE 3

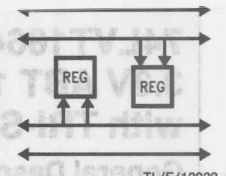


FIGURE 4

## Truth Table (Note)

Inputs						Data I/O		Output Operation Mode
G <sub>1</sub>	DIR <sub>1</sub>	CPBA <sub>1</sub>	CPBA <sub>1</sub>	SAB <sub>1</sub>	SBA <sub>1</sub>	A <sub>0-7</sub>	B <sub>0-7</sub>	
H	X	H or L	H or L	X	X	Input	Input	Isolation
H	X	↗	X	X	X			Clock An Data into A Register
H	X	X	↗	X	X			Clock Bn Data Into B Register
L	H	X	X	L	X	Input	Output	An to Bn—Real Time (Transparent Mode)
L	H	↗	X	L	X			Clock An Data to A Register
L	H	H or L	X	H	X			A Register to Bn (Stored Mode)
L	H	↗	X	H	X			Clock An Data into A Register and Output to Bn
L	L	X	X	X	L	Output	Input	Bn to An—Real Time (Transparent Mode)
L	L	X	↗	X	L			Clock Bn Data into B Register
L	L	X	H or L	X	H			B Register to An (Stored Mode)
L	L	X	↗	X	H			Clock Bn into B Register and Output to An

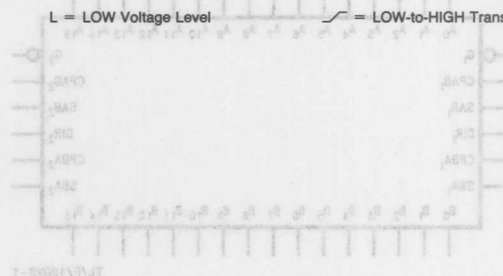
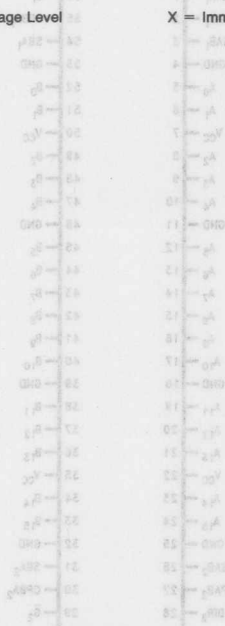
Note: The data output functions may be enabled or disabled by various signals at the G and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the appropriate clock inputs. Also applies to data I/O (A and B: 8-15) and #2 control pins.

H = HIGH Voltage Level

X = Immaterial

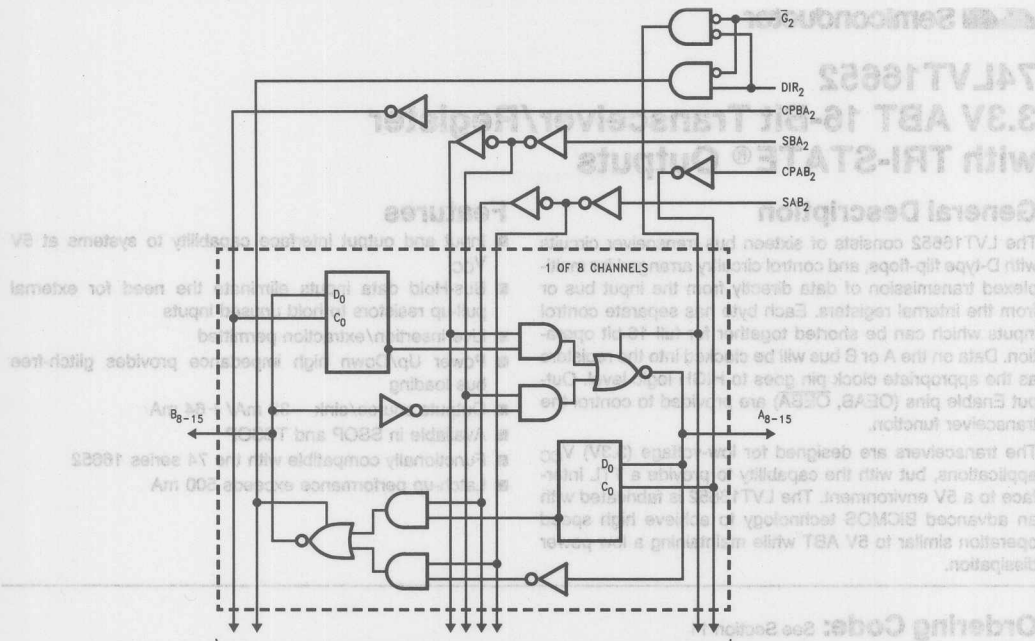
L = LOW Voltage Level

↗ = LOW-to-HIGH Transition.

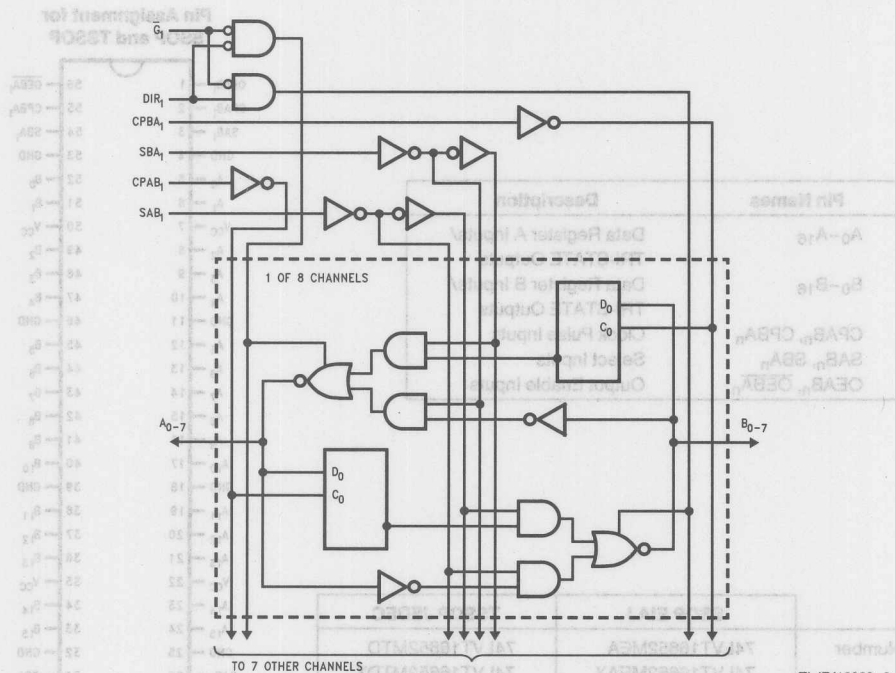


Order Number	74V11848MEX	74V11848MTD
See NS Package Number	M28A	MTD8
	74V11848MEX	74V11848MTD
	74V11848MEX	74V11848MTD

Preliminary Data: National Semiconductor reserves the right to make changes at any time without notice.



TL/F/12023-7



TL/F/12023-8

Please note that these diagrams are provided only for the understanding of logic operations and should not be used to estimate propagation delays.



## 74LVT16652 3.3V ABT 16-Bit Transceiver/Register with TRI-STATE® Outputs

### General Description

The LVT16652 consists of sixteen bus transceiver circuits with D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Each byte has separate control inputs which can be shorted together for full 16-bit operation. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to HIGH logic level. Output Enable pins (OEAB, OEBA) are provided to control the transceiver function.

The transceivers are designed for low-voltage (3.3V) V<sub>CC</sub> applications, but with the capability to provide a TTL interface to a 5V environment. The LVT16652 is fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

### Features

- Input and output interface capability to systems at 5V V<sub>CC</sub>
- Bus-Hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink — 32 mA / + 64 mA
- Available in SSOP and TSSOP
- Functionally compatible with the 74 series 16652
- Latch-up performance exceeds 500 mA

**Ordering Code:** See Section 11

### Connection Diagram

Pin Assignment for  
SSOP and TSSOP

Pin Names	Description
A <sub>0</sub> –A <sub>16</sub>	Data Register A Inputs/ TRI-STATE Outputs
B <sub>0</sub> –B <sub>16</sub>	Data Register B Inputs/ TRI-STATE Outputs
CPAB <sub>n</sub> , CPBA <sub>n</sub>	Clock Pulse Inputs
SAB <sub>n</sub> , SBA <sub>n</sub>	Select Inputs
OEAB <sub>n</sub> , OEBA <sub>n</sub>	Output Enable Inputs

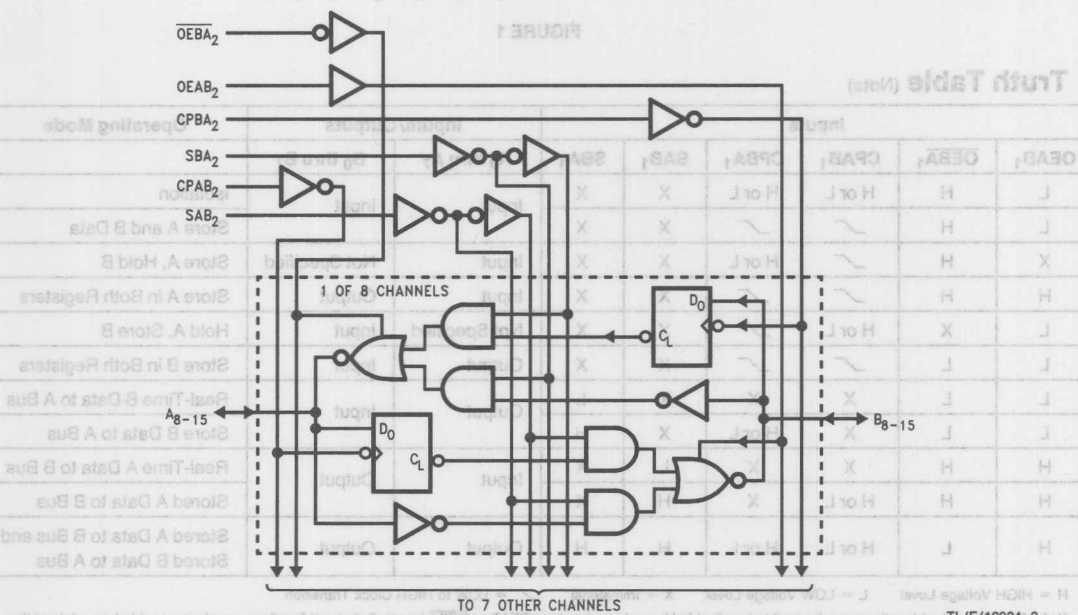
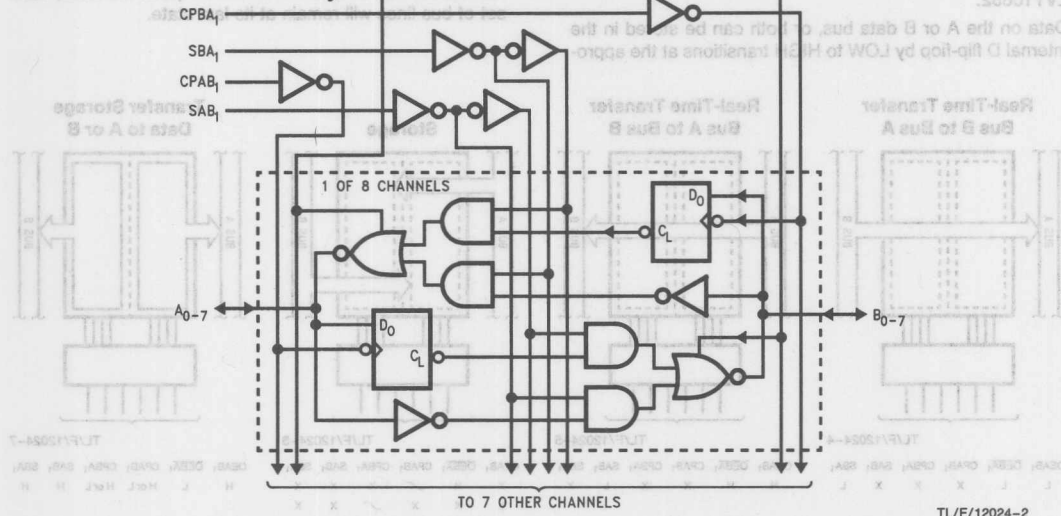
	SSOP EIAJ	TSSOP JEDEC
Order Number	74LVT16652MEA 74LVT16652MEAX	74LVT16652MTD 74LVT16652MTDX
NS Package Number	MS56A	MTD56

OEAB <sub>1</sub>	1	56	OEBA <sub>1</sub>
CPAB <sub>1</sub>	2	55	CPBA <sub>1</sub>
SAB <sub>1</sub>	3	54	SBA <sub>1</sub>
GND	4	53	GND
A <sub>0</sub>	5	52	B <sub>0</sub>
A <sub>1</sub>	6	51	B <sub>1</sub>
V <sub>CC</sub>	7	50	V <sub>CC</sub>
A <sub>2</sub>	8	49	B <sub>2</sub>
A <sub>3</sub>	9	48	B <sub>3</sub>
A <sub>4</sub>	10	47	B <sub>4</sub>
GND	11	46	GND
A <sub>5</sub>	12	45	B <sub>5</sub>
A <sub>6</sub>	13	44	B <sub>6</sub>
A <sub>7</sub>	14	43	B <sub>7</sub>
A <sub>8</sub>	15	42	B <sub>8</sub>
A <sub>9</sub>	16	41	B <sub>9</sub>
A <sub>10</sub>	17	40	B <sub>10</sub>
GND	18	39	GND
A <sub>11</sub>	19	38	B <sub>11</sub>
A <sub>12</sub>	20	37	B <sub>12</sub>
A <sub>13</sub>	21	36	B <sub>13</sub>
V <sub>CC</sub>	22	35	V <sub>CC</sub>
A <sub>14</sub>	23	34	B <sub>14</sub>
A <sub>15</sub>	24	33	B <sub>15</sub>
GND	25	32	GND
SAB <sub>2</sub>	26	31	SBA <sub>2</sub>
CPAB <sub>2</sub>	27	30	CPBA <sub>2</sub>
OEAB <sub>2</sub>	28	29	OEBA <sub>2</sub>

TL/F/12024-1

## Logic Diagrams

enable Clock Input (CPAB<sub>n</sub>, CPBA<sub>n</sub>) regardless of the Select or Output Enable inputs. When SAB and SBA are in the real time transfer mode, it is also possible to store data without using the real time transfer mode. In this configuration each output reinforces its input when all other data sources to the two sets of registers in a HIGH impedance state, each



Please note that these diagrams are provided only for the understanding of logic operations and should not be used to estimate propagation delays.

The select ( $SAB_n$ ,  $SBA_n$ ) controls can multiplex stored and real-time.

The examples in Figure 1 demonstrate the four fundamental bus-management functions that can be performed with the LVT16652.

Data on the A or B data bus, or both can be stored in the internal D flip-flop by LOW to HIGH transitions at the appro-

riate or Output Enable Inputs. When SAB and SBA are in the real time transfer mode, it is also possible to store data without using the internal D flip-flops by simultaneously enabling  $OEAB_n$  and  $OEBA_n$ . In this configuration each Output reinforces its Input. Thus when all other data sources to the two sets of bus lines are in a HIGH impedance state, each set of bus lines will remain at its last state.

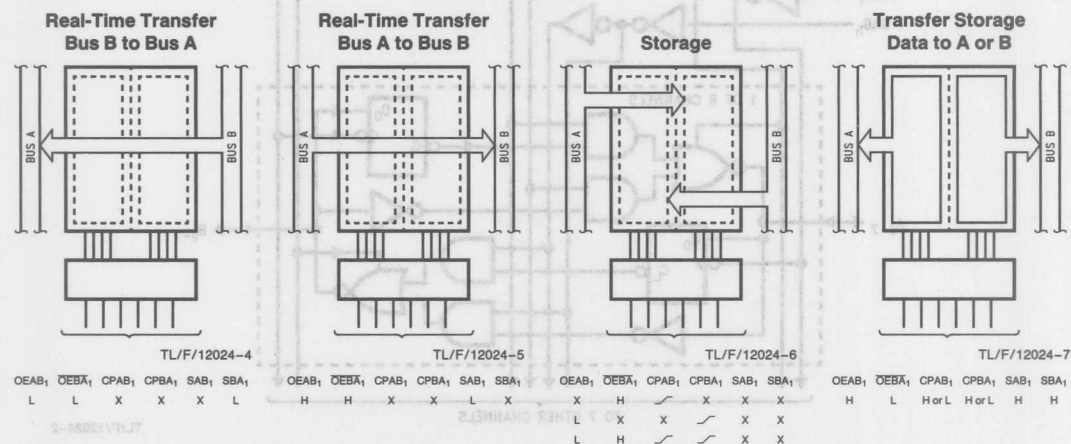


FIGURE 1

### Truth Table (Note)

Inputs						Inputs/Outputs		Operating Mode
$OEAB_1$	$OEBA_1$	$CPAB_1$	$CPBA_1$	$SAB_1$	$SBA_1$	$A_0$ thru $A_7$	$B_0$ thru $B_7$	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	—	—	X	X			Store A and B Data
X	H	—	H or L	X	X	Input	Not Specified	Store A, Hold B
H	H	—	—	X	X	Input	Output	Store A in Both Registers
L	X	H or L	—	X	X	Not Specified	Input	Hold A, Store B
L	L	—	—	X	X	Output	Input	Store B in Both Registers
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus
L	L	X	H or L	X	H			Store B Data to A Bus
H	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus
H	H	H or L	X	H	X			Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored A Data to B Bus and Stored B Data to A Bus

H = HIGH Voltage Level L = LOW Voltage Level X = Immaterial — = LOW to HIGH Clock Transition

**Note:** The data output functions may be enabled or disabled by various signals at  $OEAB$  or  $OEBA$  inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW to HIGH transition on the clock inputs. This also applies to data I/O (A and B: 8-15) and #2 control pins.

11-3	Available and Planned Package Offerings .....
11-4	Ordering Information and Physical Dimensions .....
11-4	Low Voltage Logic Ordering Information .....
11-6	Package Code vs NS Package Number .....
11-6	JEDC-EIAJ-SSOP Small Outline Package Comparison .....
11-7	Immediate Packing Method for Low Voltage Logic Packages .....
11-8	Tube Specifications and Drawings .....
11-10	Tape and Reel Specifications and Drawings .....
11-16	Physical Dimensions .....

## Section 11

### Physical Dimensions



## Section 11 Contents

Available and Planned Package Offering .....	11-3
Ordering Information and Physical Dimensions .....	11-4
Low Voltage Logic Ordering Information .....	11-4
Package Code vs NS Package Number .....	11-6
JEDEC-EIAJ-SSOP Small Outline Package Comparison .....	11-6
Immediate Packing Method for Low Voltage Logic Packages .....	11-7
Tube Specifications and Drawings .....	11-8
Tape and Reel Specifications and Drawings .....	11-10
Physical Dimensions .....	11-16
Bookshelf	
Distributors	

## Package Offering

### Available and Planned Package Offering

For most current packaging information, contact your National Semiconductor representative.

Type	Lead Count	LVQ	LVX	LCX	LVT
00	14	SOIC JEDEC & EIAJ	SOIC JEDEC & EIAJ, SSOP I, TSSOP		
02	14	SOIC JEDEC & EIAJ	SOIC JEDEC & EIAJ, SSOP I, TSSOP		
04	14	SOIC JEDEC & EIAJ	SOIC JEDEC & EIAJ, SSOP I, TSSOP		
08	14	SOIC JEDEC & EIAJ	SOIC JEDEC & EIAJ, SSOP I, TSSOP		
14	14	SOIC JEDEC & EIAJ	SOIC JEDEC & EIAJ, SSOP I, TSSOP		
32	14	SOIC JEDEC & EIAJ	SOIC JEDEC & EIAJ, SSOP I, TSSOP		
74	14	SOIC JEDEC & EIAJ	SOIC JEDEC & EIAJ, SSOP I, TSSOP		
86	14	SOIC JEDEC & EIAJ	SOIC JEDEC & EIAJ, SSOP I, TSSOP		
125	14	SOIC JEDEC & EIAJ	SOIC JEDEC & EIAJ, SSOP I, TSSOP		SOIC JEDEC & EIAJ, TSSOP
138	16	SOIC JEDEC & EIAJ	SOIC JEDEC & EIAJ, SSOP I, TSSOP		
151	16	SOIC JEDEC & EIAJ			
157	16	SOIC JEDEC & EIAJ	SOIC JEDEC & EIAJ, SSOP I, TSSOP		
174	16	SOIC JEDEC & EIAJ	SOIC JEDEC & EIAJ, SSOP I, TSSOP		
240	20	SOIC JEDEC & EIAJ, QSOP	SOIC JEDEC & EIAJ, SSOP I, TSSOP	SOIC JEDEC & EIAJ, TSSOP	SOIC JEDEC & EIAJ, TSSOP
241	20	SOIC JEDEC & EIAJ, QSOP			
244	20	SOIC JEDEC & EIAJ, QSOP	SOIC JEDEC & EIAJ, SSOP I, TSSOP	SOIC JEDEC & EIAJ, TSSOP	SOIC JEDEC & EIAJ, TSSOP
245	20	SOIC JEDEC & EIAJ, QSOP	SOIC JEDEC & EIAJ, SSOP I, TSSOP	SOIC JEDEC & EIAJ, TSSOP	SOIC JEDEC & EIAJ, TSSOP
273	20	SOIC JEDEC & EIAJ, QSOP	SOIC JEDEC & EIAJ, SSOP I, TSSOP		
373	20	SOIC JEDEC & EIAJ, QSOP	SOIC JEDEC & EIAJ, SSOP I, TSSOP	SOIC JEDEC & EIAJ, TSSOP	SOIC JEDEC & EIAJ, TSSOP
374	20	SOIC JEDEC & EIAJ, QSOP	SOIC JEDEC & EIAJ, SSOP I, TSSOP	SOIC JEDEC & EIAJ, TSSOP	SOIC JEDEC & EIAJ, TSSOP
573	20	SOIC JEDEC & EIAJ, QSOP	SOIC JEDEC & EIAJ, SSOP I, TSSOP		
646	24			SOIC JEDEC, TSSOP	SOIC JEDEC, TSSOP
652	24			SOIC JEDEC, TSSOP	SOIC JEDEC, TSSOP
3245	24		SOIC JEDEC, QSOP		
4245	24		SOIC JEDEC, QSOP		
C3245	24		SOIC JEDEC, QSOP		
C4245	24		SOIC JEDEC, QSOP		
3L383	24		SOIC JEDEC, QSOP		
3L384	24		SOIC JEDEC, QSOP		
16240	48			SSOP, TSSOP	SSOP, TSSOP
16244	48			SSOP, TSSOP	SSOP, TSSOP
16245	48			SSOP, TSSOP	SSOP, TSSOP
16373	48			SSOP, TSSOP	SSOP, TSSOP
16374	48			SSOP, TSSOP	SSOP, TSSOP
16646	56			SSOP, TSSOP	SSOP, TSSOP
16652	56			SSOP, TSSOP	SSOP, TSSOP

WM = (0.300" Wide) Molded Small Outline Package, JEDEC  
 QSC = Shrink Small Outline Package, JEDEC  
 (also known as QSOP)

" " = Non-Configurable  
 Device Type





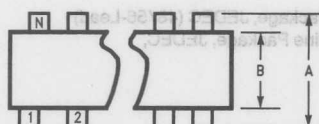
## Package Code vs NS Package Number

Package Code	Description	NS Package Number					
		14-Lead	16-Lead	20-Lead	24-Lead	48-Lead	56-Lead
S	Molded Small Outline Package, JEDEC	M14A	M16A	M20B	M24B		
M	Molded Small Outline Package, JEDEC	M14A	M16A	M20B	M24B		
WM	Molded Small Outline Package, JEDEC	M14B	M16B	M20B	M24B		
SJ	Molded Small Outline Package, EIAJ	M14D	M16D	M20D			
MSC	Molded Shrink Small Outline Package, EIAJ, Type I	MSC14	MSC16	MSC20			
MTC	Molded Thin Shrink Small Outline Package, JEDEC, 4.4 mm Body Width	MTC14	MTC16	MTC20	MTC24		
QS	Molded Shrink Small Outline Package, JEDEC (also known as QSOP)			MQA20	MQA24		
MEA	Molded Shrink Small Outline Package, JEDEC					MS48A	MS56A
MTD	Molded Thin Shrink Small Outline Package, JEDEC, 6.1 mm Body Width					MTD48	MTD56

## JEDEC-EIAJ-SSOP Small Outline Package Comparison

Package	Dim	14-Pin		16-Pin		20-Pin		24-Pin	
		Min	Max	Min	Max	Min	Max	Min	Max
SOIC JEDEC	A	0.228 (5.80)	0.245 (6.20)	0.228 (5.80)	0.245 (6.20)	0.393 (10.0)	0.420 (10.65)	0.393 (10.0)	0.420 (10.65)
	B	0.149 (3.80)	0.158 (4.00)	0.149 (3.80)	0.158 (4.00)	0.291 (7.40)	0.300 (7.60)	0.291 (7.40)	0.300 (7.60)
SOIC EIAJ	A	0.295 (7.50)	0.319 (8.10)	0.295 (7.62)	0.319 (8.89)	0.295 (7.62)	0.319 (8.89)		
	B	0.205 (5.20)	0.213 (5.40)	0.205 (5.20)	0.213 (5.40)	0.205 (5.20)	0.213 (5.40)		
SSOP Type I	A	0.240 (6.10)	0.264 (6.70)	0.240 (6.10)	0.264 (6.70)	0.240 (6.10)	0.264 (6.70)		
	B	0.165 (4.20)	0.181 (4.60)	0.165 (4.20)	0.181 (4.60)	0.165 (4.20)	0.181 (4.60)		
TSSOP	A	0.244 (6.20)	0.260 (6.60)	0.244 (6.20)	0.260 (6.60)	0.244 (6.20)	0.260 (6.60)	0.244 (6.20)	0.260 (6.60)
	B	0.169 (4.30)	0.177 (4.50)	0.169 (4.30)	0.177 (4.50)	0.169 (4.30)	0.177 (4.50)	0.169 (4.30)	0.177 (4.50)
SSOP JEDEC (aka QSOP)	A					0.231 (5.87)	0.241 (6.12)	0.231 (5.87)	0.241 (6.12)
	B					0.151 (3.84)	0.157 (3.99)	0.151 (3.84)	0.157 (3.99)

Units: Inch (mm)



TL/F/11642-1

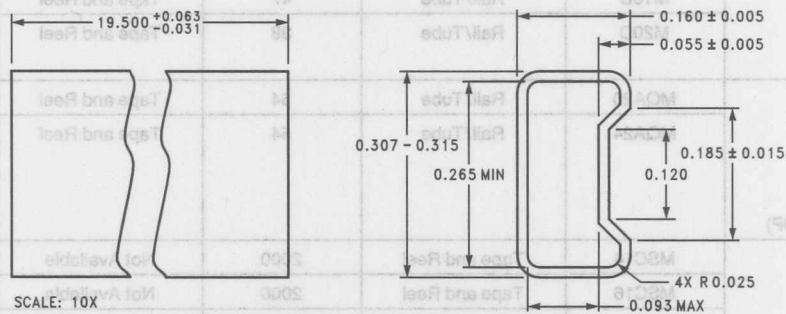
# Immediate Packing Method for Low Voltage Logic Packages

Package Type	NS Package Number	Primary Immediate Container		Secondary Immediate Container	
		Method	Quantity	Method	Quantity
Small Outline Package, JEDEC (SOIC)	M14A	Rail/Tube	55	Tape and Reel	2500
	M14B	Rail/Tube	50	Tape and Reel	1000
	M16A	Rail/Tube	48	Tape and Reel	2500
	M16B	Rail/Tube	45	Tape and Reel	1000
	M20B	Rail/Tube	36	Tape and Reel	1000
	M24B	Rail/Tube	30	Tape and Reel	1000
Small Outline Package, EIAJ (SOP)	M14D	Rail/Tube	47	Tape and Reel	1000
	M16D	Rail/Tube	47	Tape and Reel	1000
	M20D	Rail/Tube	38	Tape and Reel	1000
Shrink Small Outline Package, JEDEC (SSOP or QSOP)	MQA20	Rail/Tube	54	Tape and Reel	2500
	MQA24	Rail/Tube	54	Tape and Reel	2500
Shrink Small Outline Package, EIAJ, Type 1 (SSOP)	MSC14	Tape and Reel	2000	Not Available	
	MSC16	Tape and Reel	2000	Not Available	
	MSC20	Tape and Reel	2000	Not Available	
Shrink Small Outline Package, JEDEC (SSOP)	MEA48	Rail/Tube	29	Tape and Reel	1000
	MEA56	Rail/Tube	29	Tape and Reel	1000
Thin Shrink Small Outline Package, JEDEC 4.4 mm (TSSOP)	MTC14	Tape and Reel	2500		
	MTC16	Tape and Reel	2500		
	MTC20	Tape and Reel	2500		
	MTC24	Tape and Reel	2500		
Thin Shrink Small Outline Package, JEDEC 6.1 mm (TSSOP)	MTD48	Rail/Tube	39	Tape and Reel	
	MTD56	Rail/Tube	39	Tape and Reel	

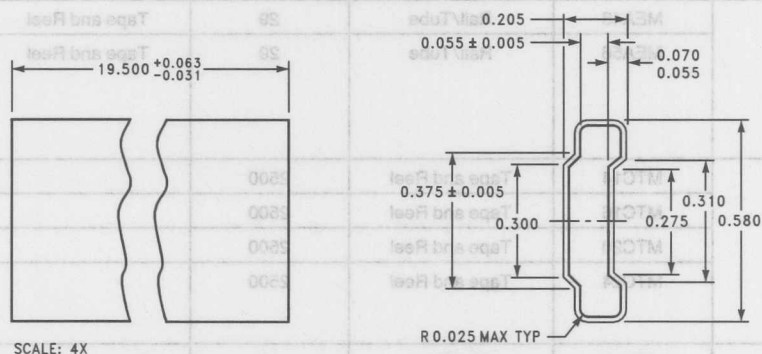
# Ordering Information and Physical

14 SO (150 mil) (M14A)	Static Dissipative	Clear	55
16 SO (150 mil) (M16A)	Static Dissipative	Clear	48
20 SO (300 mil) (M20B)	Static Dissipative	Clear	36
24 SO (300 mil) (M24B)	Static Dissipative	Clear	30
20 SSO (MQA20)	Static Dissipative	Clear	54
24 SSO (MQA24)	Static Dissipative	Clear	54

**JEDEC SSOP 20/24, JEDEC SOIC 14/16 (150 mil) Tube  
MQA20/MQA24, M14A/M16A**

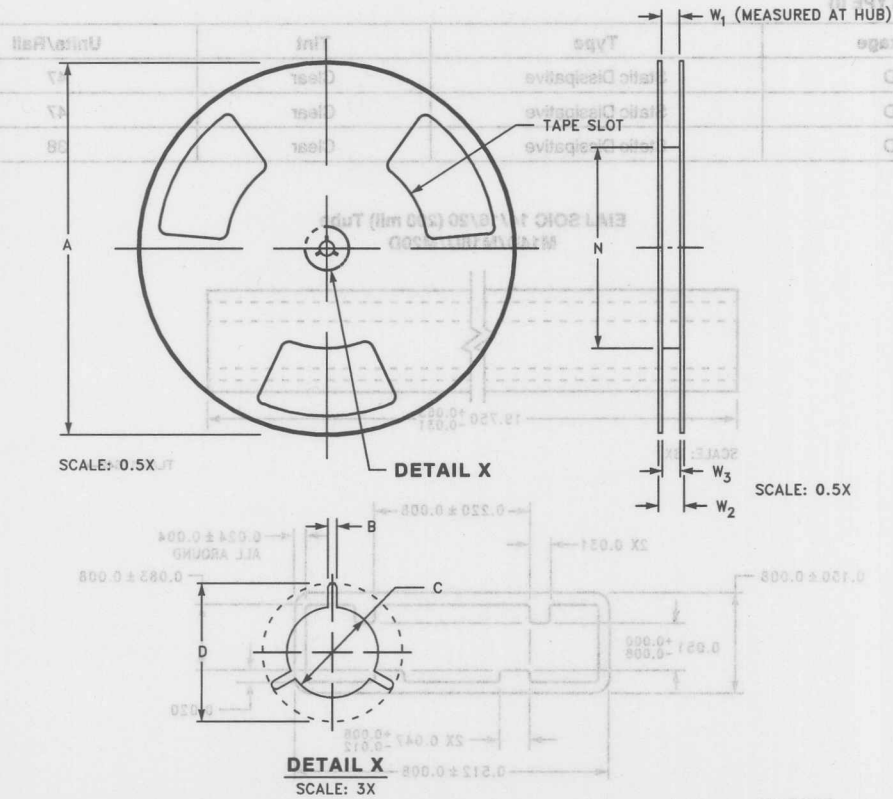


**JEDEC SOIC 20/24 (300 mil) Tube  
M20B/M24B**





# Tape and Reel Specifications and Drawings



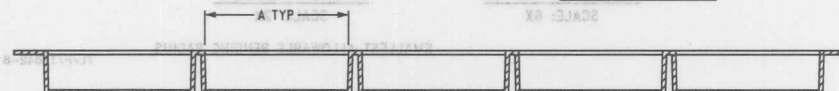
Plastic 13" Reel for 16 mm and 24 mm Tape

Tape Size	A	B	C	D	N	W <sub>1</sub>	W <sub>2</sub>	W <sub>3</sub>
24 mm	13.00 330.0	0.059 1.50	0.512 ± 0.008 13.00 ± 0.20	0.795 20.20	7.000 178.00	0.961 + 0.078/−0.000 24.40 + 2.00/−0.00	1.197 30.40	W <sub>1</sub> + 0.078/−0.039 W <sub>1</sub> + 2.00/−1.00
16 mm	13.00 330.0	0.059 1.50	0.512 ± 0.008 13.00 ± 0.20	0.795 20.20	7.000 178.00	0.646 + 0.078/−0.000 16.40 + 2.00/−0.00	0.882 22.40	W <sub>1</sub> + 0.078/−0.039 W <sub>1</sub> + 2.00/−1.00

## (Continued)

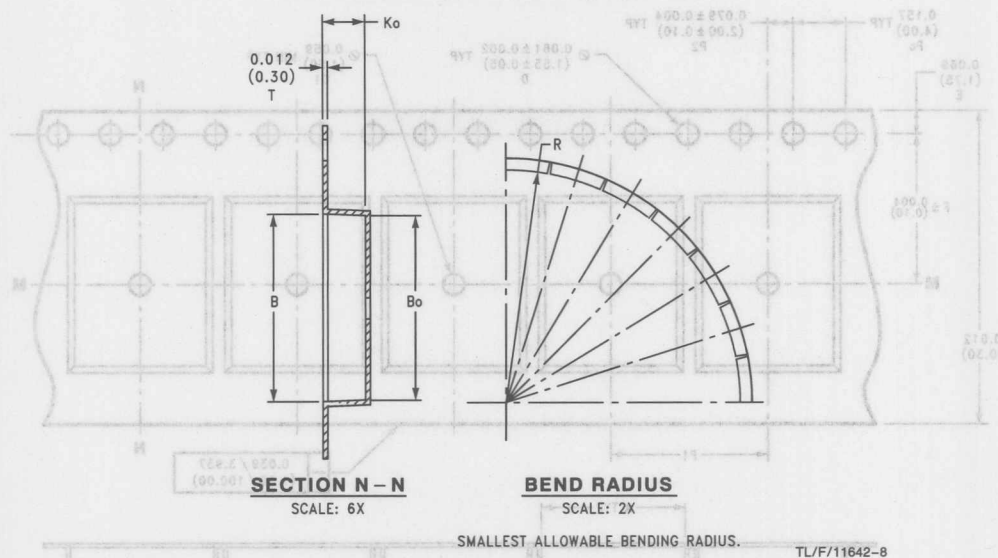
11

**JEDEC SOIC 16 mm and 24 mm Tape**

SECTION M - M

TL/F/11642-7

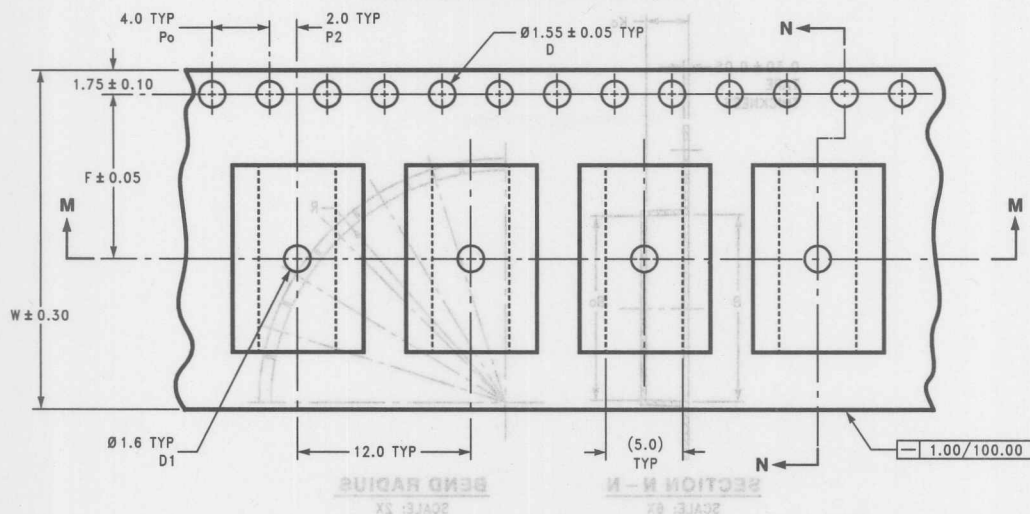
JEDEC SOIC 16mm and 24mm Tape (Continued)



Pkg Type	Tape Size	Dim B	Dim Bo	Dim Ko	Dim A	Dim Ao	Dim W	Dim F	Dim P1	Rad R
24 SO (300 mil)	24 mm	0.630 (16.00)	0.624 (15.85)	0.118 (3.00)	0.437 (11.10)	0.429 (10.90)	0.945 (24.00)	0.453 (11.50)	0.472 (12.00)	1.181 (30.00)
20 SO (300 mil)	24 mm	0.530 (13.45)	0.524 (13.30)	0.118 (3.00)	0.436 (11.08)	0.429 (10.90)	0.945 (24.00)	0.453 (11.50)	0.472 (12.00)	1.181 (30.00)
16 SO (150 mil)	16 mm	0.411 (10.45)	0.406 (10.30)	0.083 (2.10)	0.262 (6.65)	0.256 (6.50)	0.630 (16.00)	0.295 (7.50)	0.315 (8.00)	1.181 (30.00)
14 SO (150 mil)	16 mm	0.380 (9.65)	0.374 (9.50)	0.083 (2.10)	0.262 (6.65)	0.256 (6.50)	0.630 (16.00)	0.295 (7.50)	0.315 (8.00)	1.181 (30.00)
24 SSO (150 mil)	16 mm	0.380 (9.65)	0.374 (9.50)	0.083 (2.10)	0.262 (6.65)	0.256 (6.50)	0.630 (16.00)	0.295 (7.50)	0.315 (8.00)	1.181 (30.00)
20 SSO (150 mil)	16 mm	0.380 (9.65)	0.374 (9.50)	0.083 (2.10)	0.262 (6.65)	0.256 (6.50)	0.630 (16.00)	0.295 (7.50)	0.315 (8.00)	1.181 (30.00)

# Tape and Reel Specifications and Drawings (Continued)

EIAJ SOIC 16 mm and 24 mm Tape



SMALLEST ALLOWABLE BENDING RADIUS

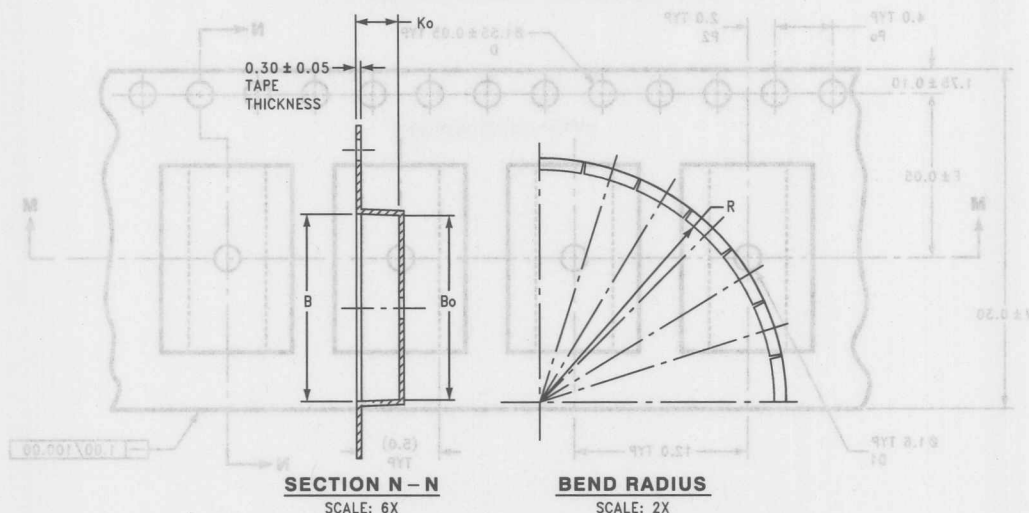
Pkg Type	Dim A	Dim B	Dim C	Dim D	Dim E	Dim F	Dim G	Dim H	Dim I	Dim J	Dim K	Dim L	Dim M	Dim N	Dim O	Dim P	Dim Q	Dim R	Dim S	Dim T	Dim U	Dim V	Dim W	Dim X	Dim Y	Dim Z
20 SO (200 mil)	24 mm	8.7	8.4	10.7	10.7	10.7	10.7	10.7	10.7	10.7	10.7	10.7	10.7	10.7	10.7	10.7	10.7	10.7	10.7	10.7	10.7	10.7	10.7	10.7	10.7	10.7
14/18 SO (200 mil)	18 mm	8.7	8.4	10.7	10.7	10.7	10.7	10.7	10.7	10.7	10.7	10.7	10.7	10.7	10.7	10.7	10.7	10.7	10.7	10.7	10.7	10.7	10.7	10.7	10.7	10.7

SECTION M-M

TL/F/11642-9

# Tape and Reel Specifications and Drawings (Continued)

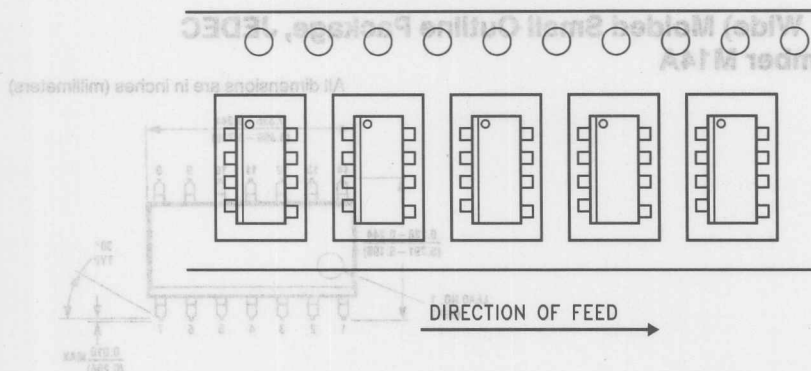
EIAJ SOIC 16 mm and 24 mm Tape (Continued)



Pkg Type	Tape Size	Dim A	Dim A <sub>o</sub>	Dim B	Dim B <sub>o</sub>	Dim F	Dim K <sub>o</sub>	Rad R	Dim W
20 SO (200 mil)	24 mm	8.7	8.4	13.5	13.2	11.5	2.4	50.0	24.0
14/16 SO (200 mil)	16 mm	8.7	8.4	11.0	10.7	7.5	2.4	50.0	16.0

## Tape and Reel Specifications and Drawings (Continued)

### Direction of Feed for SOIC Devices



TL/F/11642-11

### Tape and Reel Quantities

Package	Qty of Sealed Devices
JEDEC 14/16	2500
JEDEC 20/24	1000
EIAJ 14/16/20	1000

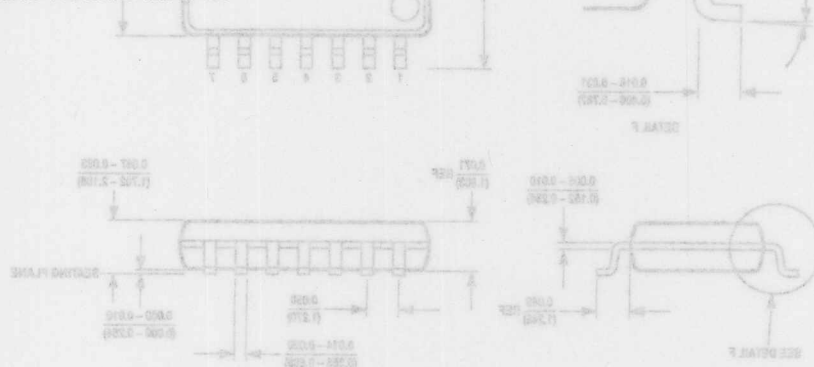
### JEDEC and EIAJ SOIC Carrier Tape Specifications

Leader (mm)						Hub (mm)					
Unsealed Carrier		Sealed Carrier		Overall Carrier		Unsealed Carrier		Sealed Carrier		Overall Carrier	
Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
0	400	500	1200	500	1200	0	340	300	640	300	740

The overall carrier minimum specification is determined by the sealed carrier minimum.

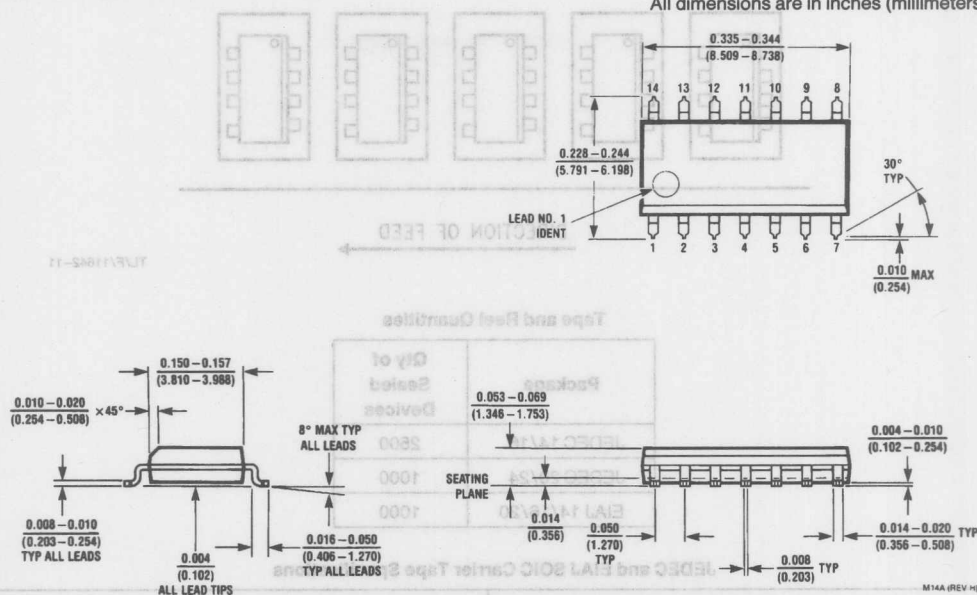
The overall carrier maximum consists of the sealed carrier minimum plus a combination of unsealed carrier and any additional sealed carrier. For example, the leader's overall maximum of 1200 mm consists of a 500 mm minimum sealed carrier, with a remaining 700 mm combination of unsealed (0 mm to 400 mm) and/or sealed (0 mm to 700 mm) carrier.

The number of pockets in the leader or hub carrier tape are determined by the tape's pitch. For example the pitch for a JEDEC SOIC 14 (mil) 16 mm tape, the P1 dimension from the previous pages, is 8.0 mm. Thus the maximum leader unsealed carrier pockets would be 400 mm/8 mm or 50.



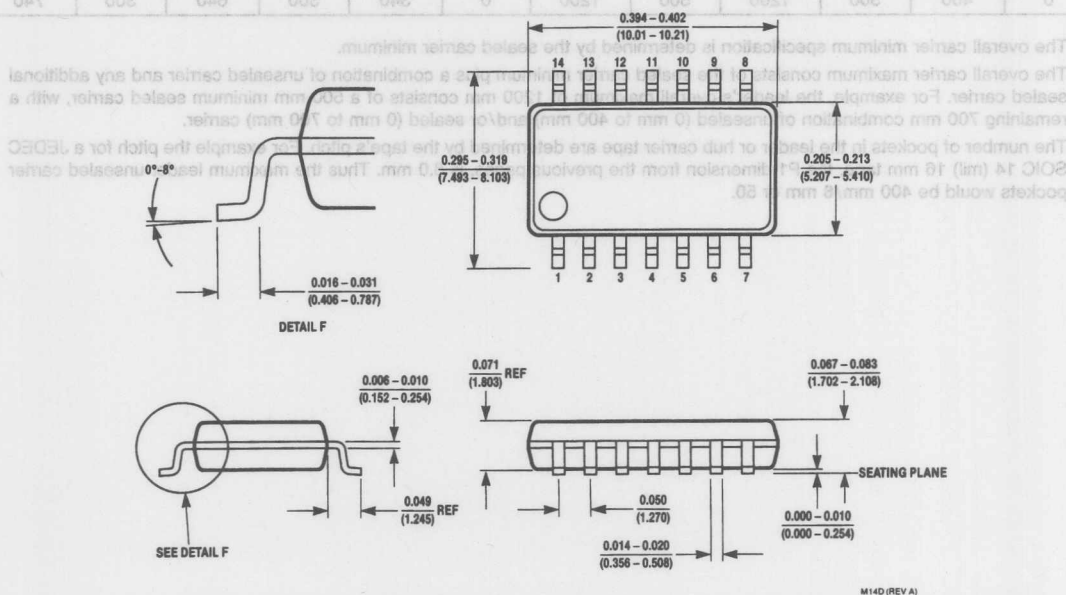
# 14 Lead (0.150" Wide) Molded Small Outline Package, JEDEC NS Package Number M14A

All dimensions are in inches (millimeters)



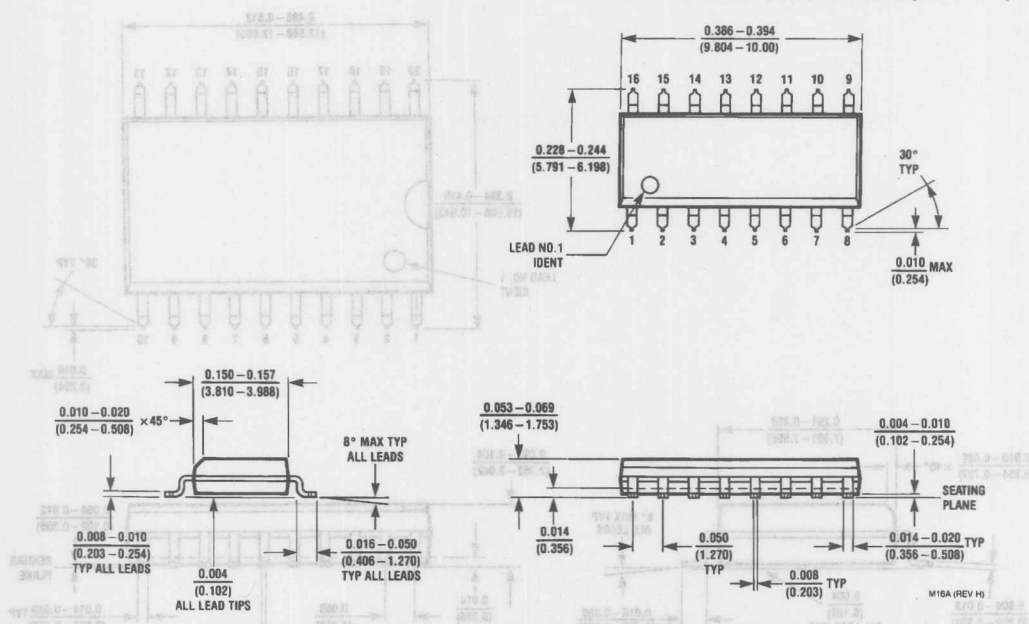
## 14 Lead Molded Small Outline Package (SOP), EIAJ Type II NS Package Number M14D

All dimensions are in inches (millimeters)



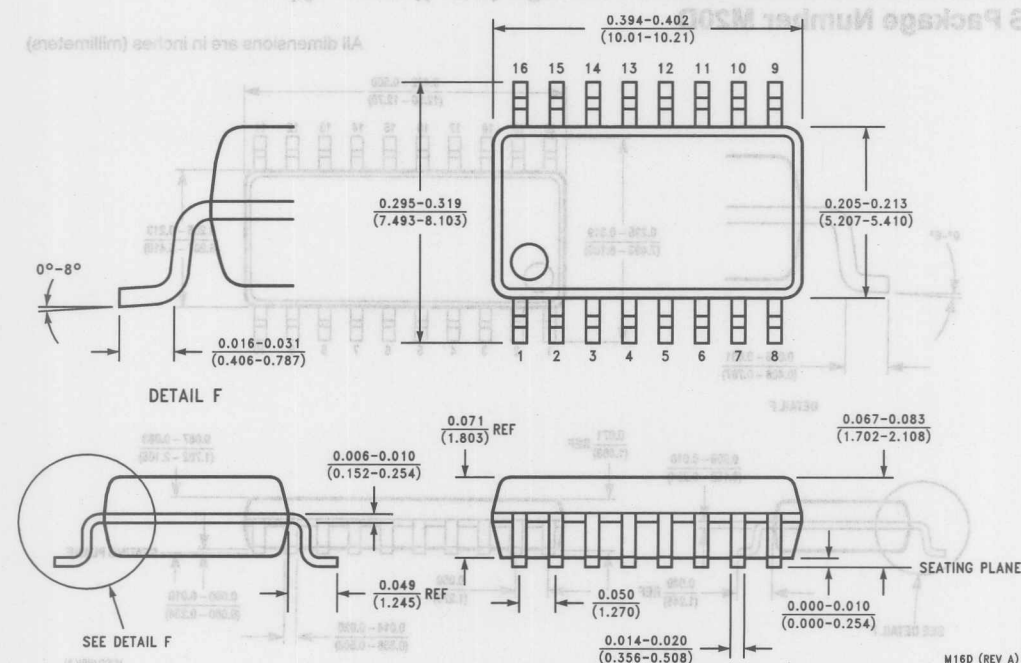
# 16 Lead (0.150" Wide) Molded Small Outline Package, JEDEC NS Package Number M16A

All dimensions are in inches (millimeters)



# 16 Lead Molded Small Outline Package (SOP), EIAJ Type II NS Package Number M16D

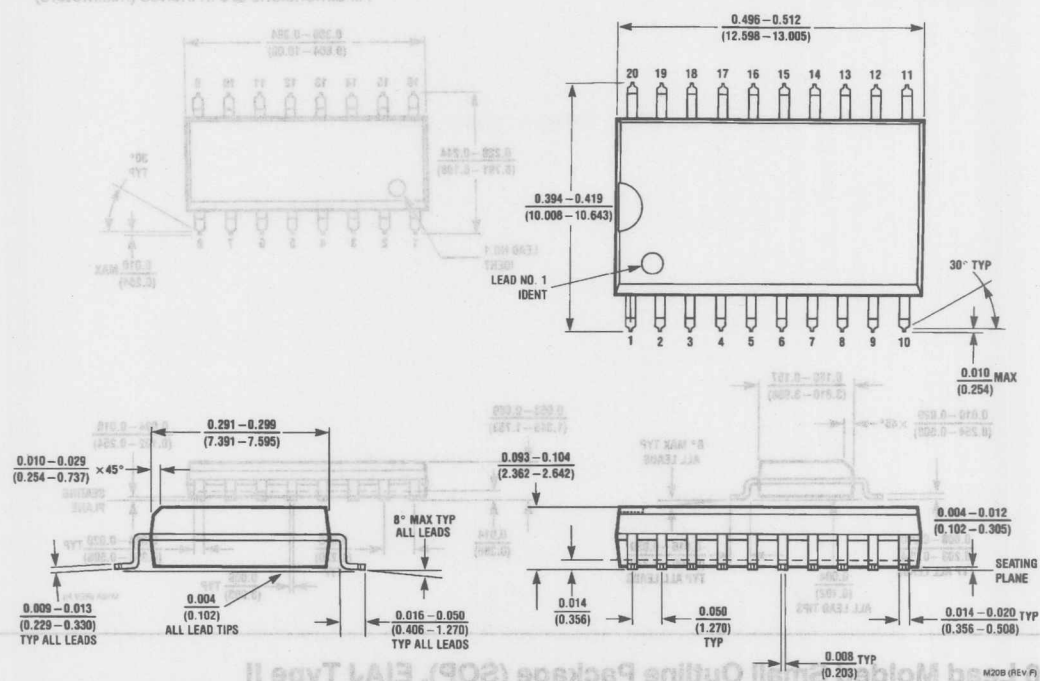
All dimensions are in inches (millimeters)



# 20 Lead (0.300" Wide) Molded Small Outline Package, JEDEC NS Package Number M20B

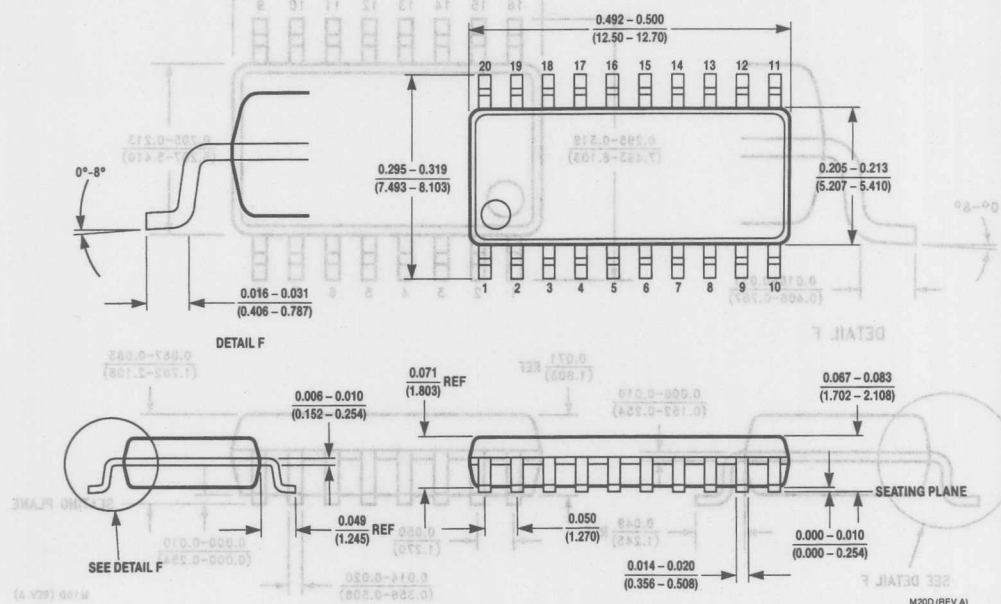
All dimensions are in inches (millimeters)

All dimensions are in inches (millimeters)



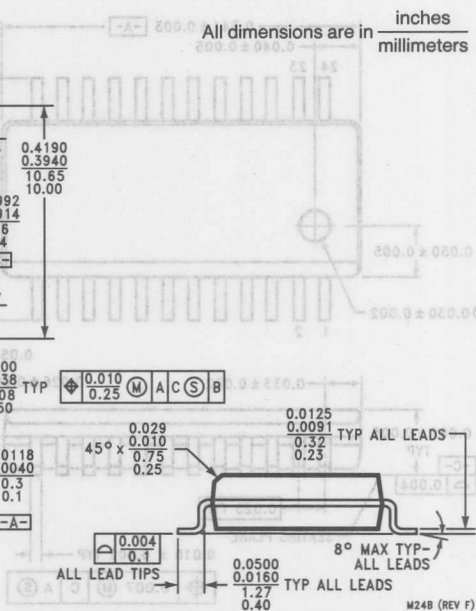
## 20 Lead Molded Small Outline Package (SOP), EIAJ Type II NS Package Number M20D

All dimensions are in inches (millimeters)



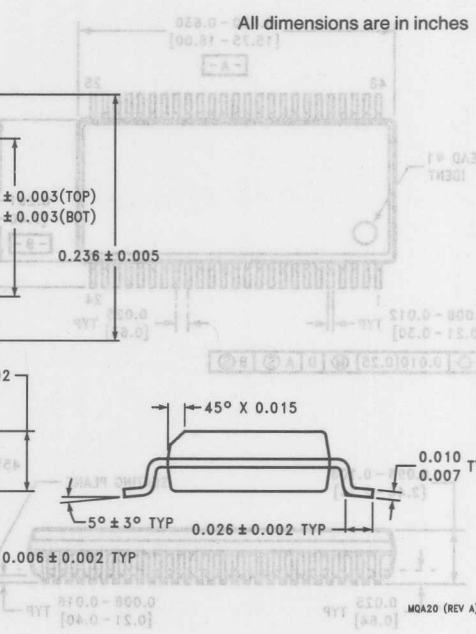
Package, JEDEC

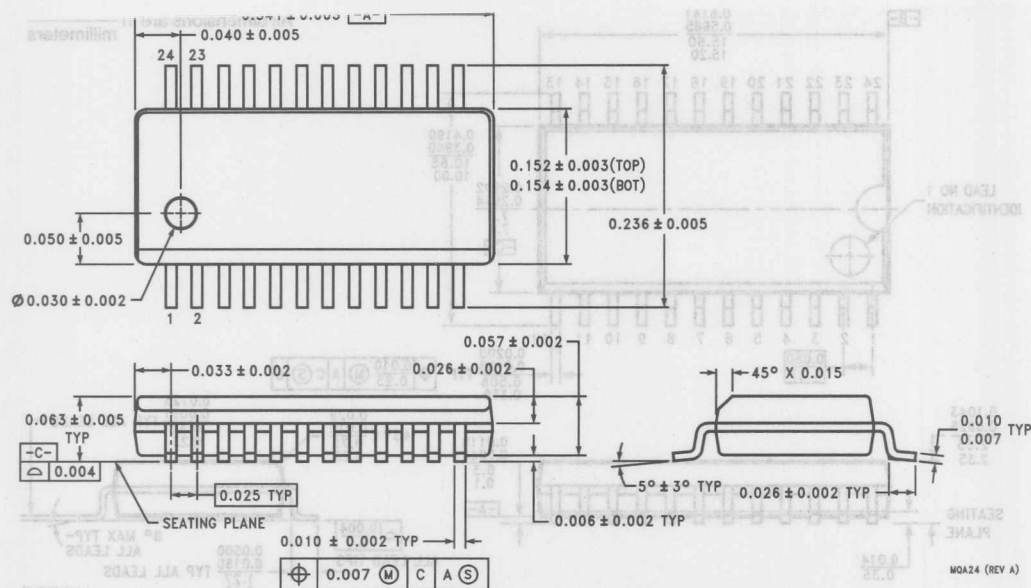
All dimensions are in  $\frac{\text{inches}}{\text{millimeters}}$



### Outline Package, JEDEC

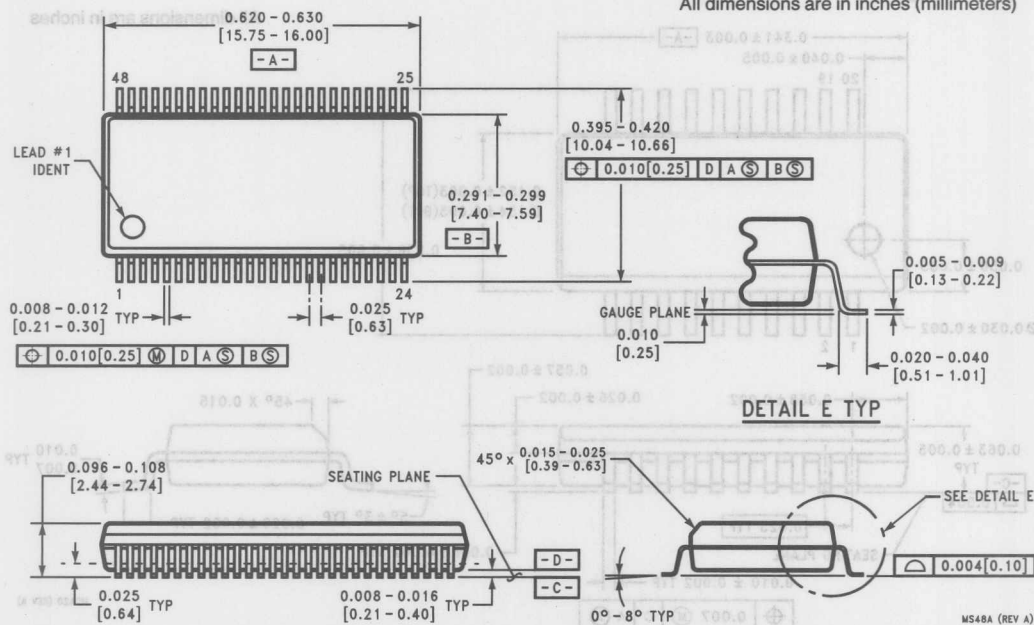
033.0 - All dimensions are in inches



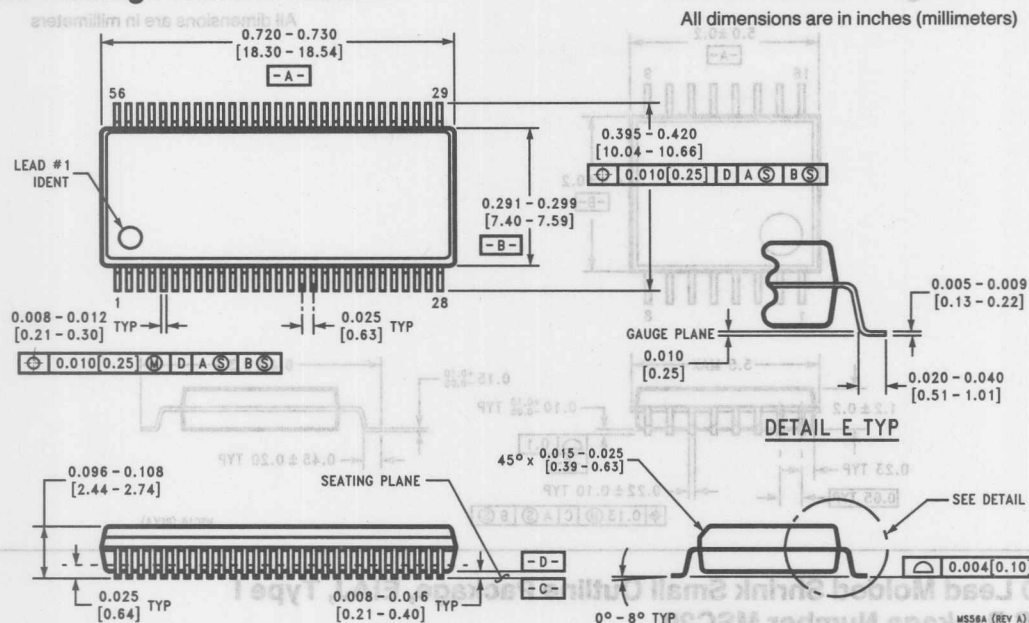


### 48 Lead (0.300" Wide) Molded Shrink Small Outline Package, JEDEC NS Package Number MS48A

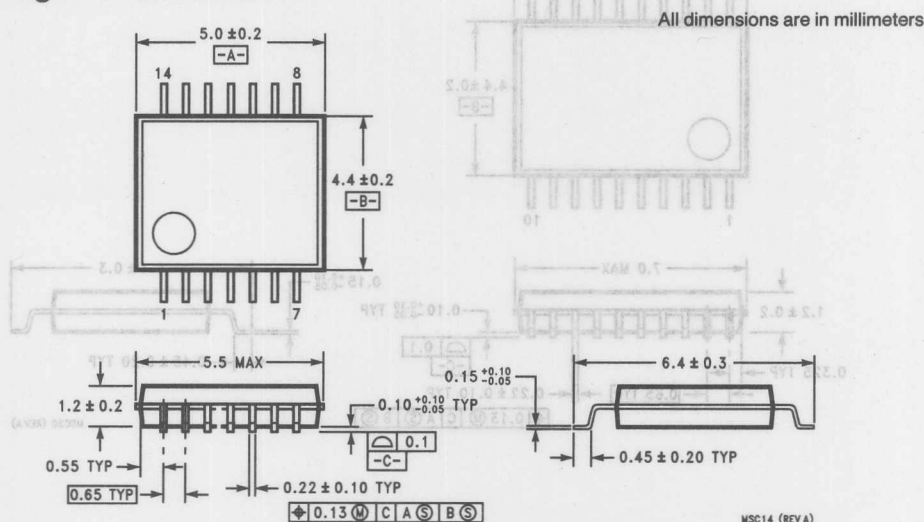
All dimensions are in inches (millimeters)



# 56 Lead (0.300" Wide) Molded Shrink Small Outline Package, JEDEC NS Package Number MS56A

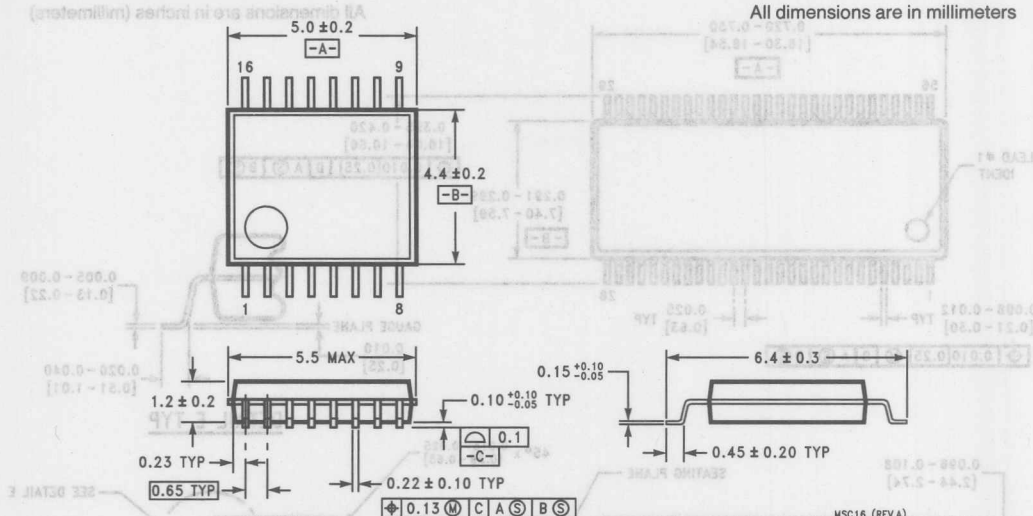


## 14 Lead Molded Shrink Small Outline Package, EIAJ, Type I NS Package Number MSC14



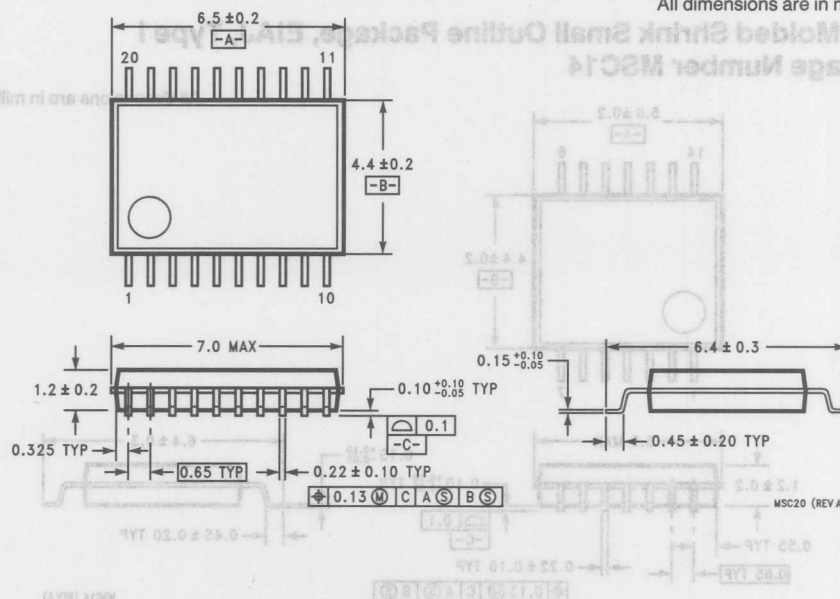
# 16 Lead Molded Shrink Small Outline Package, EIAJ, Type I NS Package Number MSC16

All dimensions are in millimeters



# 20 Lead Molded Shrink Small Outline Package, EIAJ, Type I NS Package Number MSC20

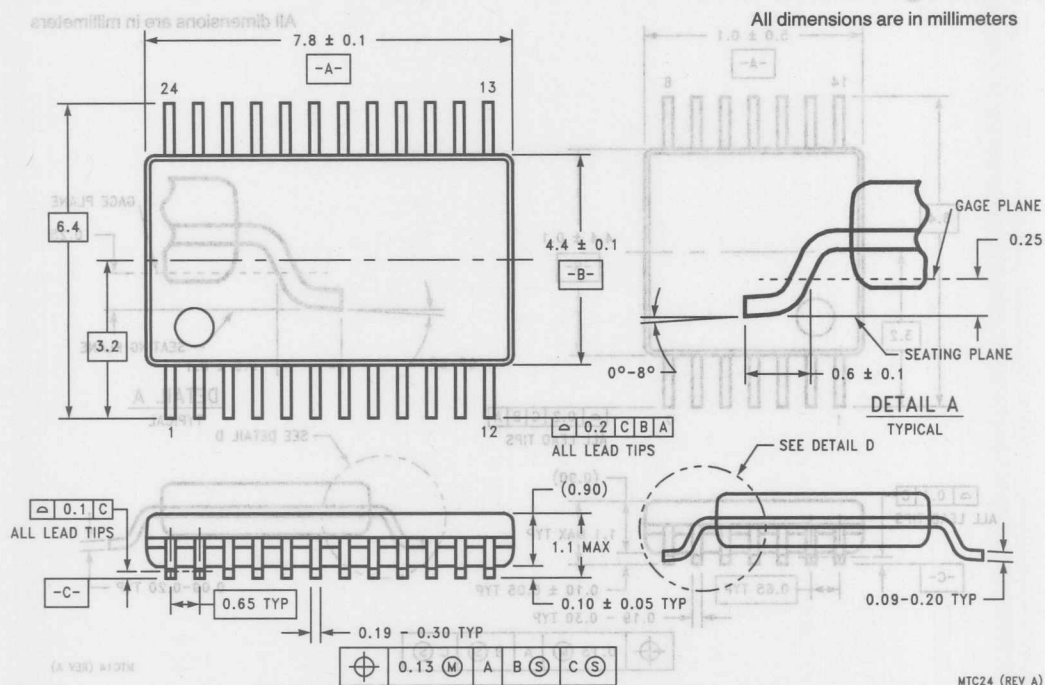
All dimensions are in millimeters



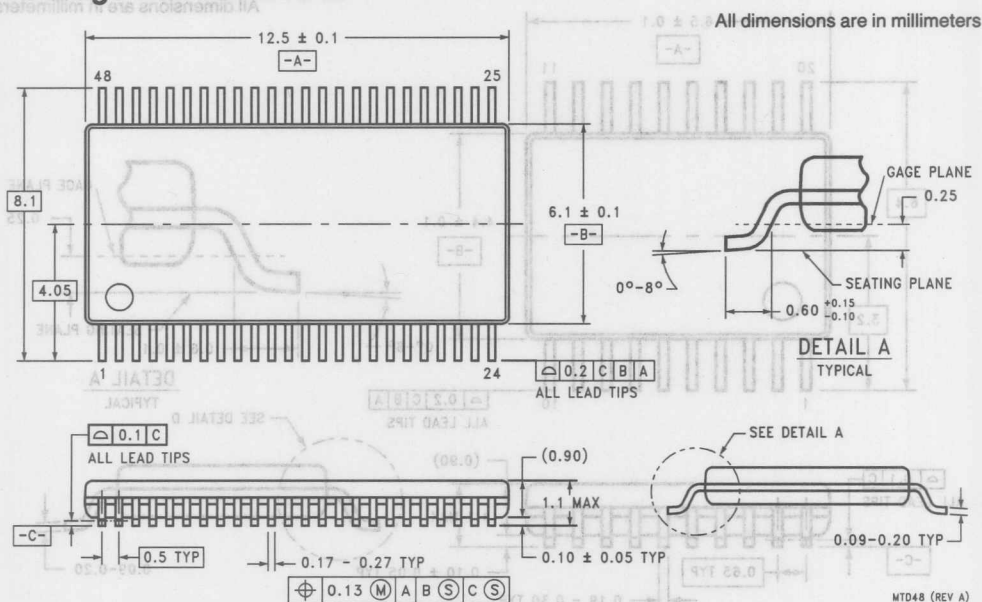
age, JEDEC

age, JEDEC

← All dimensions are in millimeters

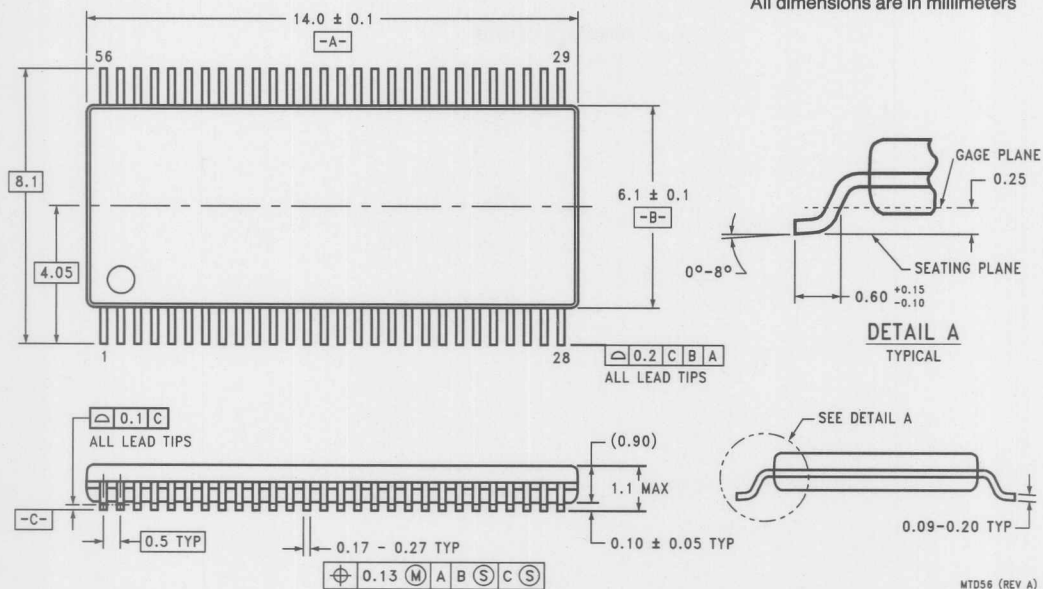


### 48 Lead Molded Thin Shrink Small Outline Package, JEDEC NS Package Number MTD48



# 56 Lead Molded Thin Shrink Small Outline Package, JEDEC NS Package Number MTD56

All dimensions are in millimeters



56 Lead Molded Thin Shrink Small Package, JEDEC  
MS Package Number MTD56

All dimensions are in millimeters

